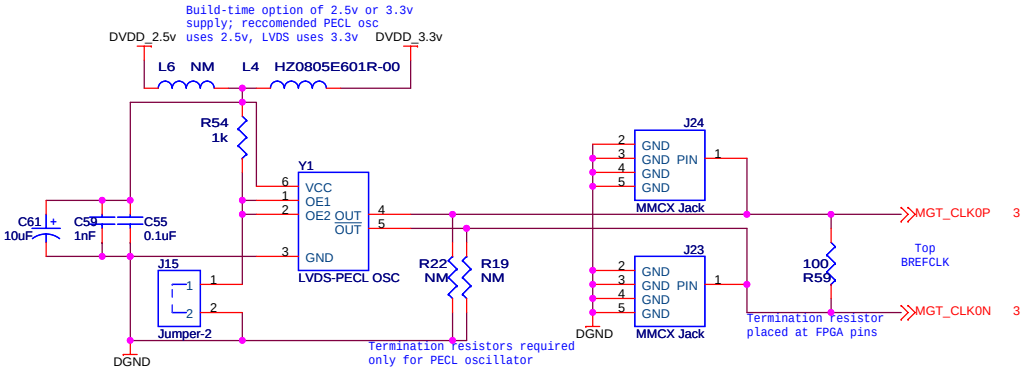
WARP FPGA Board

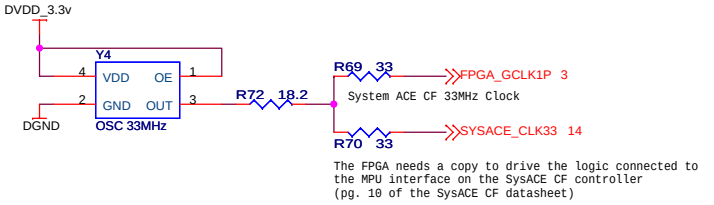
Rev 1.2 - June 2006

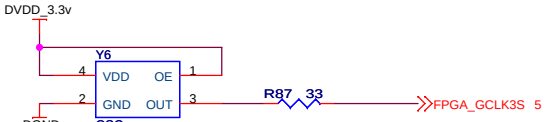
Patrick Murphy

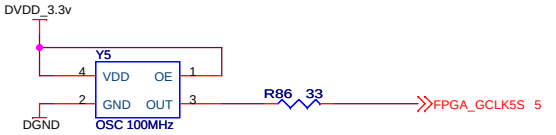
Schematic Pages:

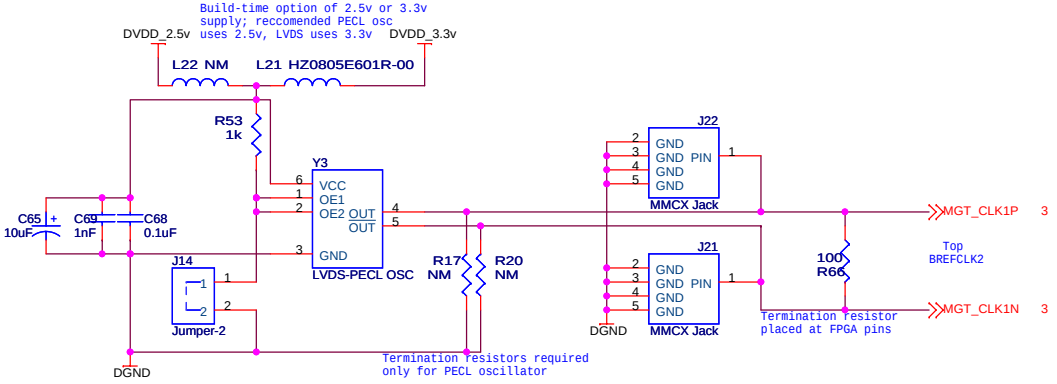
Rice University
Title
WARP FPGA Board
Description
Table of Contents
Rev
1.2
Date: Saturday, June 17, 2006
Sheet 1 of 17

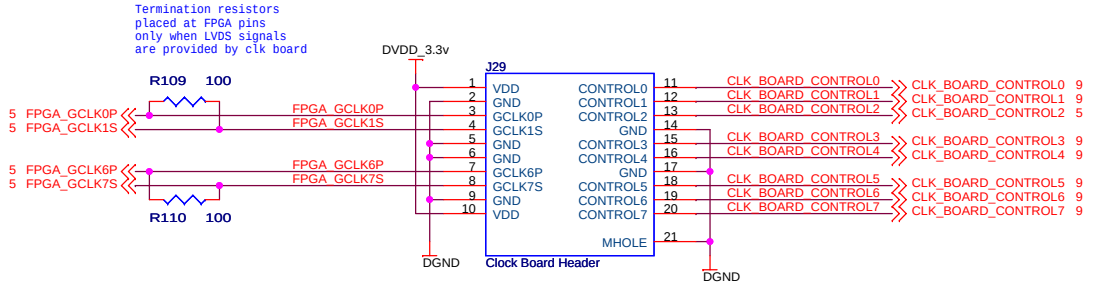




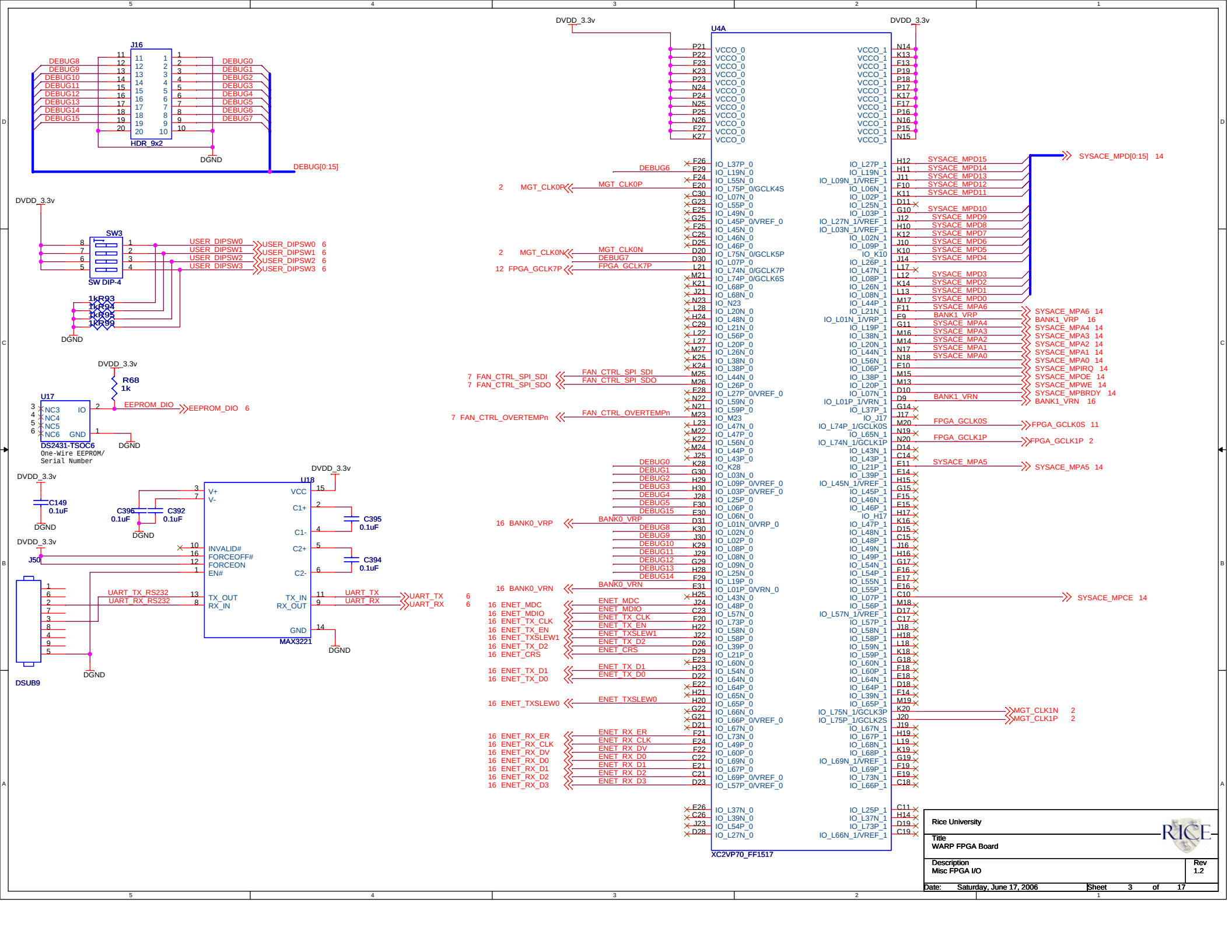


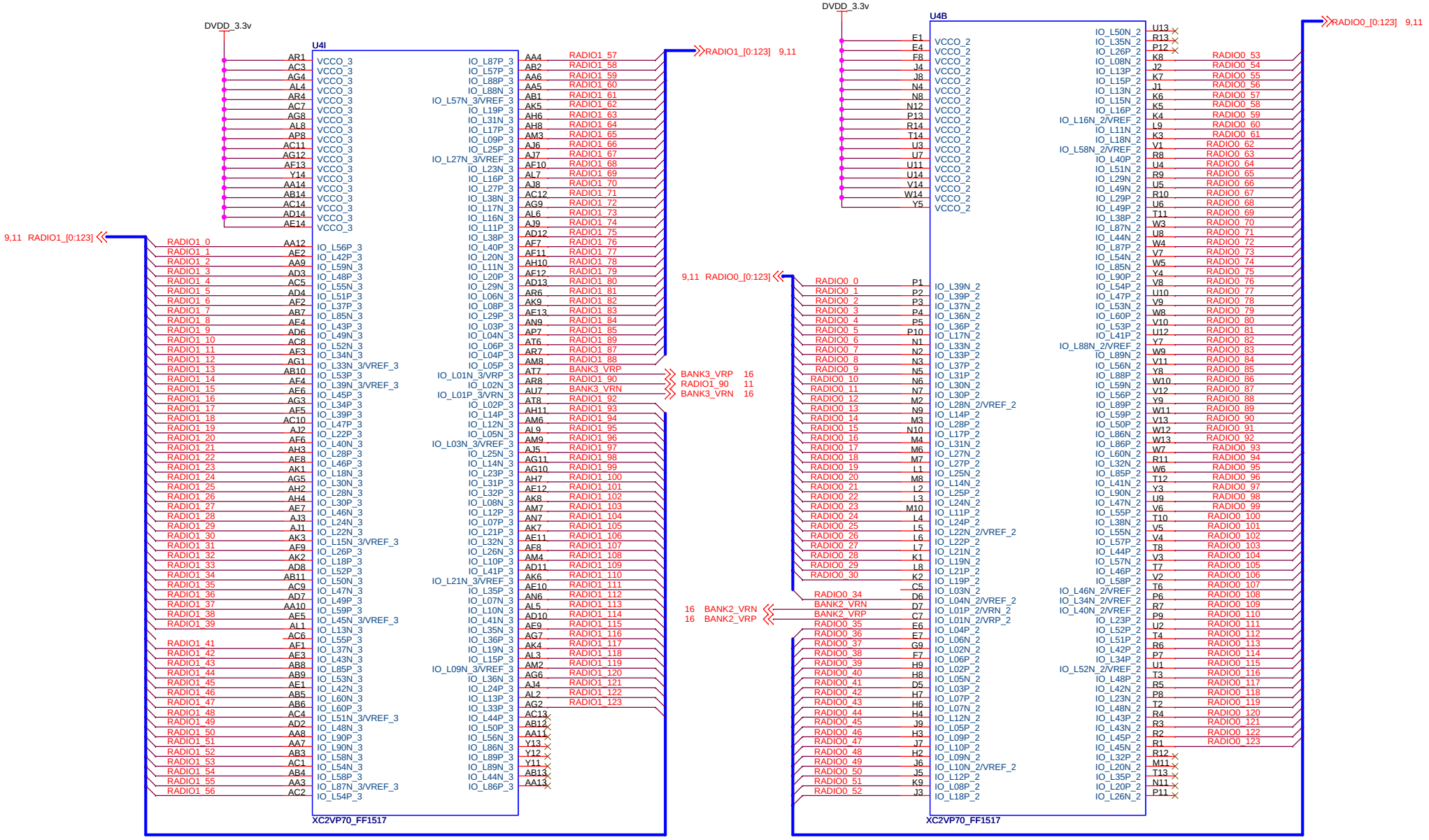




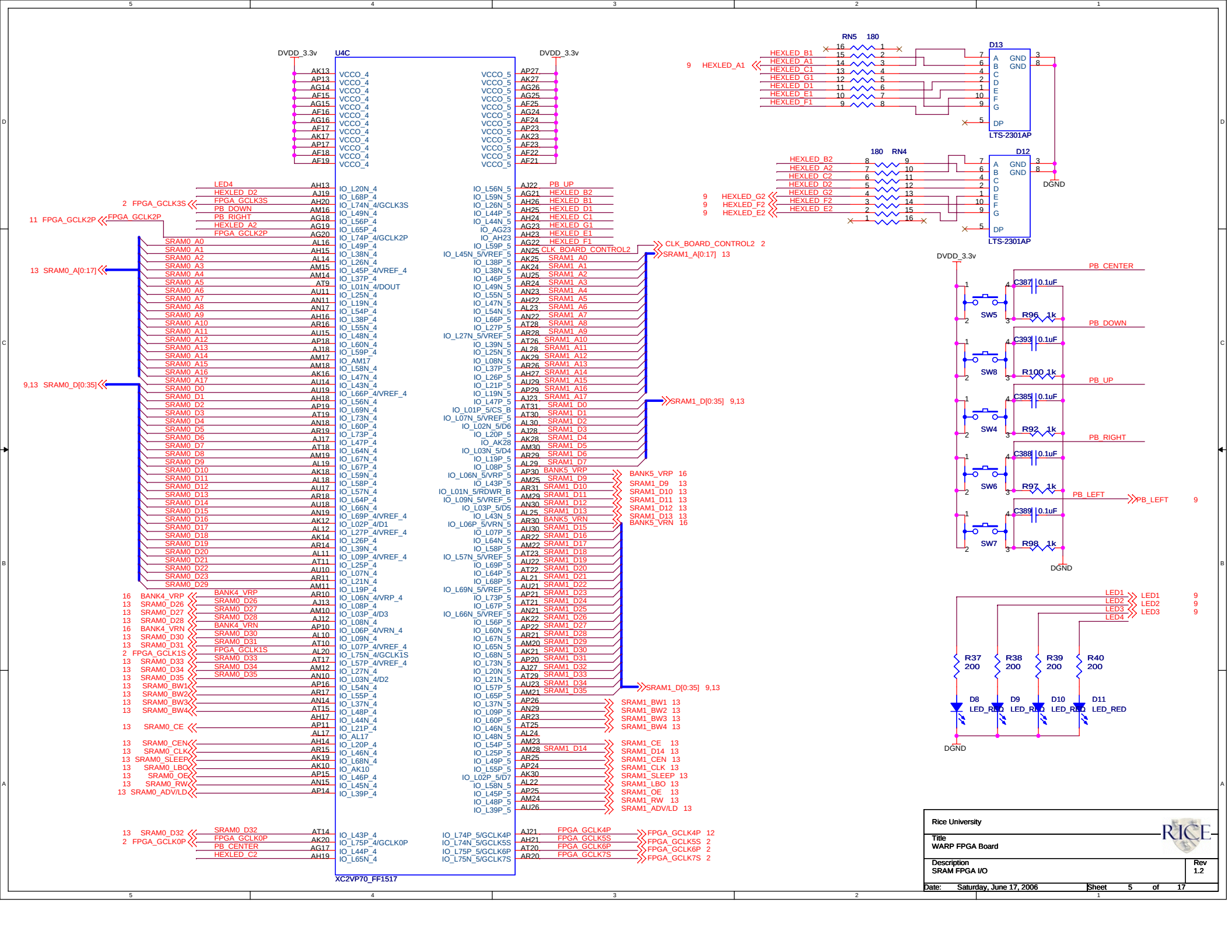


Rice University		
Title: WARP FPGA Board		
Description: Clocks		Rev: 1.2
Date: Saturday, June 17, 2006	Sheet 2 of 17	

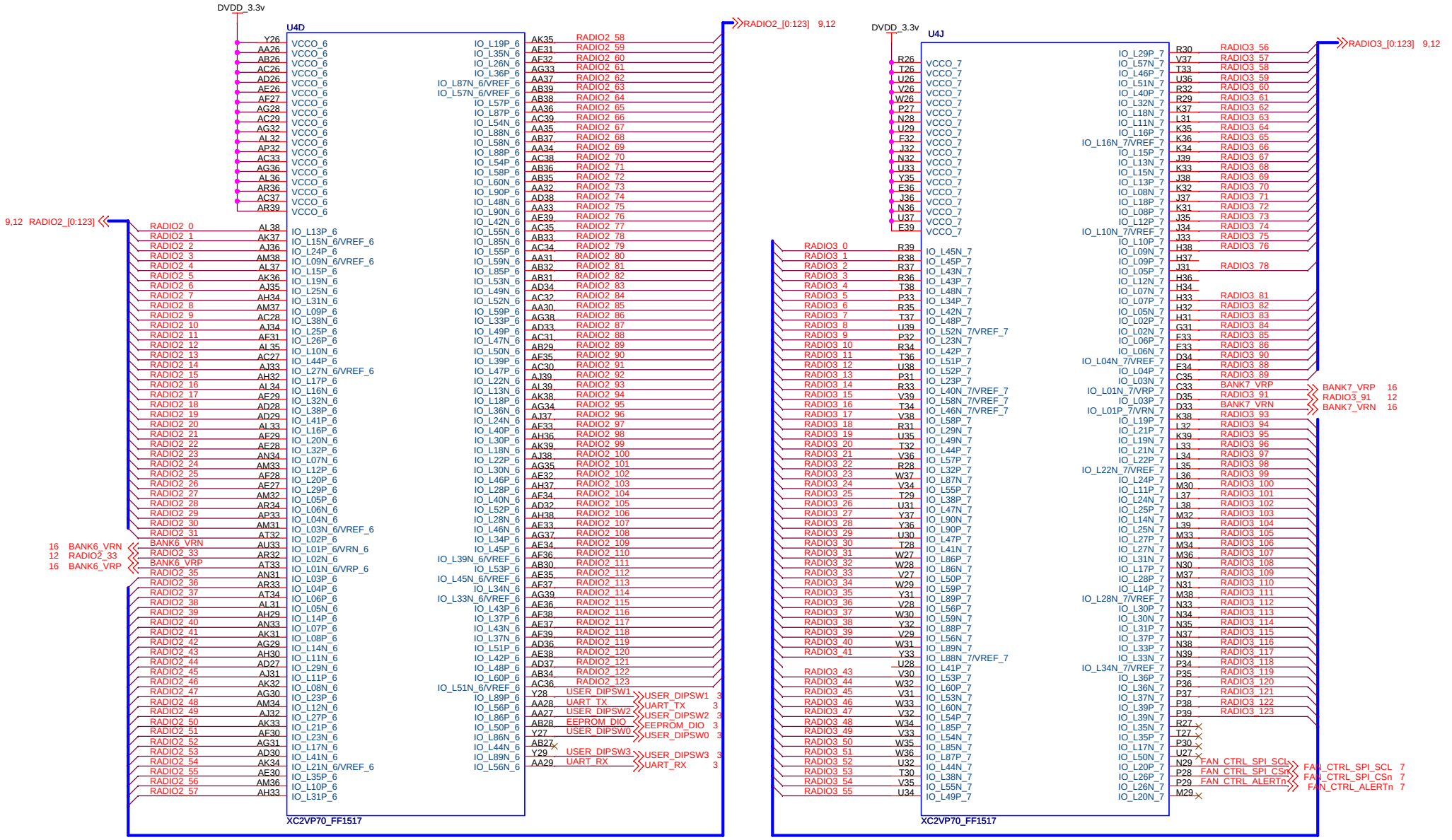

J16
HDR_9x2
DEBUG8
DEBUG9
DEBUG10
DEBUG11
DEBUG12
DEBUG13
DEBUG14
DEBUG15
DEBUG0
DEBUG1
DEBUG2
DEBUG3
DEBUG4
DEBUG5
DEBUG6
DEBUG7
DGND
DEBUG[0:15]
DVDD_3.3v
SW3
SW DIP-4
USER_DIPSW0
USER_DIPSW1
USER_DIPSW2
USER_DIPSW3
1kR93
1kR94
1kR95
1kR96
U17
DS2431-TSOC6
One-Wire EEPROM/
Serial Number
R68
1k
EEPROM_DIO
U18
MAX3221
C149
0.1uF
C396
C392
C395
C394
J50
DSUB9
UART_TX_RS232
UART_RX_RS232
UART_TX
UART_RX
U4A
XC2VP70_FF1517
MGT_CLK0P
MGT_CLK0N
FPGA_GCLK7P
DEBUG7
FAN_CTRL_SPI_SDI
FAN_CTRL_SPI_SDO
FAN_CTRL_OVERTEMPn
BANK0_VRP
BANK0_VRN
ENET_MDC
ENET_MDIO
ENET_TX_CLK
ENET_TX_EN
ENET_TXSLEW1
ENET_TX_D2
ENET_CRS
ENET_TX_D1
ENET_TX_D0
ENET_TXSLEW0
ENET_RX_ER
ENET_RX_CLK
ENET_RX_DV
ENET_RX_D0
ENET_RX_D1
ENET_RX_D2
ENET_RX_D3
SYSACE_MPD[0:15]
SYSACE_MPA6
BANK1_VRP
SYSACE_MPA4
SYSACE_MPA3
SYSACE_MPA2
SYSACE_MPA1
SYSACE_MPA0
SYSACE_MPIRQ
SYSACE_MPOE
SYSACE_MPWE
SYSACE_MPBRDY
BANK1_VRN
SYSACE_MPA5
FPGA_GCLK0S
FPGA_GCLK1P
SYSACE_MPCE
MGT_CLK1N
MGT_CLK1P
Rice University
Title
WARP FPGA Board
Description
Misc FPGA I/O
Rev
1.2
Date: Saturday, June 17, 2006
Sheet 3 of 17



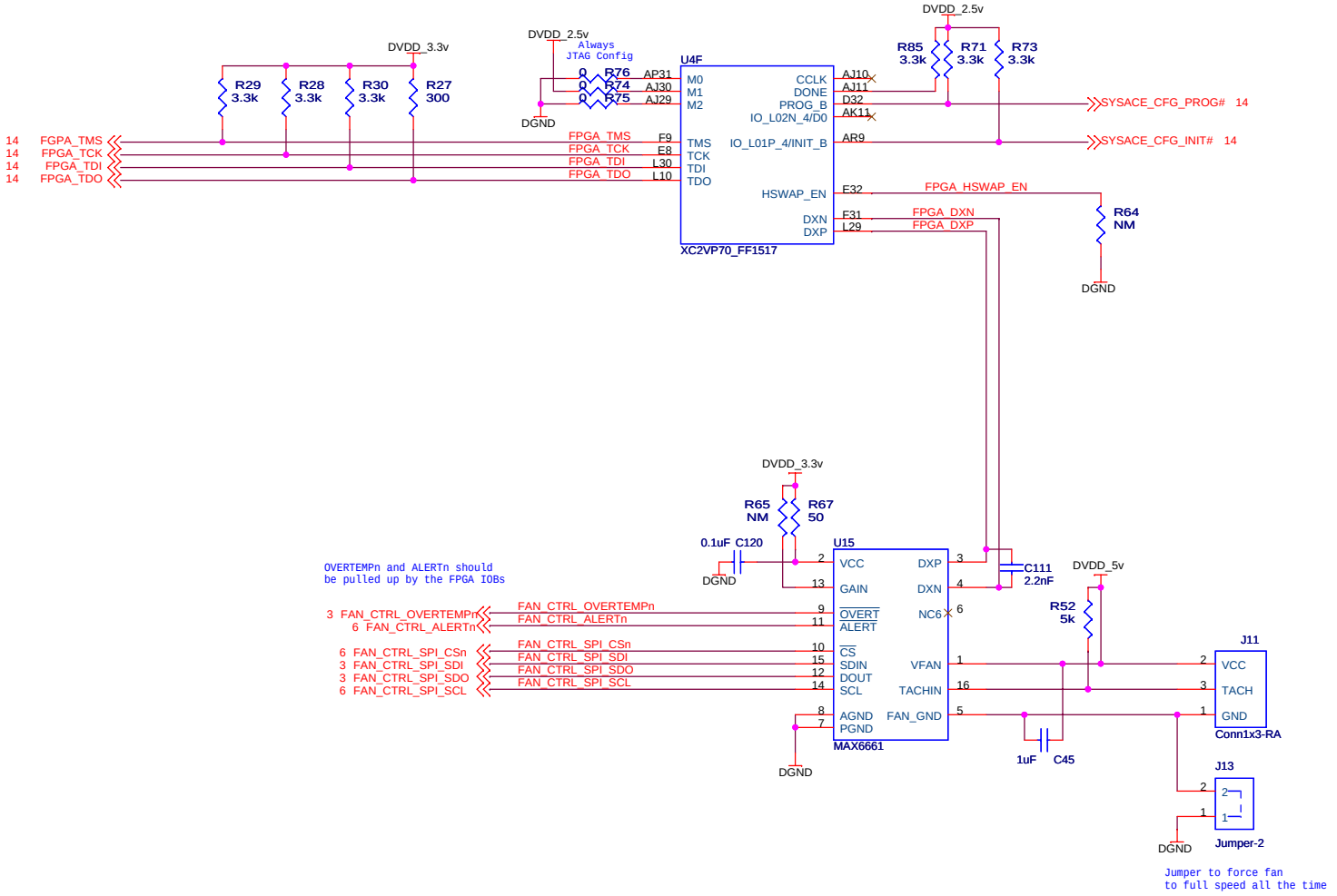
Rice University	
Title: WARP FPGA Board	
Description: Daughtercards 0-1 FPGA I/O	Rev: 1.2
Date: Saturday, June 17, 2006	Sheet 4 of 17



Rice University	
Title: WARP FPGA Board	
Description: SRAM FPGA I/O	Rev: 1.2
Date: Saturday, June 17, 2006	Sheet 5 of 17



Rice University	
Title: WARP FPGA Board	
Description: Daughtercards 2-3 FPGA I/O	Rev: 1.2
Date: Saturday, June 17, 2006	Sheet 6 of 17



Rice University	
Title: WARP FPGA Board	
Description: FPGA JTAG, Configuration & Temperature Control	Rev: 1.2
Date: Saturday, June 17, 2006	Sheet 7 of 17

Notes:
MGTB_AGND: Analog ground for bottom edge MGTs
MGTT_AGND: Analog ground for top edge MGTs
MGT_2.5v: Dedicated MGT power supply
MGT_VTR_x: MGT Rx termination voltage
(tied to MGT_2.5v for DC coupling, 1.8v for AC)

DVDD_2.5v

Unused MGTs must still be powered
See pg. 14 of the V2Pro Datasheet for details

U4E

Bottom Edge MGTs

Top Edge MGTs

XC2VP70_FF1517

MGT_2.5v

MGT_VTR_1 MGT_VTR_2 MGT_VTR_3 MGT_VTR_4 MGT_VTR_5 MGT_VTR_6 MGT_VTR_7 MGT_VTR_8

MGT_1.8v

MGTB_AGND

MGTT_AGND

DGND

HSSDC2 Jack

J8 J4 J7 J3 J6 J9 J5 J10

HDR_3x1

Four MGTs always set for DC-coupled links
Four MGTs configurable for AC or DC-coupled links

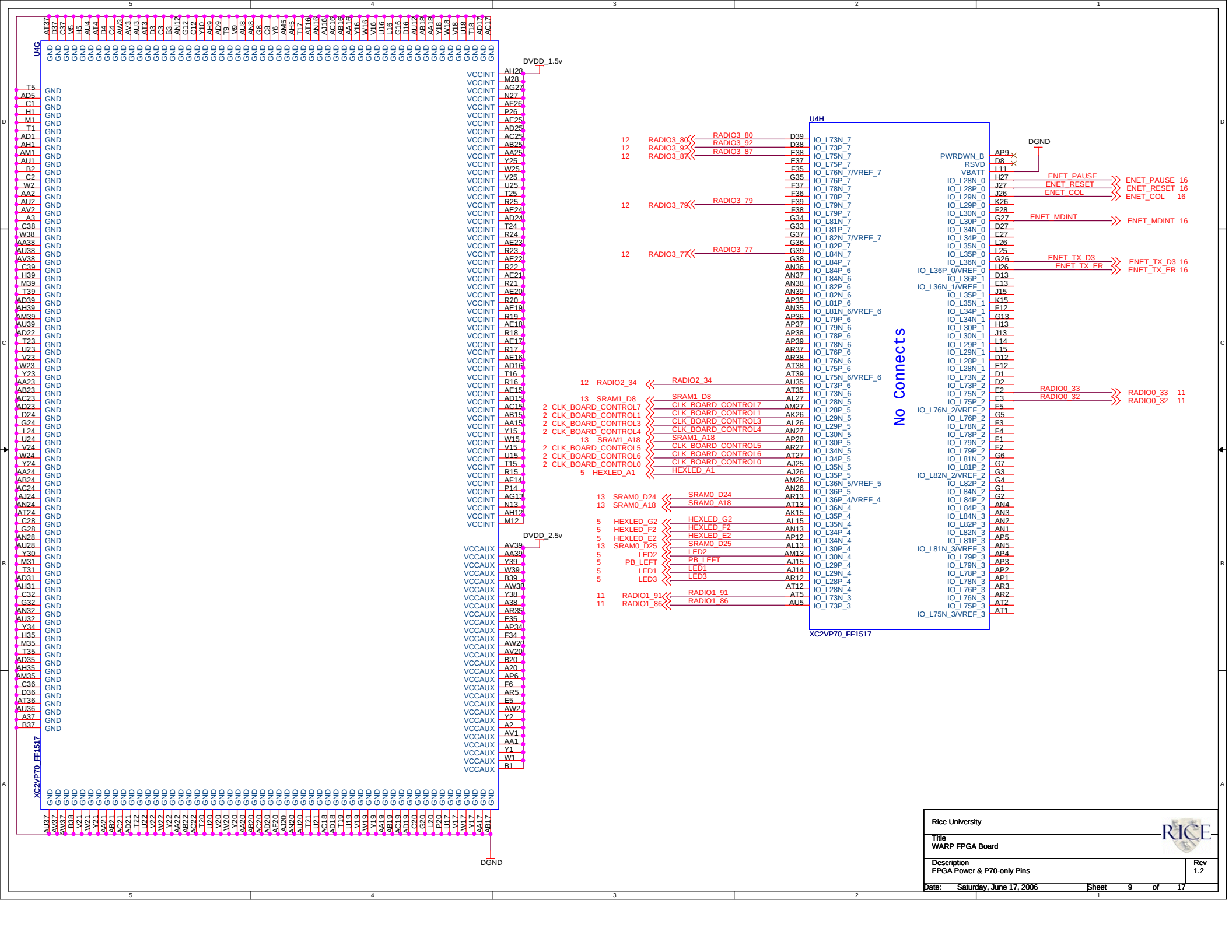
Analog/Digital Ground Filtering

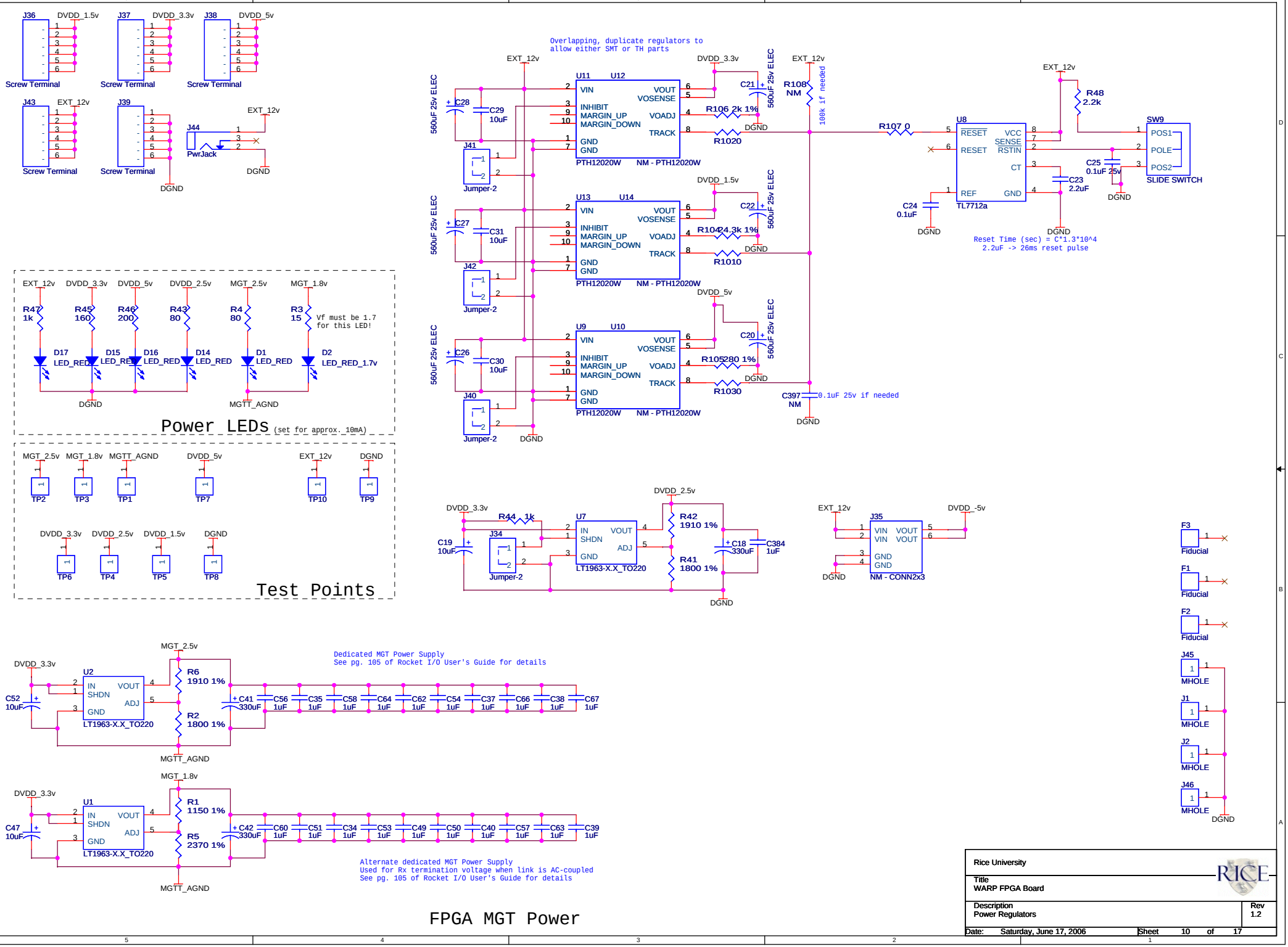
Top MGTs are used, so copule their AGND through inductors

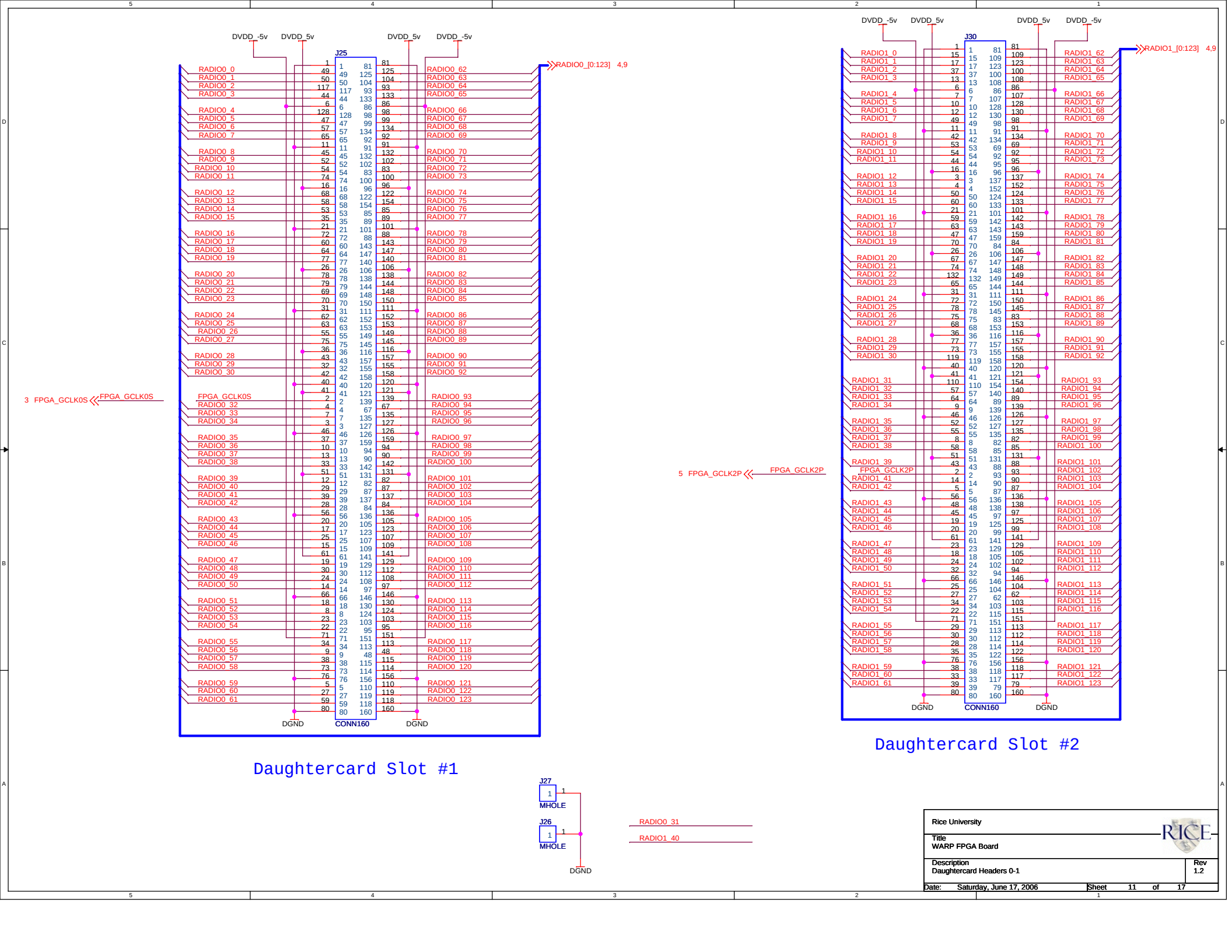
L23 PLM18AG102SN1
L5 PLM18AG102SN1
L18 PLM18AG102SN1
L43 PLM18AG102SN1
L2 PLM18AG102SN1

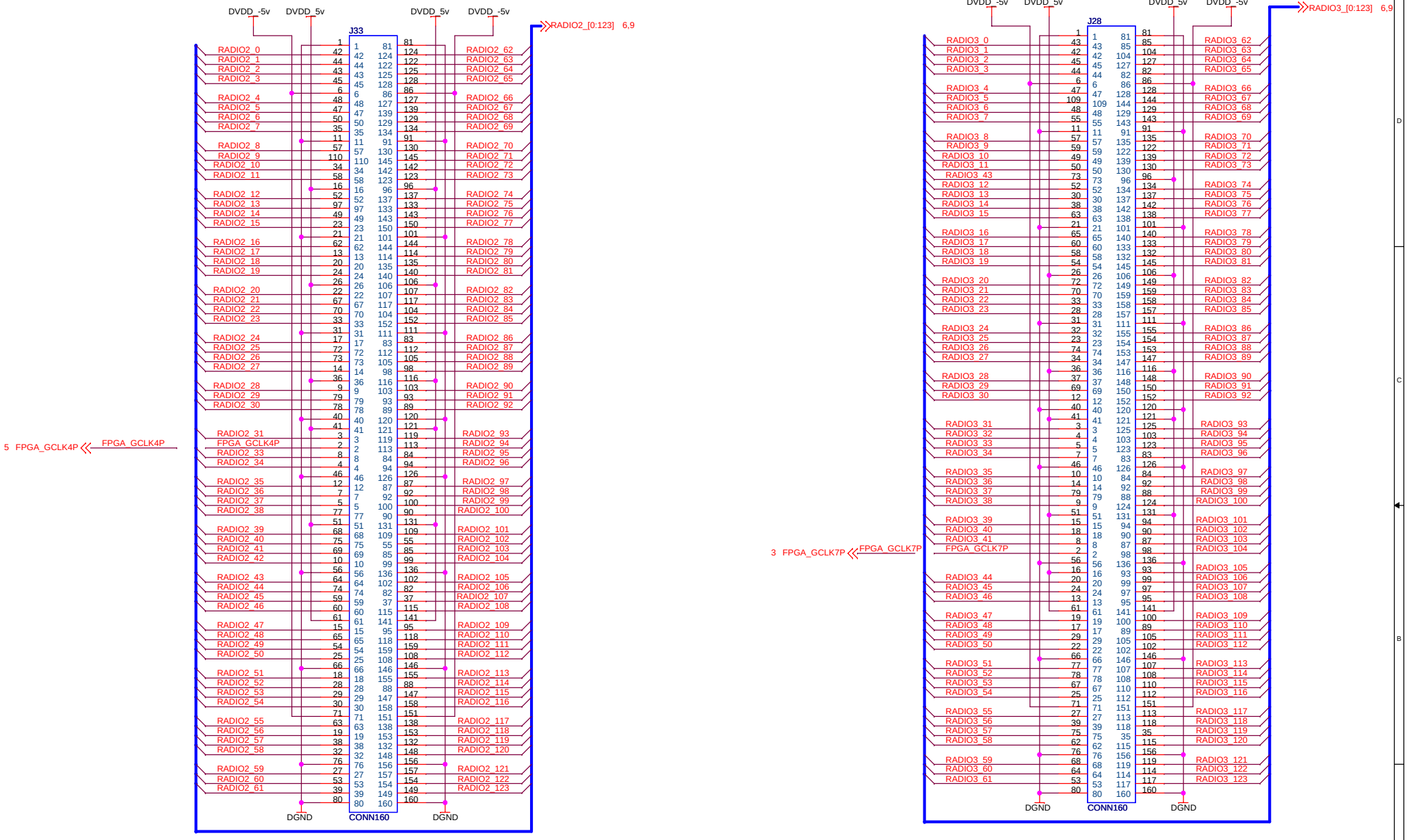
Bottom MGTs are unused, so their AGND is just DGND

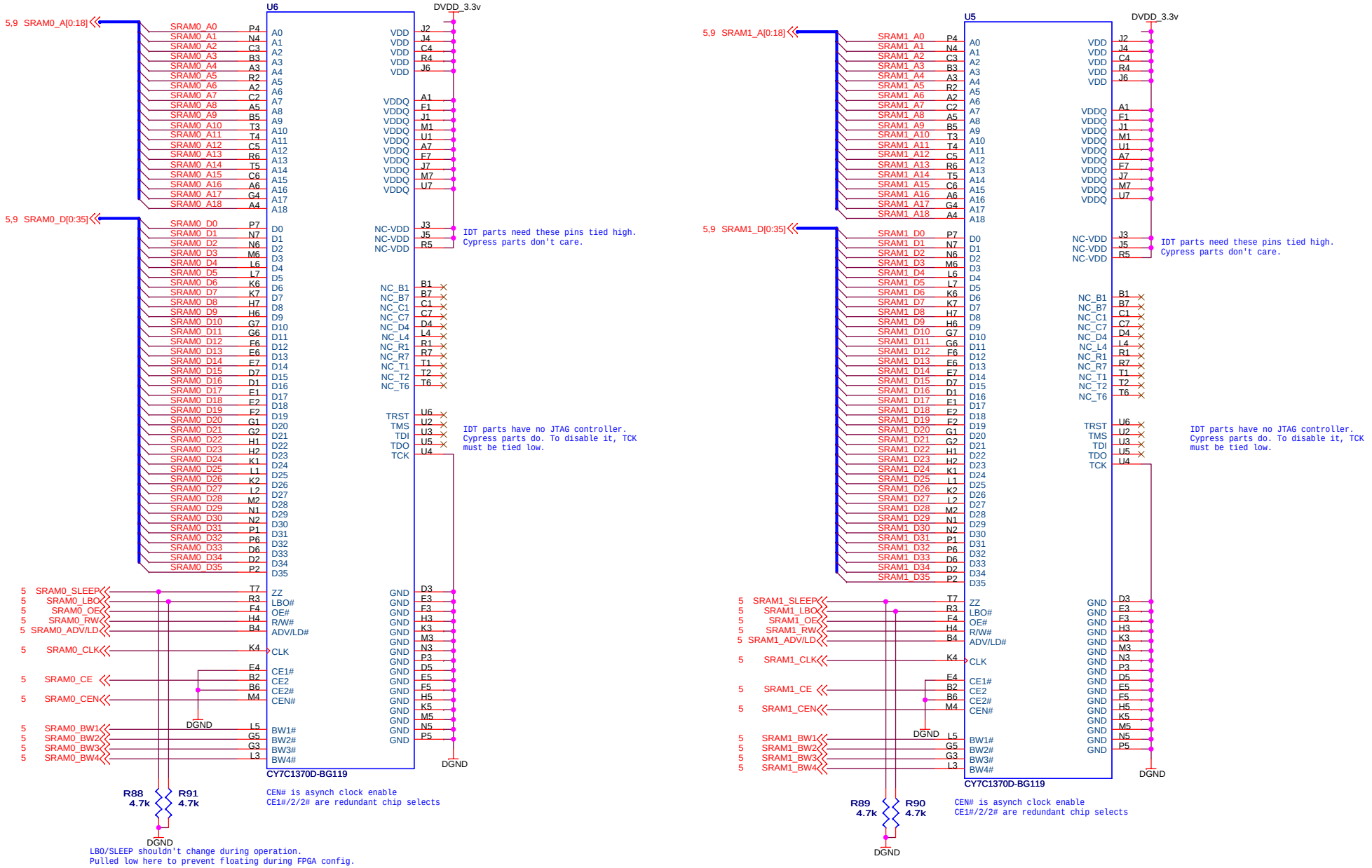
Rice University	
Title: WARP FPGA Board	
Description: Multi-gigabit Transceivers	Rev: 1.2
Date: Saturday, June 17, 2006	Sheet 8 of 17


U4G
XC2VP70_FF1517
DVDD_1.5v
DVDD_2.5v
DGND
U4H
XC2VP70_FF1517
No Connects
RADIO3_80
RADIO3_92
RADIO3_87
RADIO3_79
RADIO3_77
RADIO2_34
SRAM1_D8
CLK_BOARD_CONTROL7
CLK_BOARD_CONTROL1
CLK_BOARD_CONTROL3
CLK_BOARD_CONTROL4
SRAM1_A18
CLK_BOARD_CONTROL5
CLK_BOARD_CONTROL6
CLK_BOARD_CONTROL0
HEXLED_A1
SRAM0_D24
SRAM0_A18
HEXLED_G2
HEXLED_F2
HEXLED_E2
SRAM0_D25
LED2
PB_LEFT
LED1
LED3
RADIO1_91
RADIO1_86
ENET_PAUSE
ENET_RESET
ENET_COL
ENET_MDINT
ENET_TX_D3
ENET_TX_ER
RADIO0_33
RADIO0_32
Rice University
Title
WARP FPGA Board
Description
FPGA Power & P70-only Pins
Rev
1.2
Date: Saturday, June 17, 2006
Sheet 9 of 17

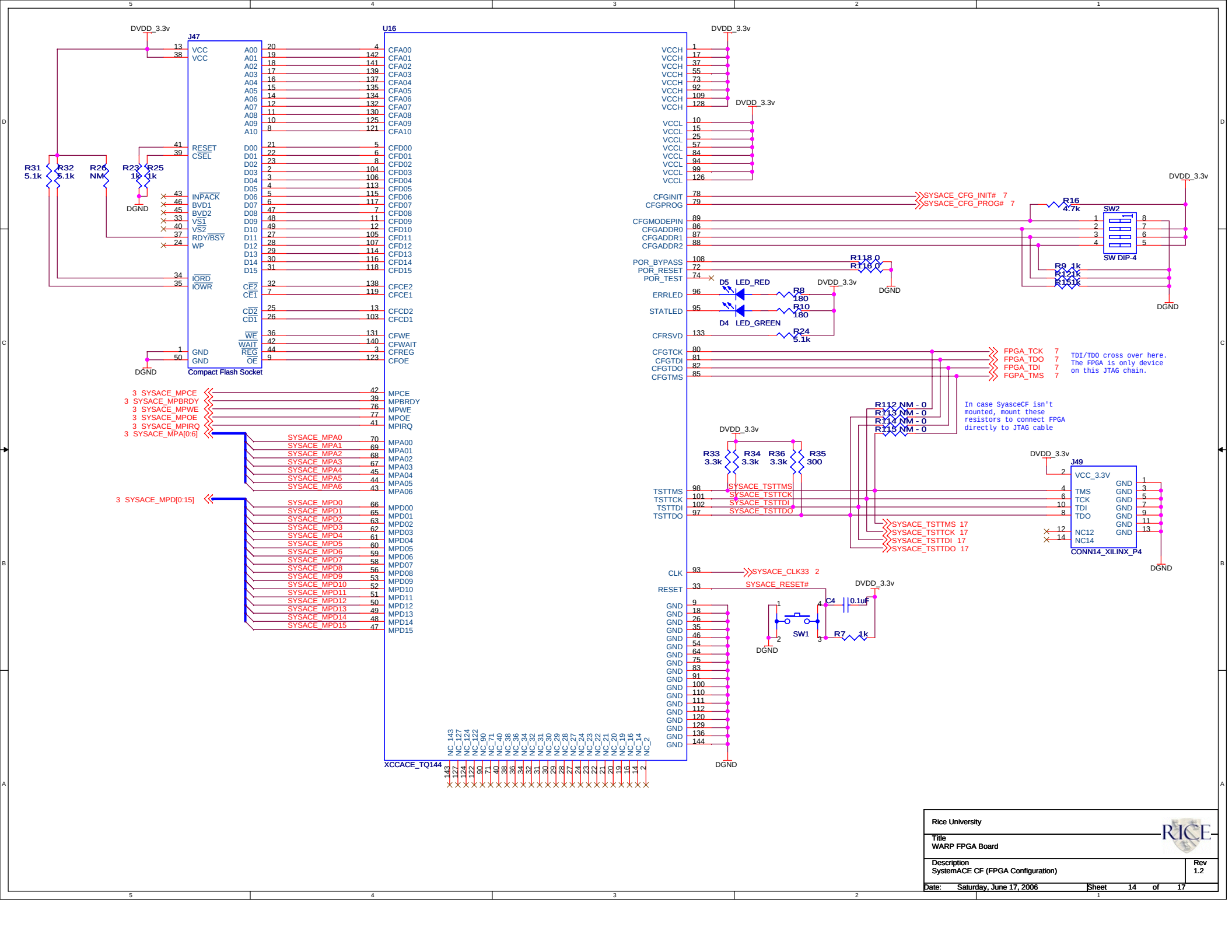

J36 DVDD_1.5v
J37 DVDD_3.3v
J38 DVDD_5v
Screw Terminal
J43 EXT_12v
J39
J44
PwrJack
DGND
Overlapping, duplicate regulators to allow either SMT or TH parts
EXT_12v
DVDD_3.3v
DVDD_1.5v
DVDD_5v
U11 U12
U13 U14
U9 U10
VIN
VOUT
VOSENSE
INHIBIT
MARGIN_UP
MARGIN_DOWN
VOADJ
TRACK
GND
PTH12020W
NM - PTH12020W
560uF 25v ELEC
C28 C29 10uF
C27 C31 10uF
C26 C30 10uF
C21
C22
C20
R106 2k 1%
R1024.3k 1%
R105280 1%
R1020
R1010
R1030
R108 NM
100k if needed
R107 0
C397 NM
0.1uF 25v if needed
J41
J42
J40
Jumper-2
U8
TL7712a
RESET
VCC
SENSE
RSTIN
CT
REF
R48 2.2k
C25 0.1uF 25v
C23 2.2uF
C24 0.1uF
SW9
POS1
POLE
POS2
SLIDE SWITCH
Reset Time (sec) = C*1.3*10^4
2.2uF -> 26ms reset pulse
EXT_12v
DVDD_3.3v
DVDD_5v
DVDD_2.5v
MGT_2.5v
MGT_1.8v
R47 1k
R45 160
R46 200
R43 80
R4 80
R3 15
Vf must be 1.7 for this LED!
D17 LED_RED
D15 LED_RED
D16 LED_RED
D14 LED_RED
D1 LED_RED
D2 LED_RED_1.7v
DGND
MGTT_AGND
Power LEDs (set for approx. 10mA)
MGT_2.5v
MGT_1.8v
MGTT_AGND
DVDD_5v
EXT_12v
DGND
TP2
TP3
TP1
TP7
TP10
TP9
DVDD_3.3v
DVDD_2.5v
DVDD_1.5v
DGND
TP6
TP4
TP5
TP8
Test Points
DVDD_3.3v
R44 1k
U7
IN
SHDN
VOUT
ADJ
GND
LT1963-X.X_TO220
J34
Jumper-2
C19 10uF
DVDD_2.5v
R42 1910 1%
R41 1800 1%
C18 330uF
C384 1uF
DGND
EXT_12v
DVDD_-5v
J35
VIN
VOUT
GND
NM - CONN2x3
F3
F1
F2
Fiducial
J45
J1
J2
J46
MHOLE
DGND
MGT_2.5v
DVDD_3.3v
U2
C52 10uF
R6 1910 1%
R2 1800 1%
C41 330uF
C56 C35 C58 C64 C62 C54 C37 C66 C38 C67 1uF
MGTT_AGND
Dedicated MGT Power Supply
See pg. 105 of Rocket I/O User's Guide for details
MGT_1.8v
U1
C47 10uF
R1 1150 1%
R5 2370 1%
C42 330uF
C60 C51 C34 C53 C49 C50 C40 C57 C63 C39 1uF
Alternate dedicated MGT Power Supply
Used for Rx termination voltage when link is AC-coupled
See pg. 105 of Rocket I/O User's Guide for details
FPGA MGT Power
Rice University
Title
WARP FPGA Board
Description
Power Regulators
Rev
1.2
Date: Saturday, June 17, 2006
Sheet 10 of 17


DVDD_-5v
DVDD_5v
J25
RADIO0_[0:123] 4,9
3 FPGA_GCLK0S
FPGA_GCLK0S
DGND
CONN160
Daughtercard Slot #1
J30
RADIO1_[0:123] 4,9
5 FPGA_GCLK2P
FPGA_GCLK2P
Daughtercard Slot #2
J27
MHOLE
J26
RADIO0_31
RADIO1_40
Rice University
Title
WARP FPGA Board
Description
Daughtercard Headers 0-1
Rev
1.2
Date: Saturday, June 17, 2006
Sheet 11 of 17

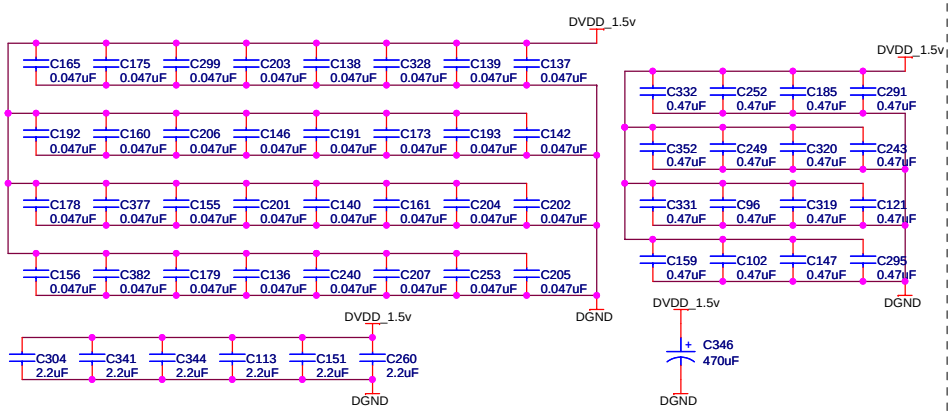

DVDD_-5v
DVDD_5v
DVDD_5v
DVDD_-5v
RADIO2_[0:123] 6,9
J33
CONN160
DGND
DGND
RADIO2_0
RADIO2_1
RADIO2_2
RADIO2_3
RADIO2_4
RADIO2_5
RADIO2_6
RADIO2_7
RADIO2_8
RADIO2_9
RADIO2_10
RADIO2_11
RADIO2_12
RADIO2_13
RADIO2_14
RADIO2_15
RADIO2_16
RADIO2_17
RADIO2_18
RADIO2_19
RADIO2_20
RADIO2_21
RADIO2_22
RADIO2_23
RADIO2_24
RADIO2_25
RADIO2_26
RADIO2_27
RADIO2_28
RADIO2_29
RADIO2_30
RADIO2_31
FPGA_GCLK4P
RADIO2_33
RADIO2_34
RADIO2_35
RADIO2_36
RADIO2_37
RADIO2_38
RADIO2_39
RADIO2_40
RADIO2_41
RADIO2_42
RADIO2_43
RADIO2_44
RADIO2_45
RADIO2_46
RADIO2_47
RADIO2_48
RADIO2_49
RADIO2_50
RADIO2_51
RADIO2_52
RADIO2_53
RADIO2_54
RADIO2_55
RADIO2_56
RADIO2_57
RADIO2_58
RADIO2_59
RADIO2_60
RADIO2_61
RADIO2_62
RADIO2_63
RADIO2_64
RADIO2_65
RADIO2_66
RADIO2_67
RADIO2_68
RADIO2_69
RADIO2_70
RADIO2_71
RADIO2_72
RADIO2_73
RADIO2_74
RADIO2_75
RADIO2_76
RADIO2_77
RADIO2_78
RADIO2_79
RADIO2_80
RADIO2_81
RADIO2_82
RADIO2_83
RADIO2_84
RADIO2_85
RADIO2_86
RADIO2_87
RADIO2_88
RADIO2_89
RADIO2_90
RADIO2_91
RADIO2_92
RADIO2_93
RADIO2_94
RADIO2_95
RADIO2_96
RADIO2_97
RADIO2_98
RADIO2_99
RADIO2_100
RADIO2_101
RADIO2_102
RADIO2_103
RADIO2_104
RADIO2_105
RADIO2_106
RADIO2_107
RADIO2_108
RADIO2_109
RADIO2_110
RADIO2_111
RADIO2_112
RADIO2_113
RADIO2_114
RADIO2_115
RADIO2_116
RADIO2_117
RADIO2_118
RADIO2_119
RADIO2_120
RADIO2_121
RADIO2_122
RADIO2_123
5 FPGA_GCLK4P
FPGA_GCLK4P
Daughtercard Slot #3
RADIO2_32
RADIO3_42
J31
MHOLE
J32
MHOLE
DGND
DVDD_-5v
DVDD_5v
DVDD_5v
DVDD_-5v
RADIO3_[0:123] 6,9
J28
CONN160
DGND
DGND
RADIO3_0
RADIO3_1
RADIO3_2
RADIO3_3
RADIO3_4
RADIO3_5
RADIO3_6
RADIO3_7
RADIO3_8
RADIO3_9
RADIO3_10
RADIO3_11
RADIO3_43
RADIO3_12
RADIO3_13
RADIO3_14
RADIO3_15
RADIO3_16
RADIO3_17
RADIO3_18
RADIO3_19
RADIO3_20
RADIO3_21
RADIO3_22
RADIO3_23
RADIO3_24
RADIO3_25
RADIO3_26
RADIO3_27
RADIO3_28
RADIO3_29
RADIO3_30
RADIO3_31
RADIO3_32
RADIO3_33
RADIO3_34
RADIO3_35
RADIO3_36
RADIO3_37
RADIO3_38
RADIO3_39
RADIO3_40
RADIO3_41
FPGA_GCLK7P
RADIO3_44
RADIO3_45
RADIO3_46
RADIO3_47
RADIO3_48
RADIO3_49
RADIO3_50
RADIO3_51
RADIO3_52
RADIO3_53
RADIO3_54
RADIO3_55
RADIO3_56
RADIO3_57
RADIO3_58
RADIO3_59
RADIO3_60
RADIO3_61
RADIO3_62
RADIO3_63
RADIO3_64
RADIO3_65
RADIO3_66
RADIO3_67
RADIO3_68
RADIO3_69
RADIO3_70
RADIO3_71
RADIO3_72
RADIO3_73
RADIO3_74
RADIO3_75
RADIO3_76
RADIO3_77
RADIO3_78
RADIO3_79
RADIO3_80
RADIO3_81
RADIO3_82
RADIO3_83
RADIO3_84
RADIO3_85
RADIO3_86
RADIO3_87
RADIO3_88
RADIO3_89
RADIO3_90
RADIO3_91
RADIO3_92
RADIO3_93
RADIO3_94
RADIO3_95
RADIO3_96
RADIO3_97
RADIO3_98
RADIO3_99
RADIO3_100
RADIO3_101
RADIO3_102
RADIO3_103
RADIO3_104
RADIO3_105
RADIO3_106
RADIO3_107
RADIO3_108
RADIO3_109
RADIO3_110
RADIO3_111
RADIO3_112
RADIO3_113
RADIO3_114
RADIO3_115
RADIO3_116
RADIO3_117
RADIO3_118
RADIO3_119
RADIO3_120
RADIO3_121
RADIO3_122
RADIO3_123
3 FPGA_GCLK7P
FPGA_GCLK7P
Daughtercard Slot #4
Rice University
Title
WARP FPGA Board
Description
Daughtercard Headers 2-3
Rev
1.2
Date: Saturday, June 17, 2006
Sheet 12 of 17



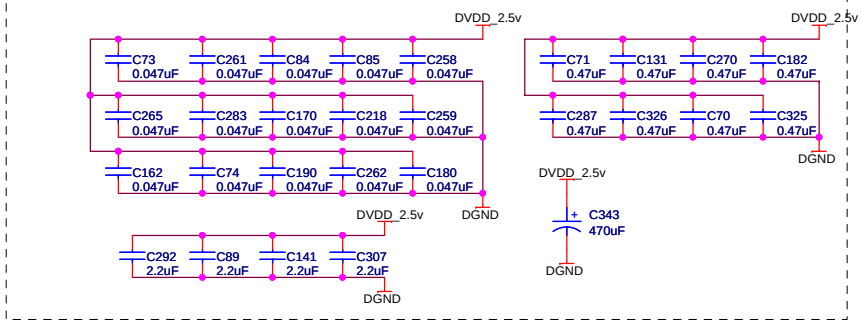
Rice University	
Title: WARP FPGA Board	
Description: SRAMs	Rev: 1.2
Date: Saturday, June 17, 2006	Sheet 13 of 17


DVDD_3.3v
J47
U16
Compact Flash Socket
XCCACE_TQ144
DGND
SW2
SW DIP-4
SW1
D5 LED_RED
D4 LED_GREEN
J49
CONN14_XILINX_P4
SYSACE_CFG_INIT# 7
SYSACE_CFG_PROG# 7
FPGA_TCK 7
FPGA_TDO 7
FPGA_TDI 7
FGPA_TMS 7
TDI/TDO cross over here.
The FPGA is only device
on this JTAG chain.
In case SyasceCF isn't
mounted, mount these
resistors to connect FPGA
directly to JTAG cable
SYSACE_RESET#
SYSACE_CLK33 2
Rice University
WARP FPGA Board
SystemACE CF (FPGA Configuration)
Rev 1.2
Date: Saturday, June 17, 2006
Sheet 14 of 17

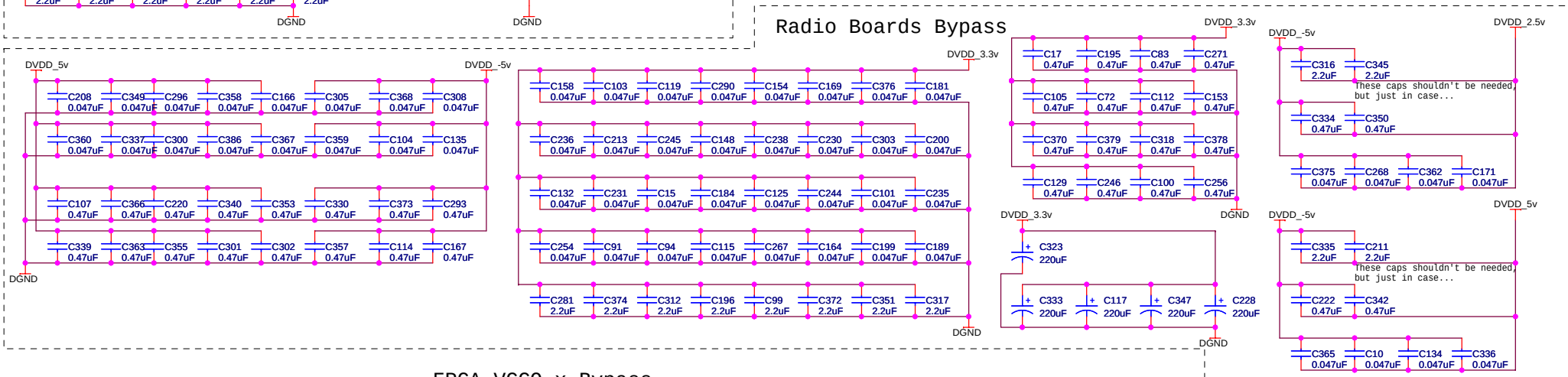
FPGA VCC_INT Bypass (56 power pins)



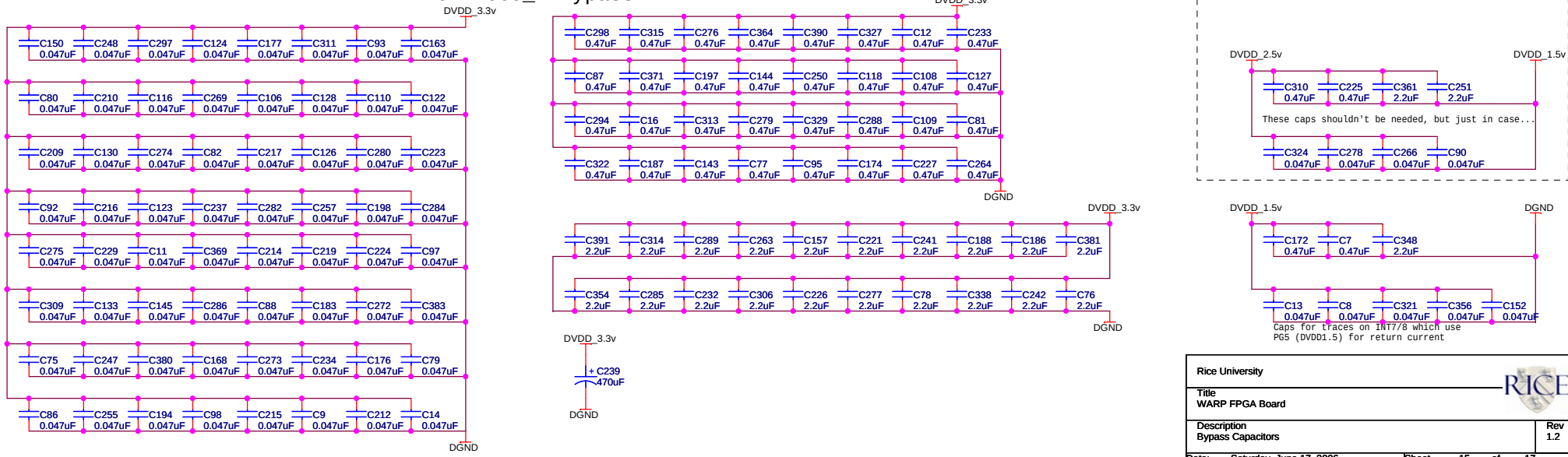
FPGA VCC_AUX Bypass (28 power pins)



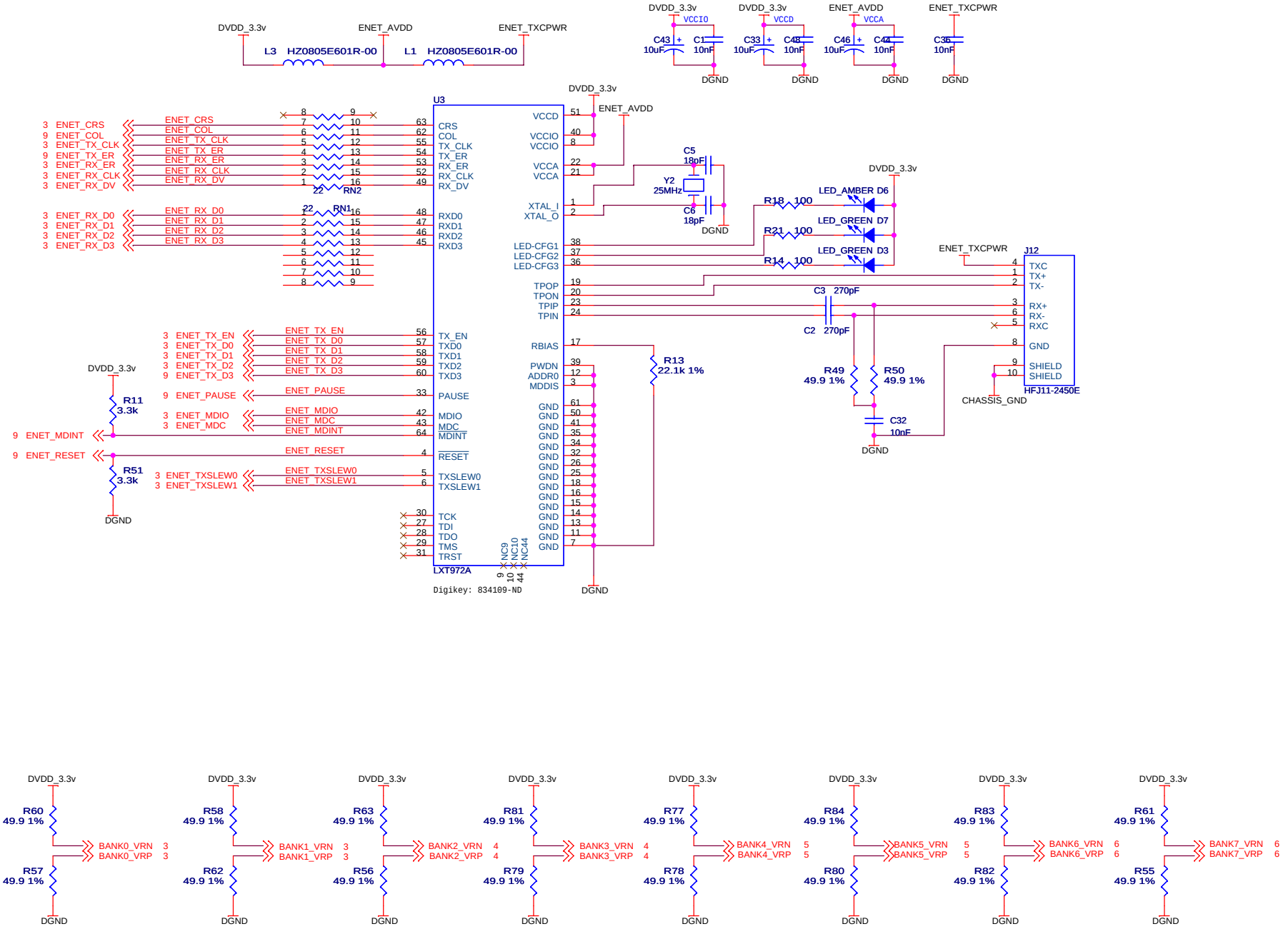
Radio Boards Bypass



FPGA VCCO_x Bypass



Rice University	
Title: WARP FPGA Board	
Description: Bypass Capacitors	Rev: 1.2
Date: Saturday, June 17, 2006	Sheet 15 of 17



Digitally Controlled Impedance Reference Resistors
Every I/O bank has option of 50-ohm DCI

When using DCI, the Bitgen option "DCI Update Mode"
should *not* be set to Quiet. If it is, some I/O will not
function properly. See pg. 235 of the Virtex-II Pro
User's Guide (DCI section of ug012.pdf) for more information

Rice University	
Title: WARP FPGA Board	
Description: 10/100 Ethernet PHY and DCI Resistors	Rev: 1.2
Date: Saturday, June 17, 2006	Sheet 16 of 17