# A High Throughput Beamforming Architecture for MIMO Systems

*Melissa Duarte, Ashutosh Sabharwal (mduarte, ashu)@rice.edu,*
*Raghu Rao, and Chris Dick (rrao, chrisd)@xilinx.com*

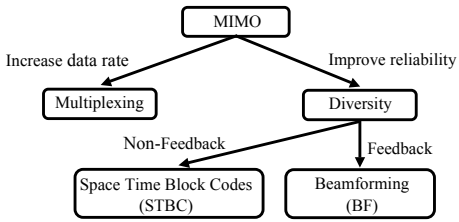
Center for Multimedia Communication

RICE

## Goal

Efficient implementation of a real-time beamforming MIMO system.

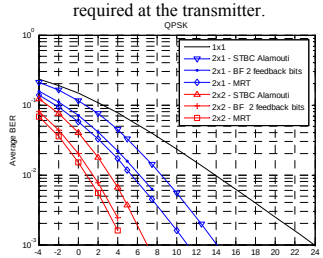
## Background




## Motivation – Why consider a feedback scheme?

Beamforming has better performance than Space Time Block Codes.

The cost of this better performance is channel state information required at the transmitter.




## Contribution

Design of a codebook that allows an efficient implementation of the channel quantizer.

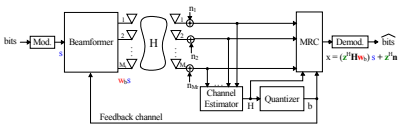
Compared to a straightforward implementation of the channel quantizer, the proposed implementation increases the number of channels quantized per FPGA unit area.

Simulation results show that standards-based systems can benefit from the proposed channel quantizer implementation.

## Future work

Integrate beamforming into Rice and Xilinx MIMO OFDM testbeds and characterize over real wireless channels.

## System model




**s**: Complex transmitted symbol
$\mathbf{w}_b$: Beamforming vector, $\|\mathbf{w}_b\|_2 = 1, \quad 1 \le b \le N$
N: Cardinality of codebook, $N=2^B$
H: Channel matrix, $M_r$ x $M_t$
**z**: Combining vector, $\|\mathbf{z}\|_2 = 1$
**x**: Input to demodulator
B: Number of feedback bits

To maximize SNR choose

$\mathbf{z} = \mathbf{H}\mathbf{w}_b / \|\mathbf{H}\mathbf{w}_b\|_2$ and $b = \arg\max_{1 \le i \le N} (\|\mathbf{H}\mathbf{w}_i\|_2)^2$

## Computational requirements of Quantizer

The Quantizer block runs an exhaustive search to find b.
To compute $\mathbf{H}\mathbf{w}_i$ for all N codewords we need to perform
$\mathbf{4NM_rM_t}$ multiplications

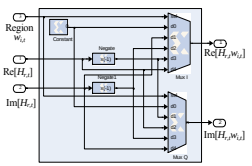
$$\mathbf{H} = \begin{bmatrix} H_{1,1} & H_{1,2} & \dots & H_{1,M_t} \\ H_{2,1} & H_{2,2} & \dots & H_{2,M_t} \\ \vdots & \vdots & \vdots & \vdots \\ H_{M_r,1} & H_{M_r,2} & \dots & H_{M_r,M_t} \end{bmatrix} \qquad \mathbf{w}_i = \begin{bmatrix} w_{1,i} \\ w_{2,i} \\ \vdots \\ w_{M_t,i} \end{bmatrix}$$

$$H_{r,t}w_{i,t} = \mathrm{Re}[H_{r,t}]\mathrm{Re}[w_{i,t}] - \mathrm{Im}[H_{r,t}]\mathrm{Im}[w_{i,t}] + j\left(\mathrm{Re}[H_{r,t}]\mathrm{Im}[w_{i,t}] + \mathrm{Im}[H_{r,t}]\mathrm{Re}[w_{i,t}]\right)$$

## Reducing the number of multiplications

If $w_{i,t} \in \{0, -j, j, -1, 1\}$ then to compute $\mathbf{H}\mathbf{w}_i$ for all N codewords we need $\mathbf{2NM_rM_t}$ multiplexers, instead of $\mathbf{4NM_rM_t}$ multipliers

| Possibilities for $w_{i,t}$ | Region $w_{i,t}$ |
|---|---|
| 0 + 0j | 0 |
| 0 - 1j | 1 |
| 0 + 1j | 2 |
| -1 + 0j | 3 |
| 1 + 0j | 4 |




## New approach

Use a new version of the codebook, labeled Mapped Codebook, in which

$w_{i,t} \in \{0, -j, j, -1, 1\}$

## Mapping of the codebook

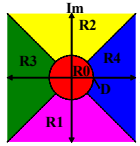
Start with the original codebook

$M_t$ transmitter antennas

N codewords

$$\begin{bmatrix} w_{1,1} & w_{1,2} & \dots & w_{1,M_t} \\ w_{2,1} & w_{2,2} & \dots & w_{2,M_t} \\ \vdots & \vdots & \vdots & \vdots \\ w_{N,1} & w_{N,2} & \dots & w_{N,M_t} \end{bmatrix} \quad w_{i,t} \in C$$

Use the following mapping regions




| | |
|---|---|
| R 0 | 0 + 0j |
| R 1 | 0 - 1j |
| R 2 | 0 + 1j |
| R 3 | - 1 + 0j |
| R 4 | 1 + 0j |

D = 1 / ( 2 sqrt( $M_t$ ) )

Obtain a Mapped Codebook

$M_t$ transmitter antennas

N codewords

$$\begin{bmatrix} w_{1,1} & w_{1,2} & \dots & w_{1,M_t} \\ w_{2,1} & w_{2,2} & \dots & w_{2,M_t} \\ \vdots & \vdots & \vdots & \vdots \\ w_{N,1} & w_{N,2} & \dots & w_{N,M_t} \end{bmatrix} \quad w_{i,t} \in \{0, -j, j, -1, 1\}$$

Normalizing gain.

$$\begin{bmatrix} ng_1 \\ ng_2 \\ \vdots \\ ng_N \end{bmatrix} \quad ng_i \in R$$

## Increase in Throughput

- Assume that for the implementation of one multiplexer the area needed in the FPGA is the same as for the implementation of one multiplier
- Using the Mapped Codebook increases the number of channels quantized per FPGA unit area by a factor equal to **β**

$$\beta = \frac{\textbf{Multipliers (Original Codebook)}}{\textbf{Multipliers (Mapped Codebook)} + \textbf{Multiplexers (Mapped Codebook)}}$$

## Resource estimate for 802.16e

Compute the number of multipliers and multiplexers required for $N = 2^3$, $M_t = M_r = 4$, $FPGA_{clk} = 100MHz$, $T_{OFDM} = 100.8\mu s$

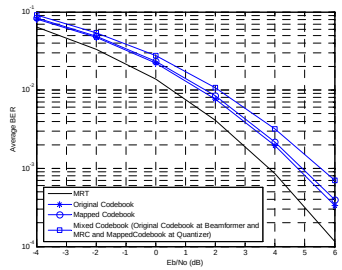
$T_{OFMD}$: Duration of an OFDM symbol
K: Number of subcarriers
Time constraint: K channels must be quantized in a time $\le T_{OFDM}$

| | | K = 128 1.25MHz Bw | K = 512 5MHz Bw | K = 1024 10Mhz Bw | K = 2048 20Mhz Bw |
|---|---|---|---|---|---|
| Original Codebook | Total Multipliers Quantizer | 8 | 31 | 60 | 119 |
| | Total Multiplexers Quantizer | 0 | 0 | 0 | 0 |
| Mapped Codebook | Total Multipliers Quantizer | 2 | 5 | 8 | 16 |
| | Total Multiplexers Quantizer | 4 | 14 | 27 | 53 |
| **β** | | 1.33 | 1.63 | 1.71 | 1.72 |

Using the Mapped Codebook increases the number of channels quantized per FPGA unit area by a factor equal to **β**

## Simulation results using Mapped Codebook

Beamforming 3x3 MIMO – 3 Feedback bits – 16QAM
802.16e Codebook




Mixed Codebook scheme: Integration of proposed high throughput architecture in a standards-based system