

WARP: Hardware

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WARP Workshop
Nile University
April 16, 2008



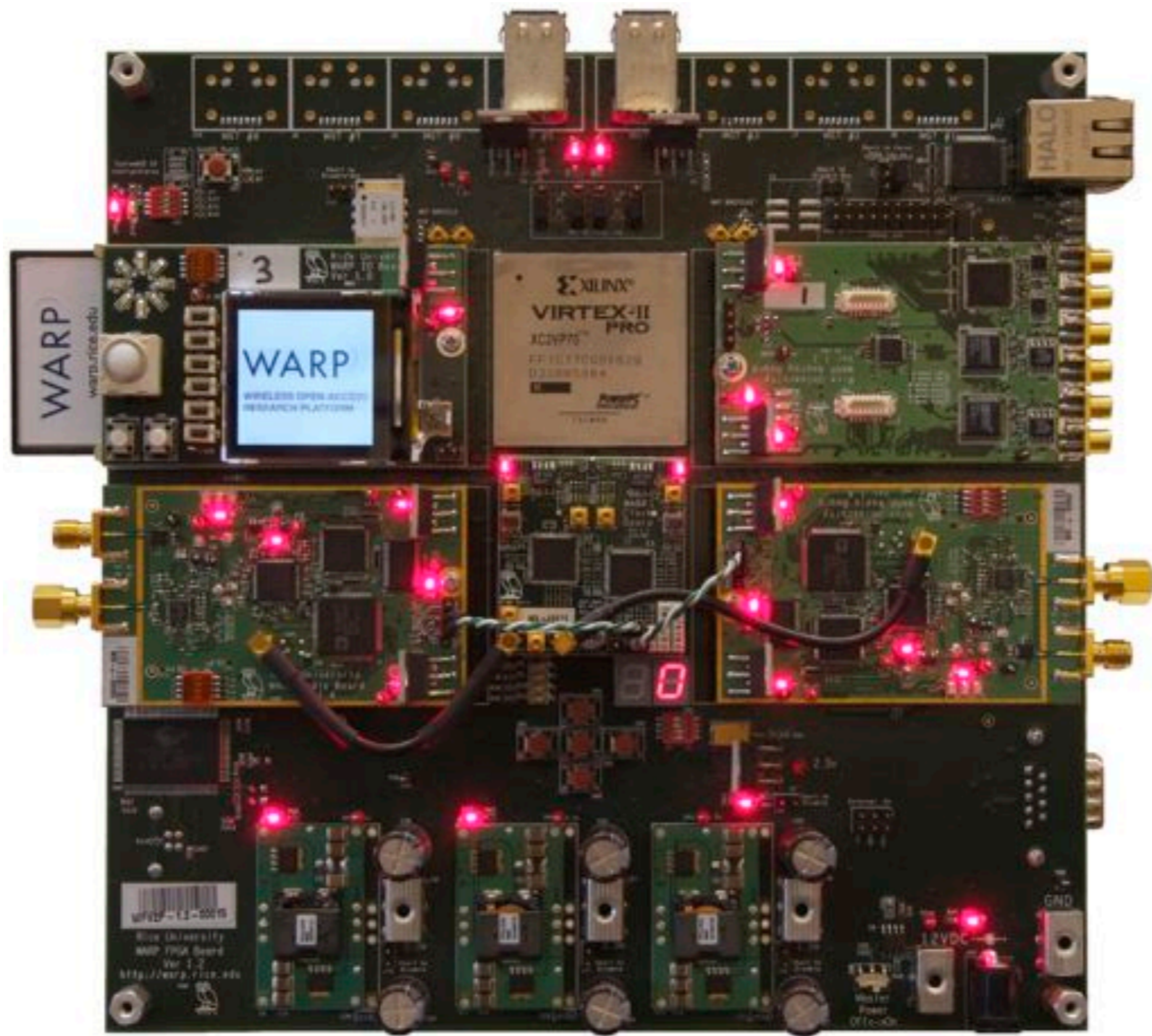
warp.rice.edu

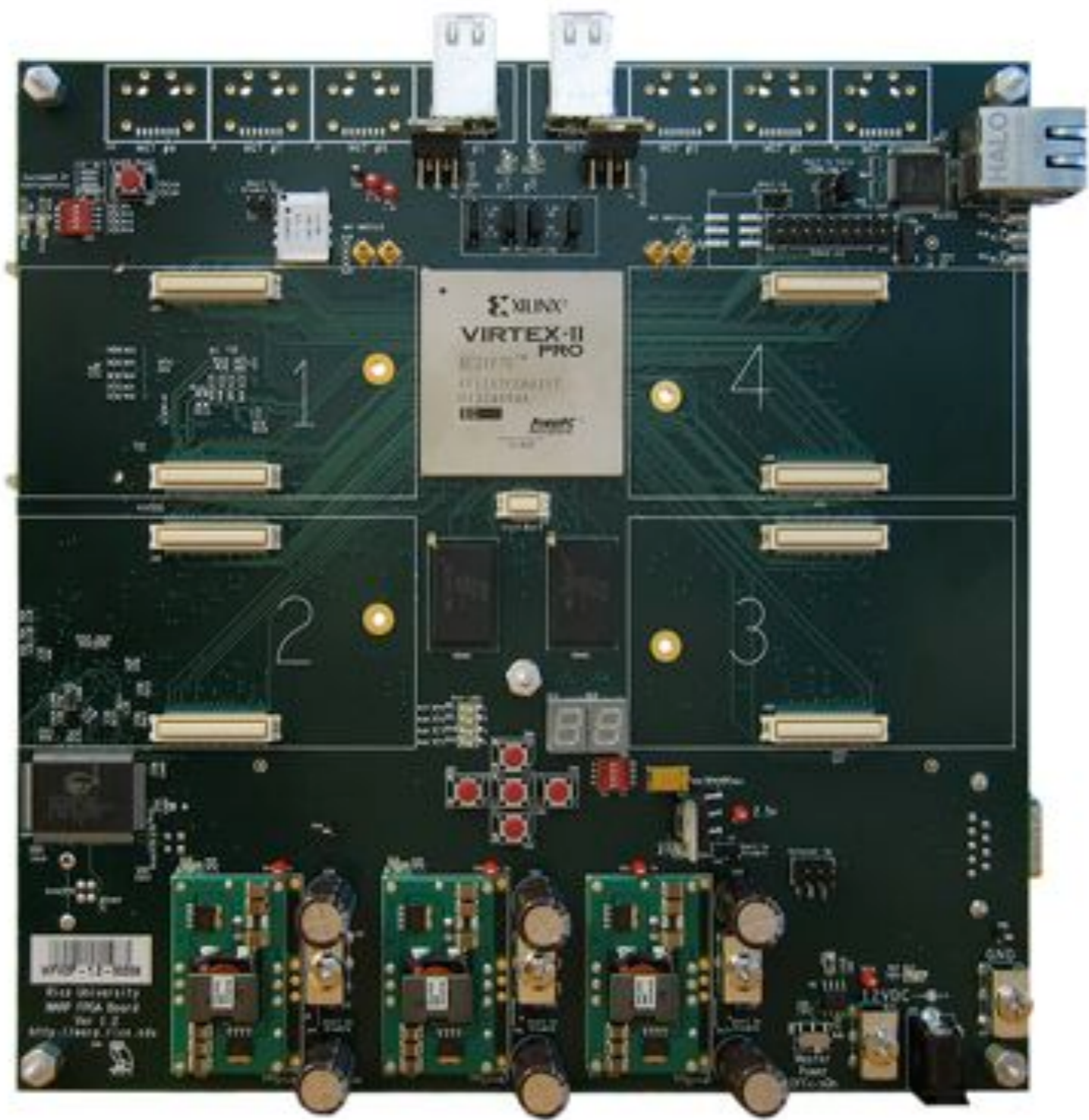


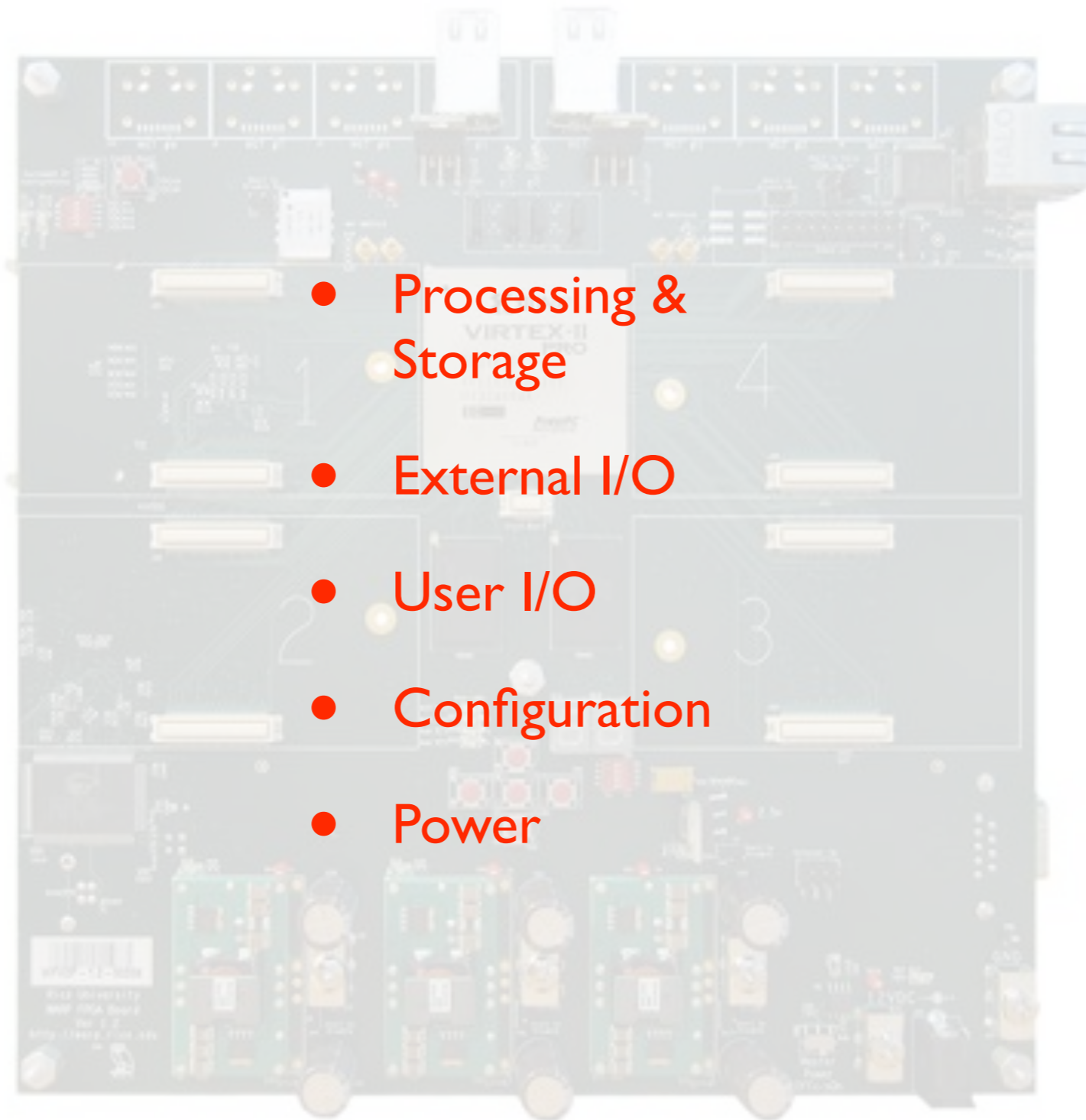
Questions From Yesterday?

WARP Hardware

- WARP Hardware Components
 - FPGA Board
 - Radio Board
 - Clock Board
- FPGA Architecture
- WARP Design Flows







- Processing & Storage

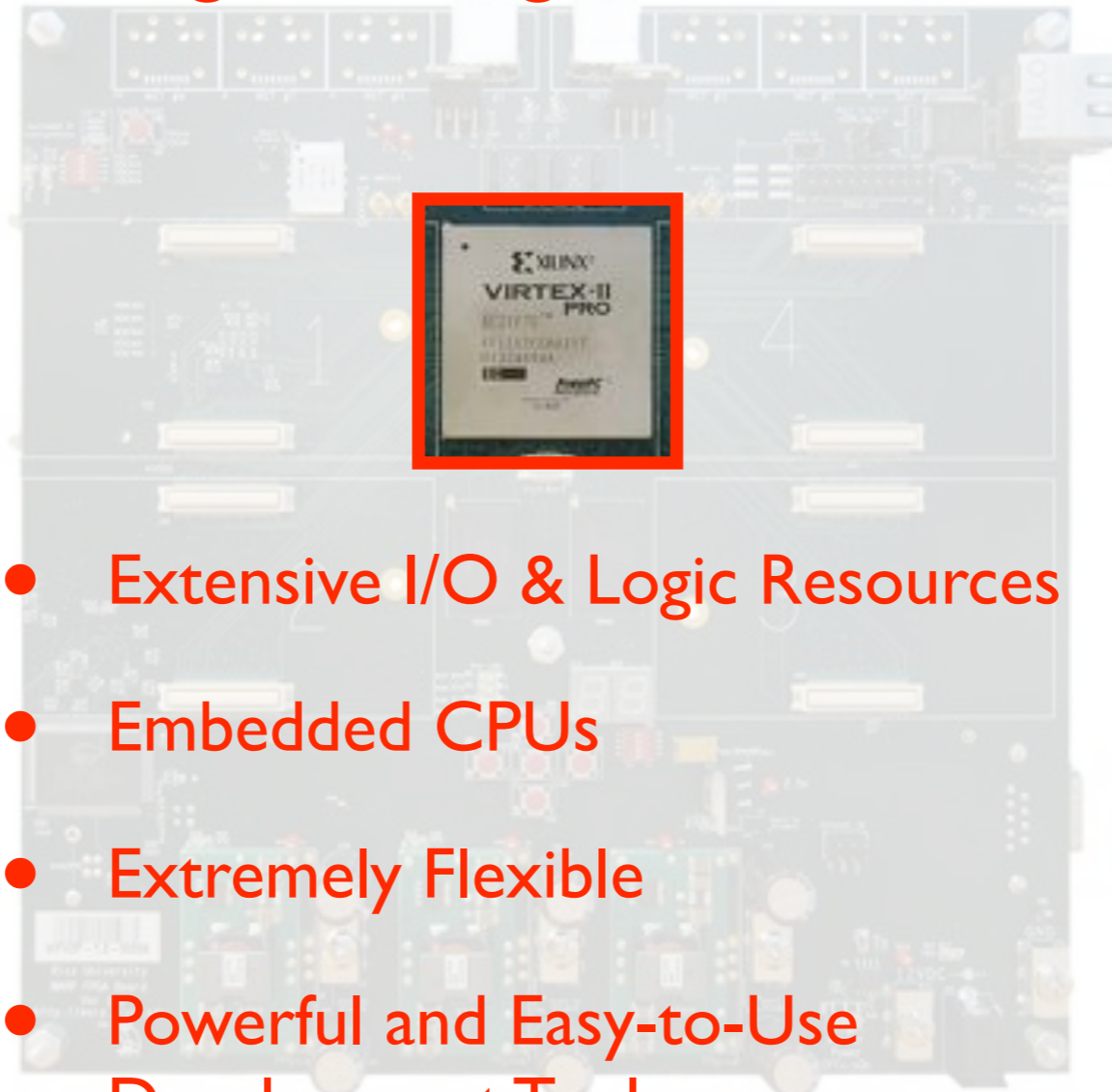
- External I/O

- User I/O

- Configuration

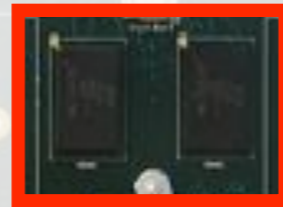
- Power

Processing & Storage : XC2VP70 FPGA

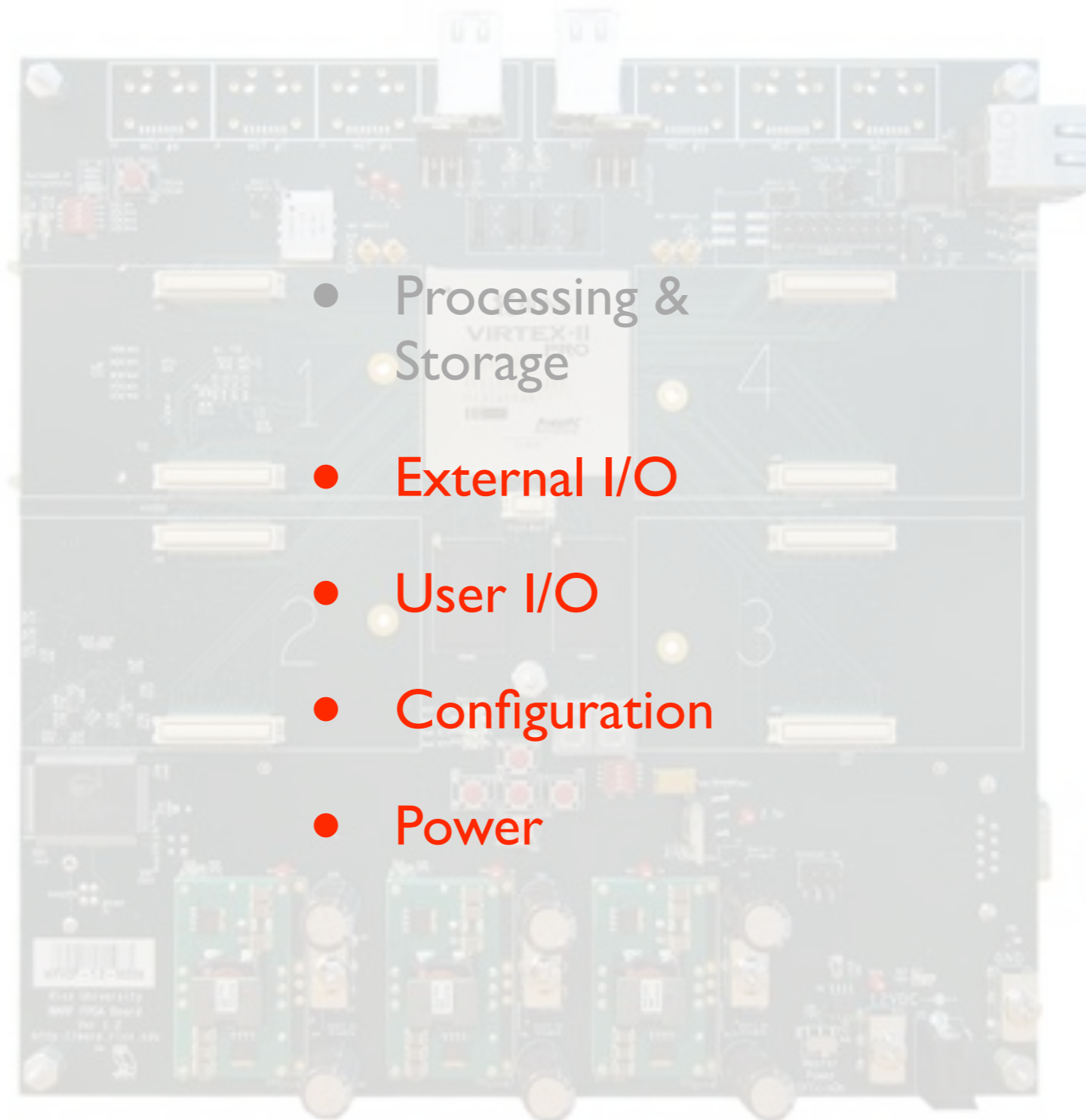


- Extensive I/O & Logic Resources
- Embedded CPUs
- Extremely Flexible
- Powerful and Easy-to-Use Development Tools

Processing & Storage : 4 MByte Onboard SRAM



- Augments FPGA's Internal RAM Resources
- Usable as Instruction and/or Data Memory
- Two ICs, Each 512K x 32



- Processing & Storage

- External I/O

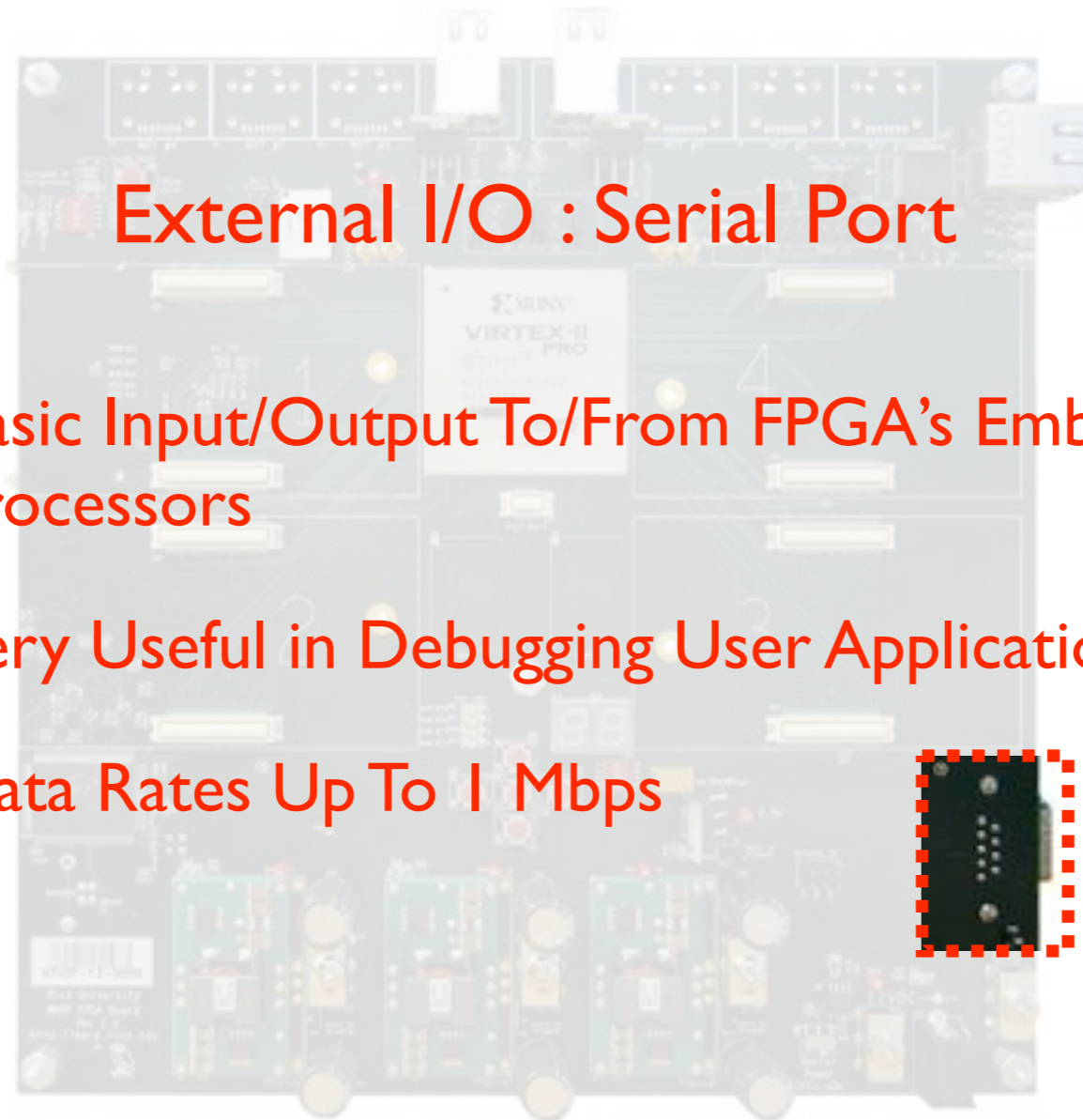
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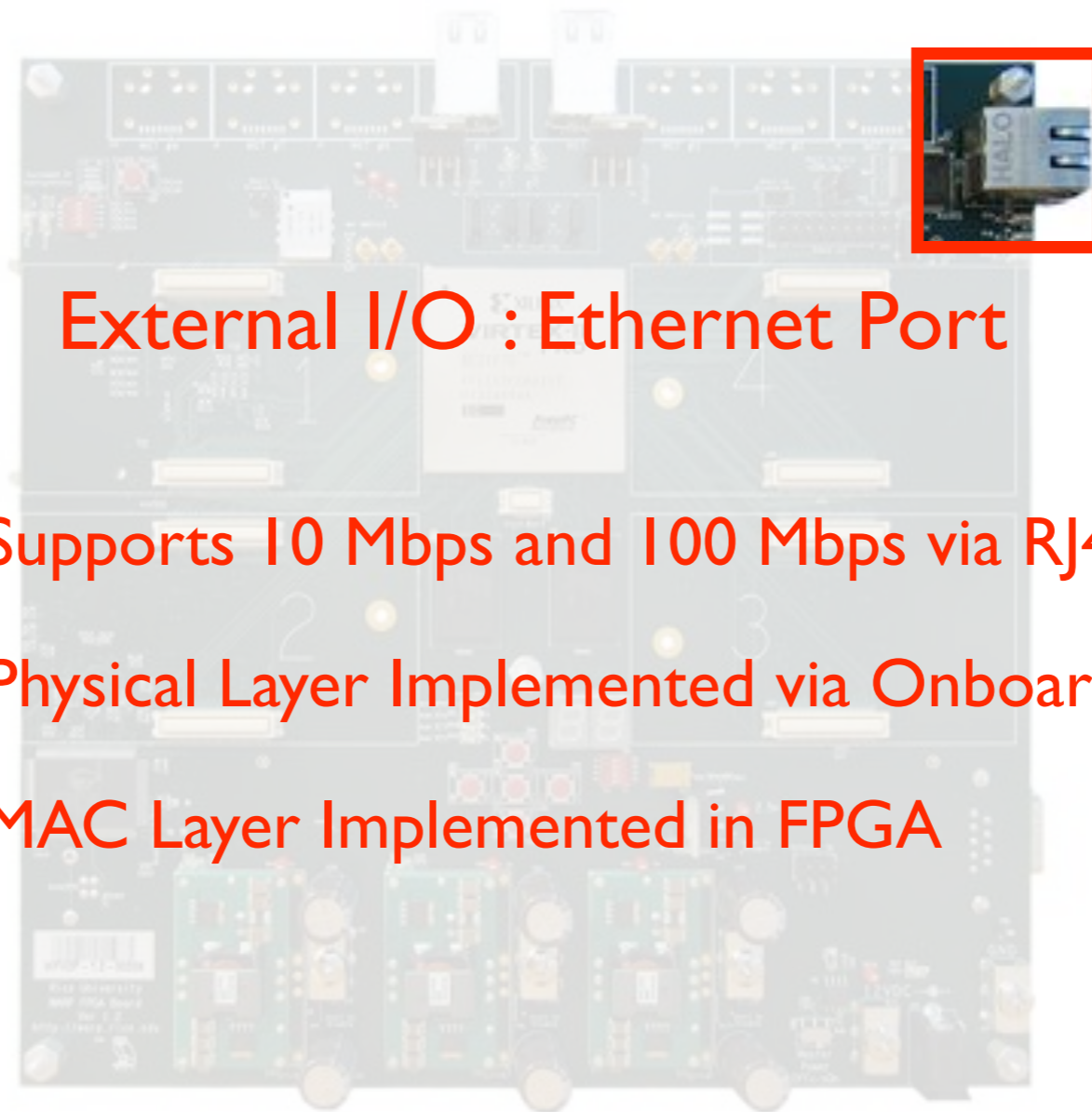
- Configuration

- Power

External I/O : Serial Port

- Basic Input/Output To/From FPGA's Embedded Processors
- Very Useful in Debugging User Applications
- Data Rates Up To 1 Mbps





External I/O : Ethernet Port

- Supports 10 Mbps and 100 Mbps via RJ45
- Physical Layer Implemented via Onboard IC
- MAC Layer Implemented in FPGA



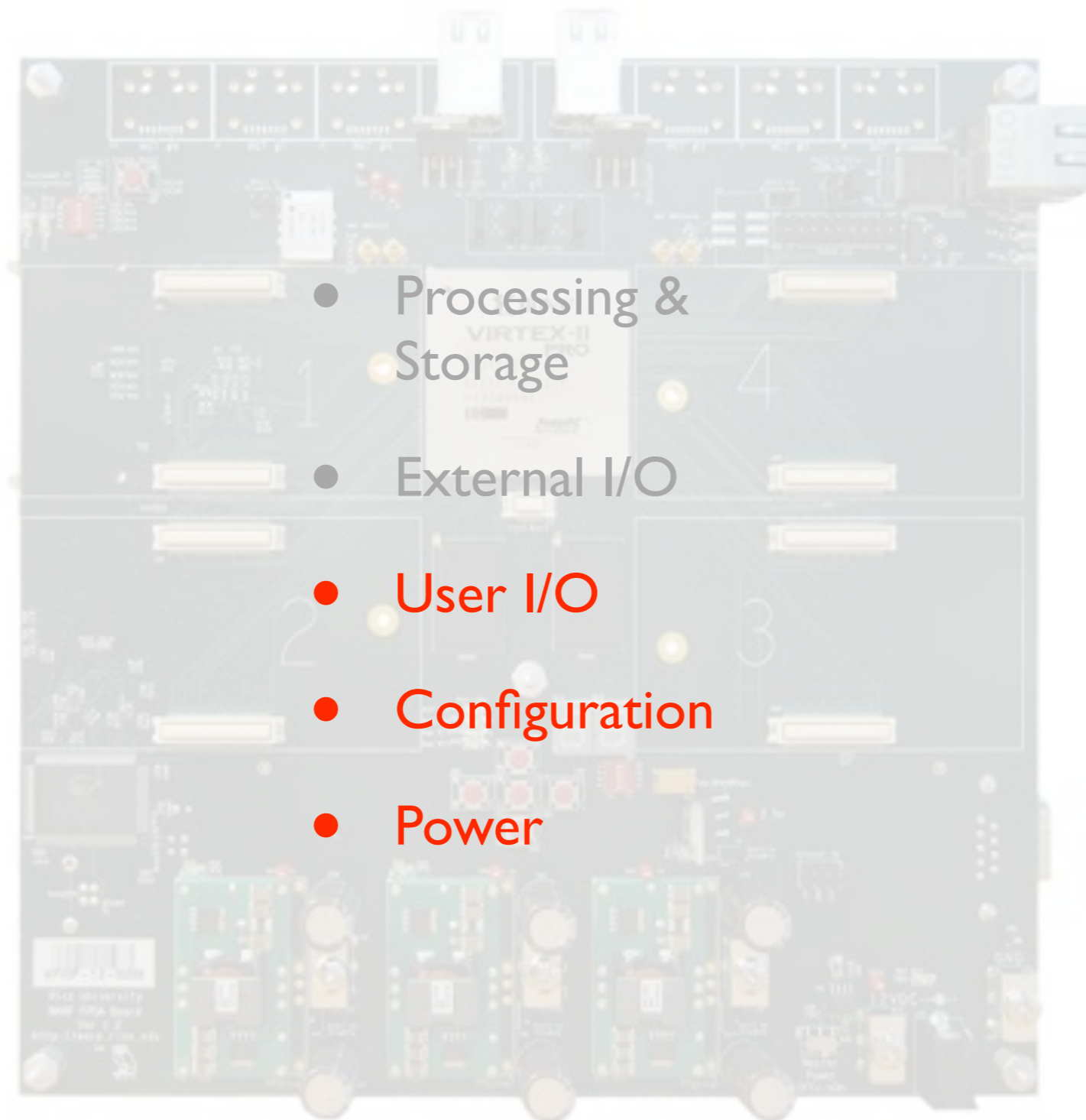
External I/O : Multi-Gigabit Transceivers

- High Performance Serial Links (3.125 Gbps Full Duplex)
- Inter-Board Communication for Multi-FPGA Processing

External I/O : Daughtercard Connectors



- Provide Expanded Functionality via Custom Daughtercards
- Connect to FPGA Through General Purpose Digital I/Os
- Protocol Defined By Logic and Software Residing in FPGA
- Supports Radios, Video Cards, A/D & D/A Cards, Others



- Processing & Storage

- External I/O

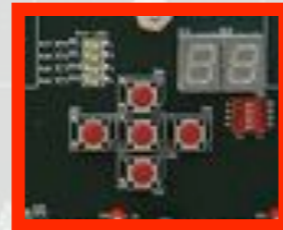
- User I/O

- Configuration

- Power

User I/O : Switches, Buttons, LEDs

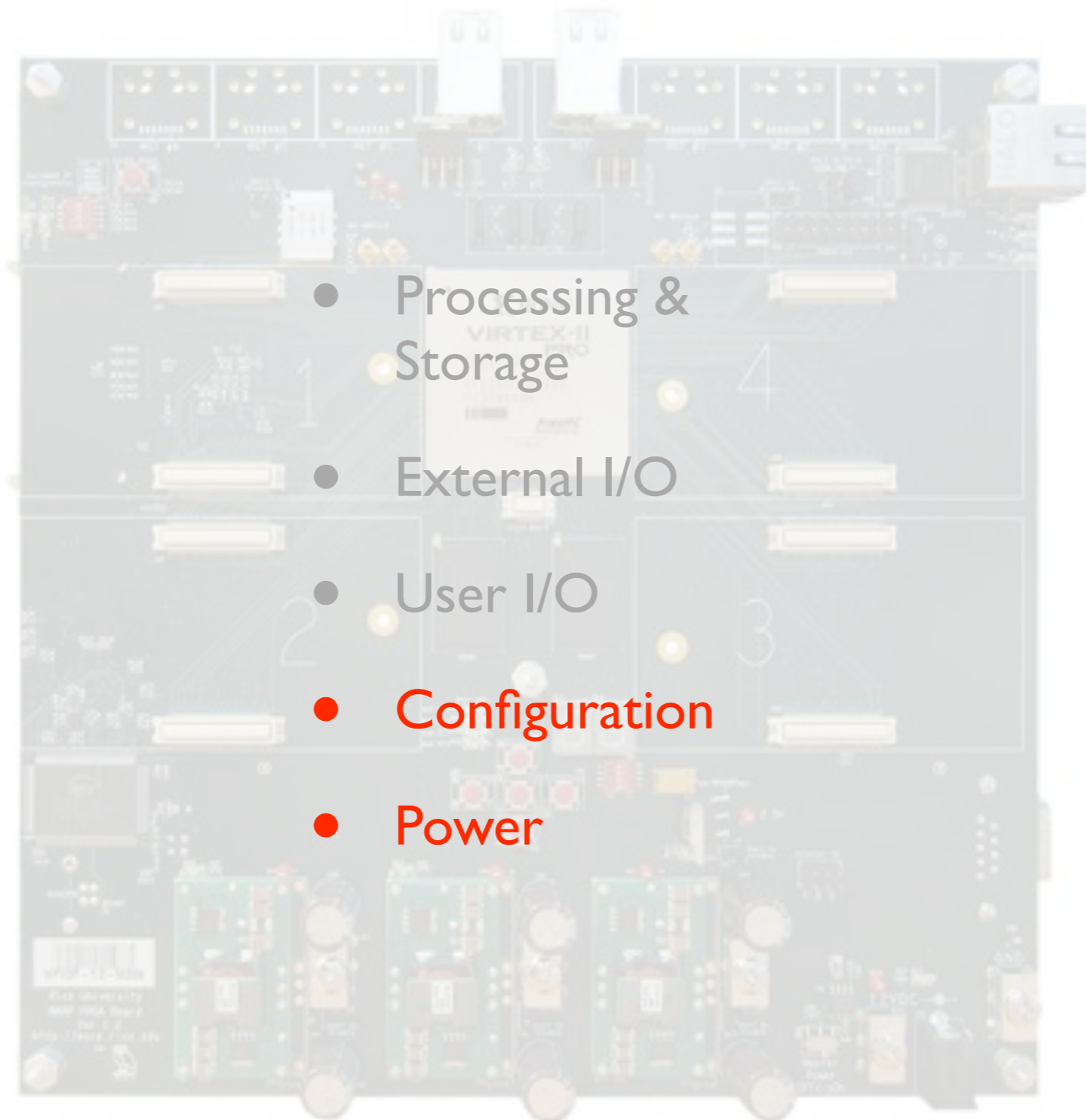
- Discrete and 7-Segment LEDs Provide Visible Status
- Buttons and Switches Provide Mechanism for User Input





User I/O : Generic 20-Pin Header

- Direct Connection to 16 FPGA Pins and 4 Ground Signals
- Allows FPGA Signals to be Driven Off-Board
- Enables Viewing of Critical Signals During Low-Level Debugging



- Processing & Storage

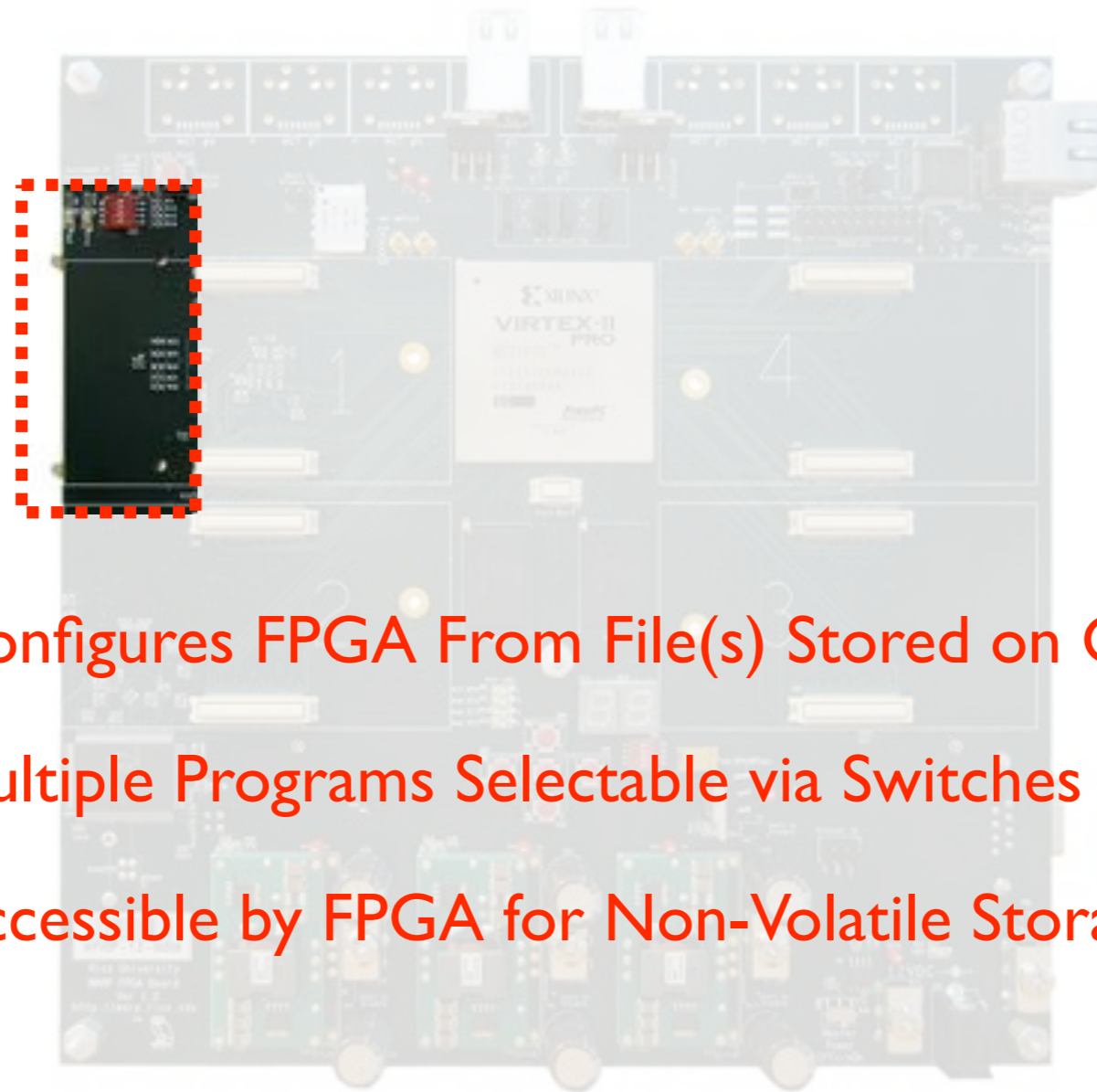
- External I/O

- User I/O

- Configuration

- Power

Configuration : Compact Flash Slot



- Configures FPGA From File(s) Stored on CF Card
- Multiple Programs Selectable via Switches on PCB
- Accessible by FPGA for Non-Volatile Storage

Configuration : JTAG Header

- Connects to Xilinx Parallel IV or Platform USB Configuration Cables
- Used to Configure FPGA From PC During Development

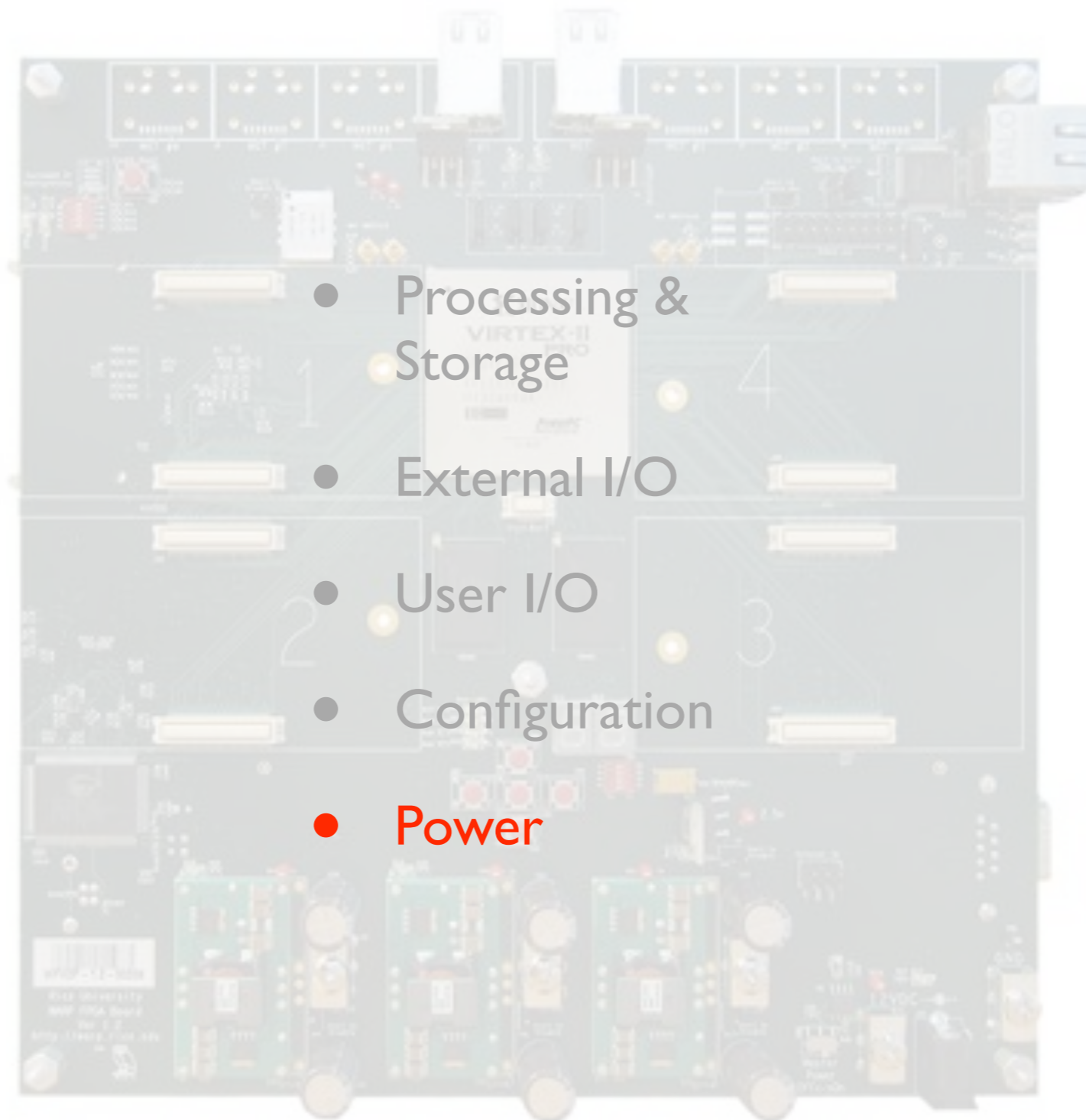


- Provides Interface for Debugging Tools (e.g. ChipScope)
- Supports Industry-Standard Boundary Scan Testing

Configuration : USB Connector

- Allows Direct Connection to PC via Standard USB Cable
- Emulates Functionality of Xilinx Platform USB Cable
- Eliminates the Need for Dedicated Configuration Cables





- Processing & Storage

- External I/O

- User I/O

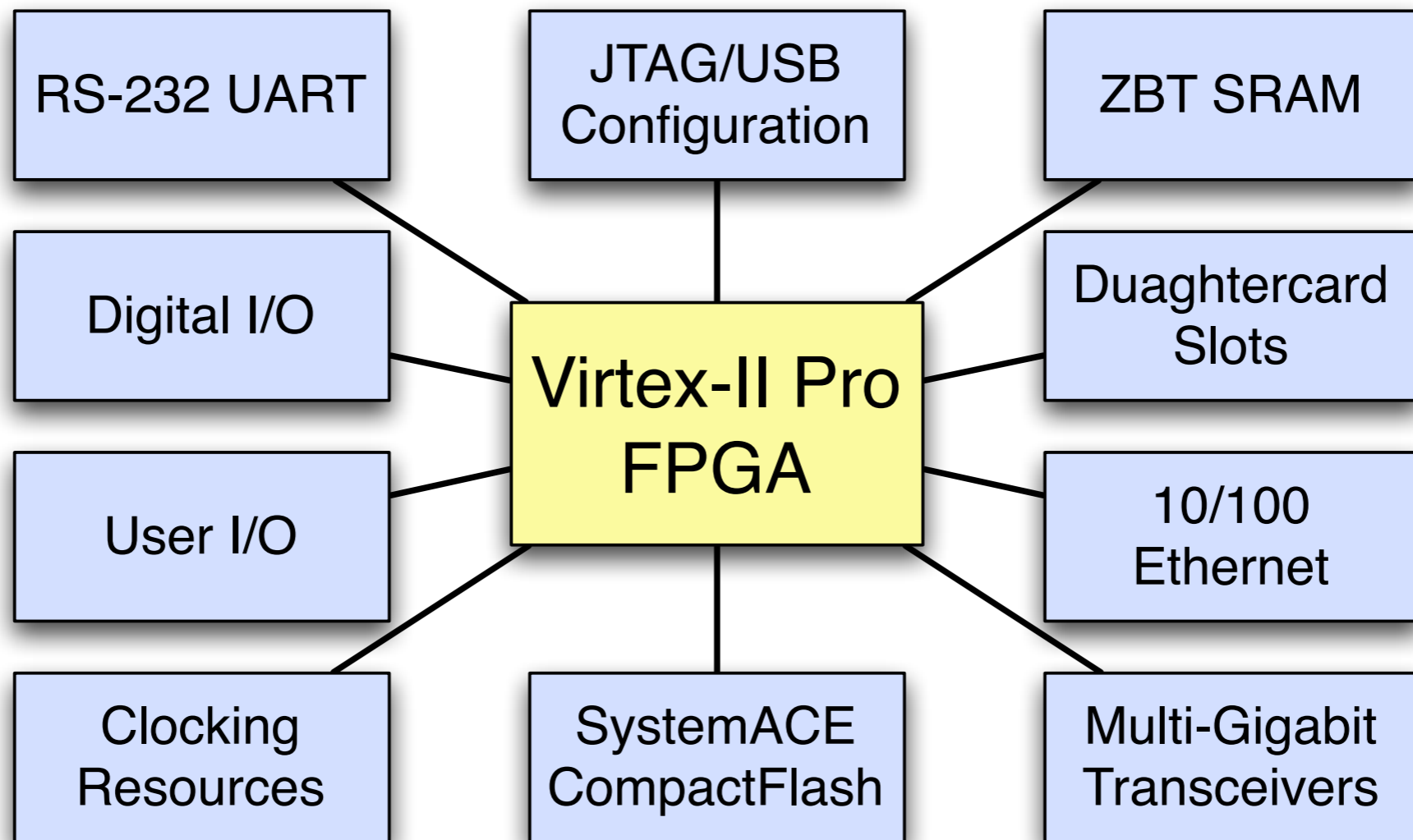
- Configuration

- **Power**

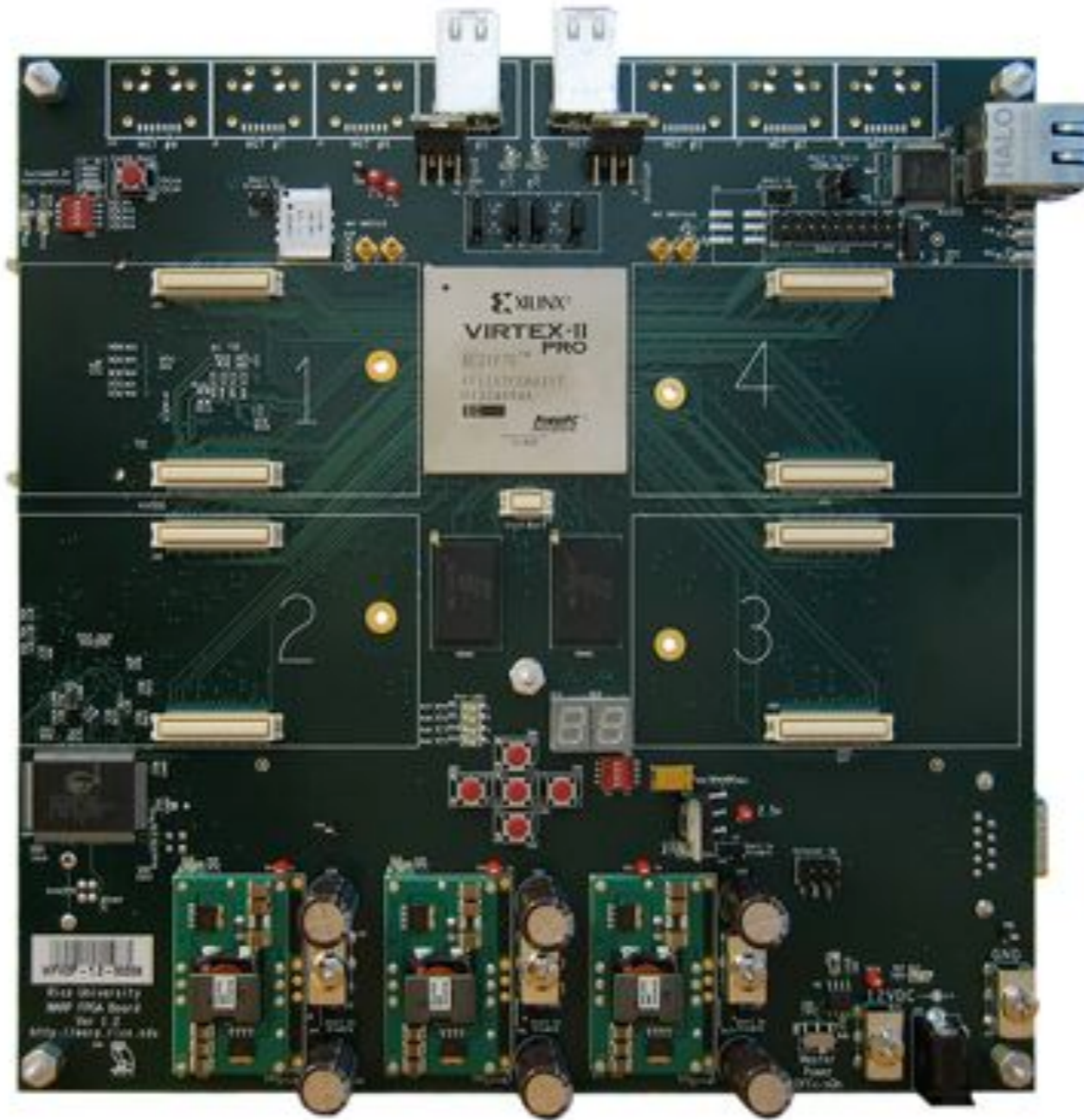


Power : 12V DC Voltage Input

- User Supplies a Single External Voltage Supply
- All Other Required Voltages are Derived on PCB

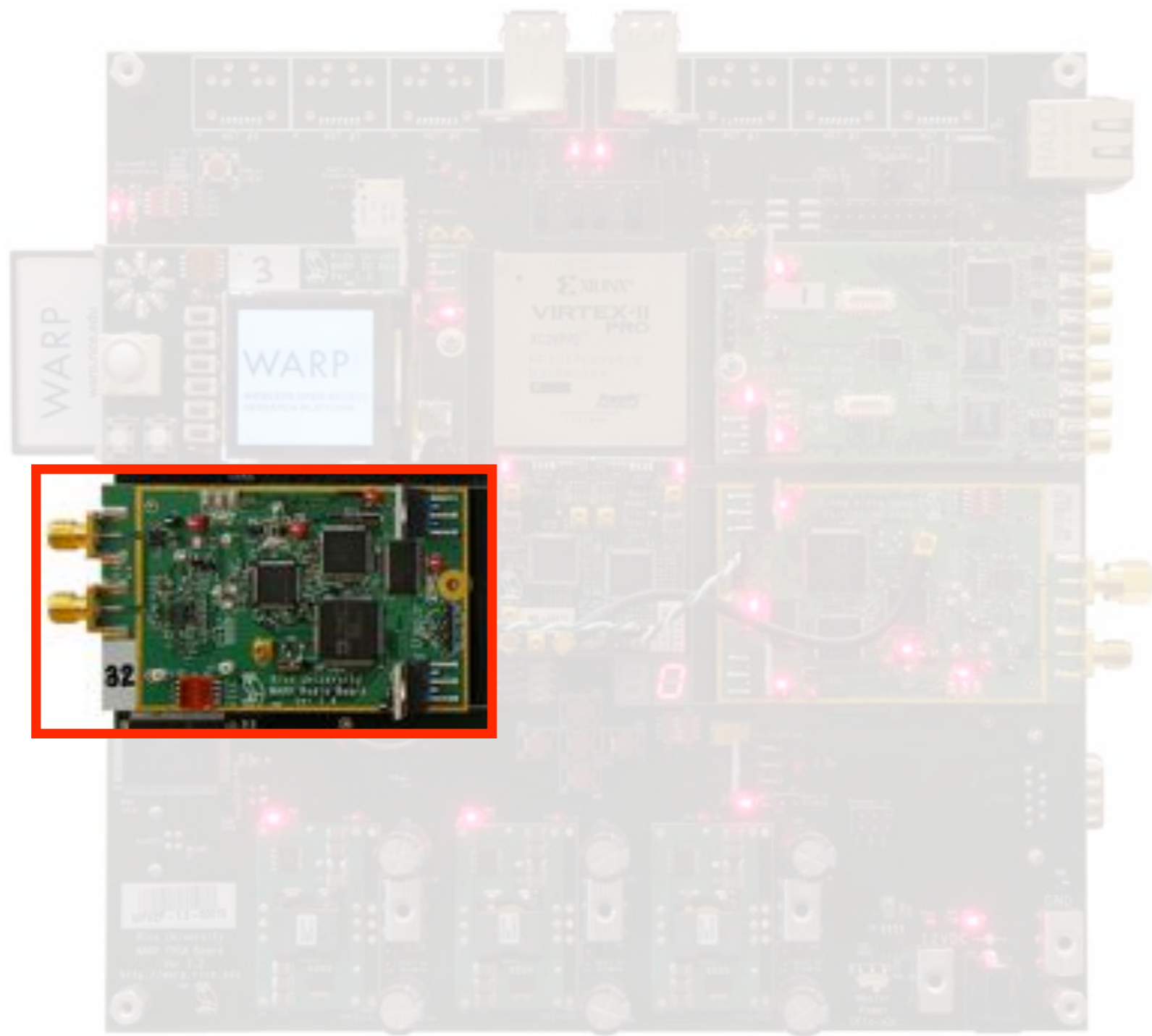


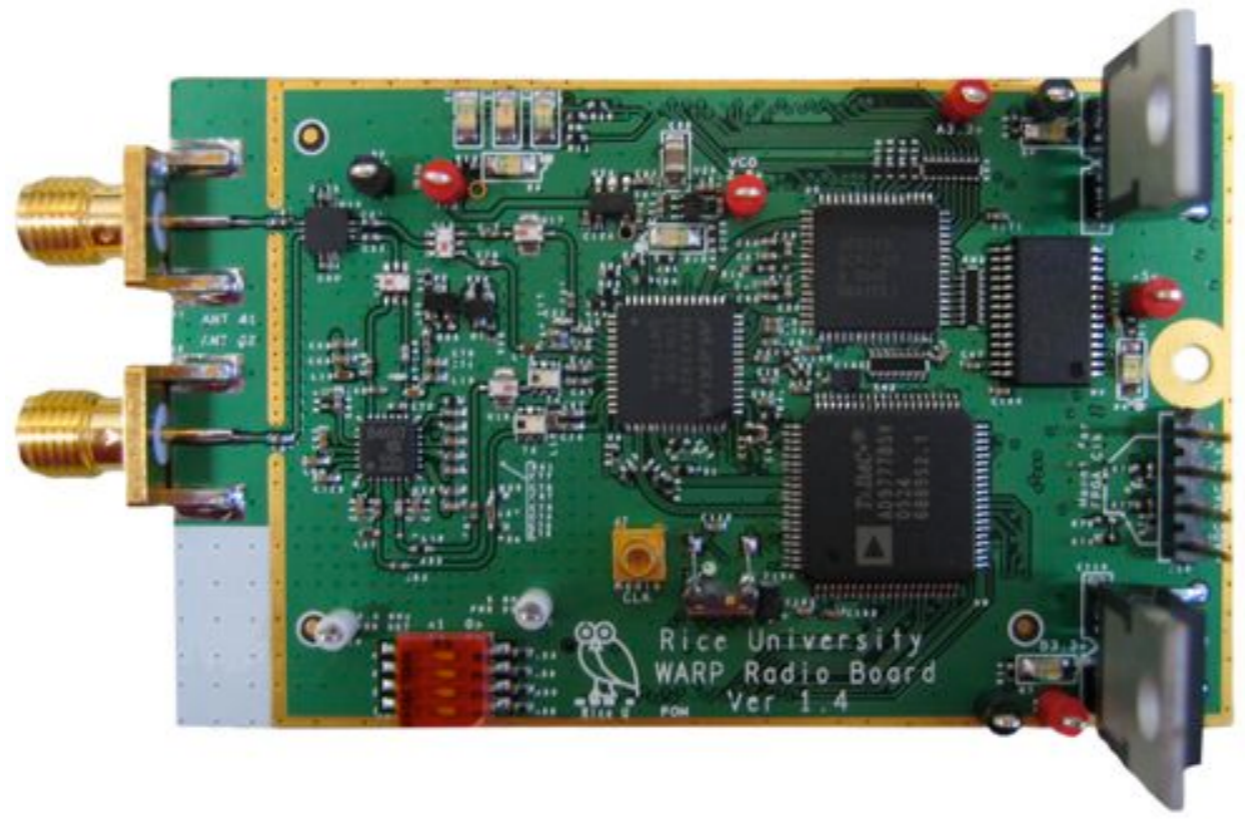
Questions?

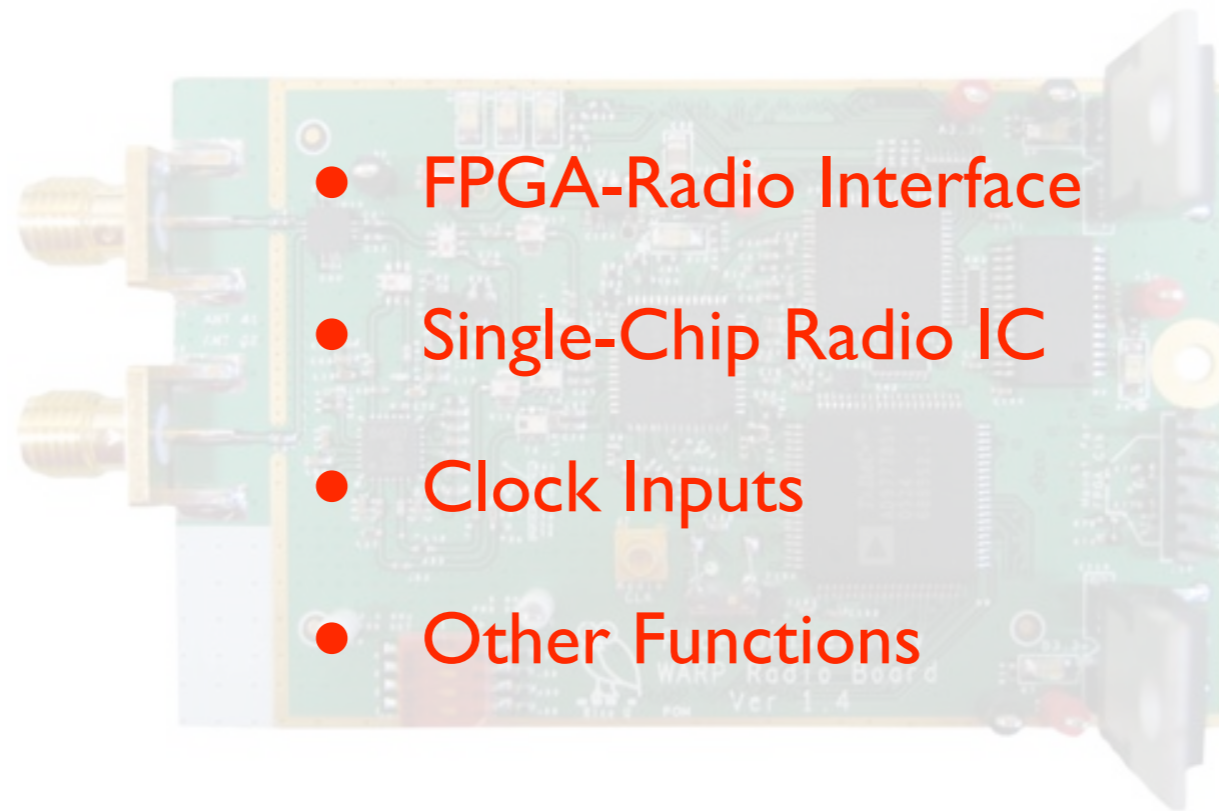


WARP Hardware

- WARP Hardware Components
 - FPGA Board
 - Radio Board
 - Clock Board
- FPGA Architecture
- WARP Design Flows

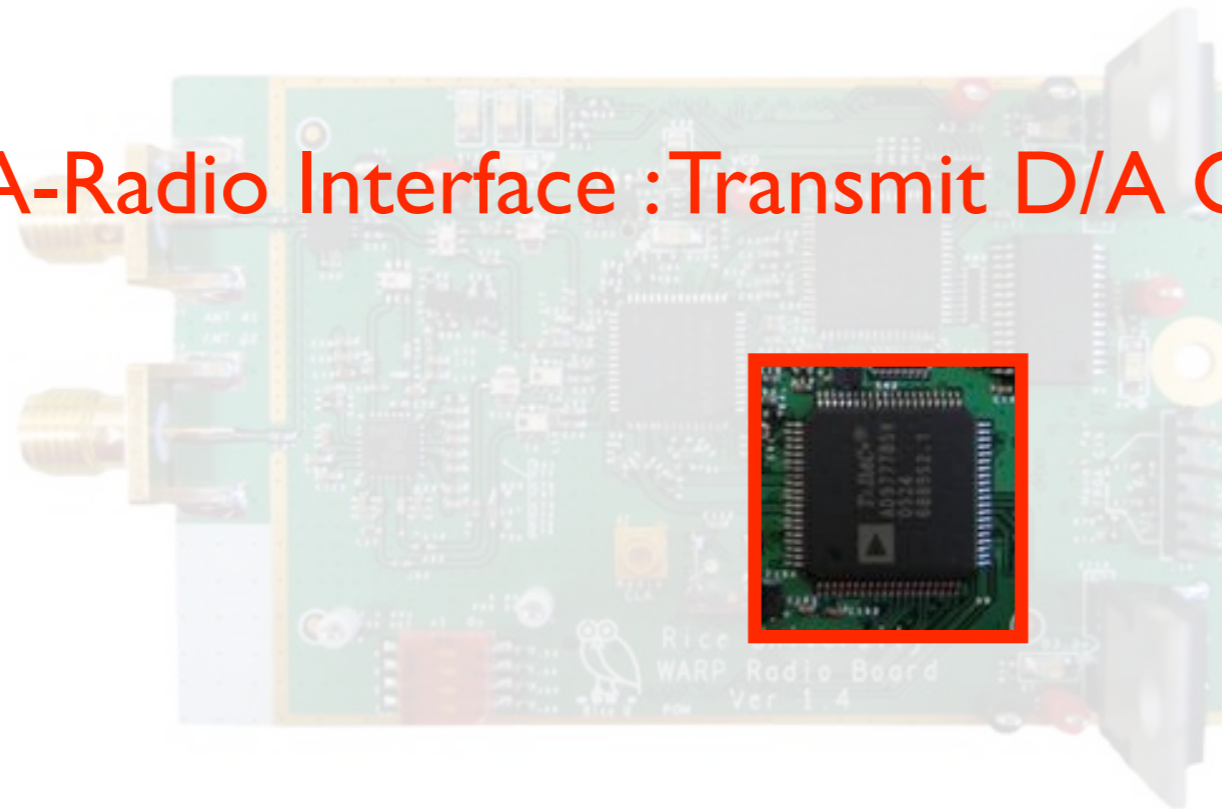






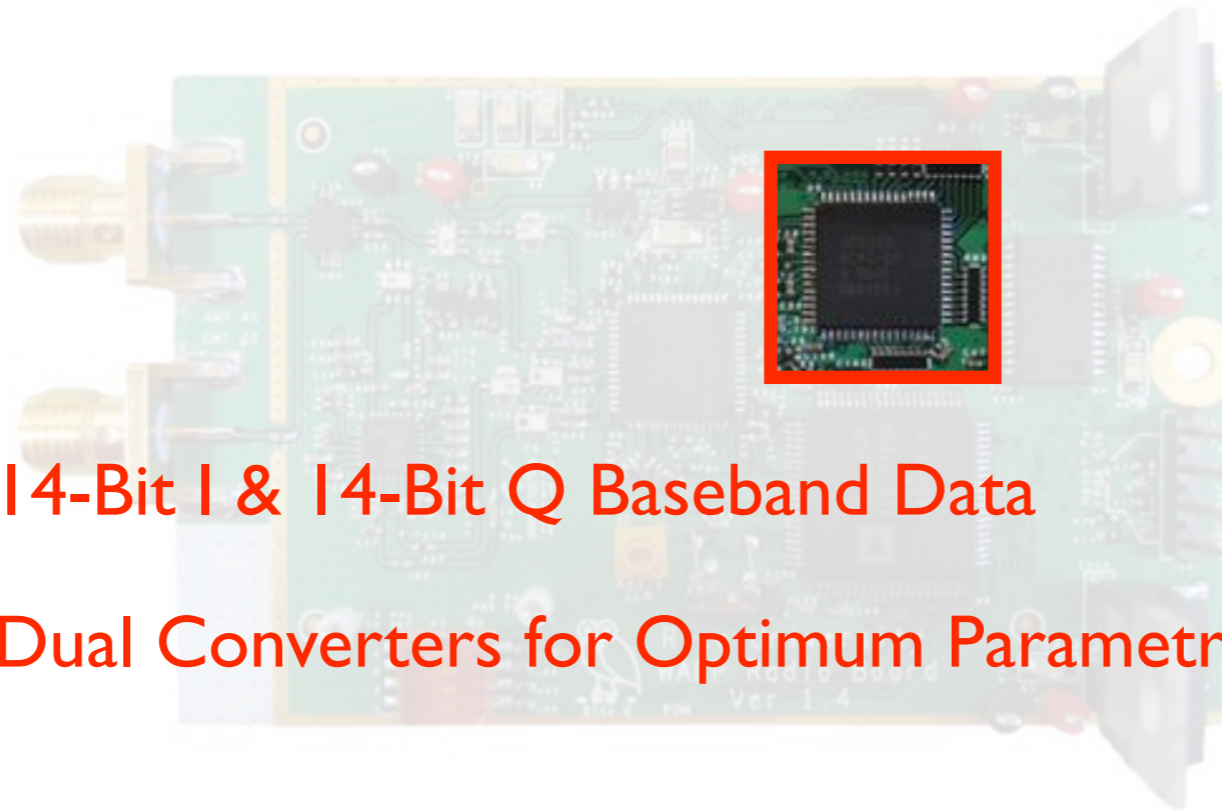
- FPGA-Radio Interface
- Single-Chip Radio IC
- Clock Inputs
- Other Functions

FPGA-Radio Interface : Transmit D/A Converters



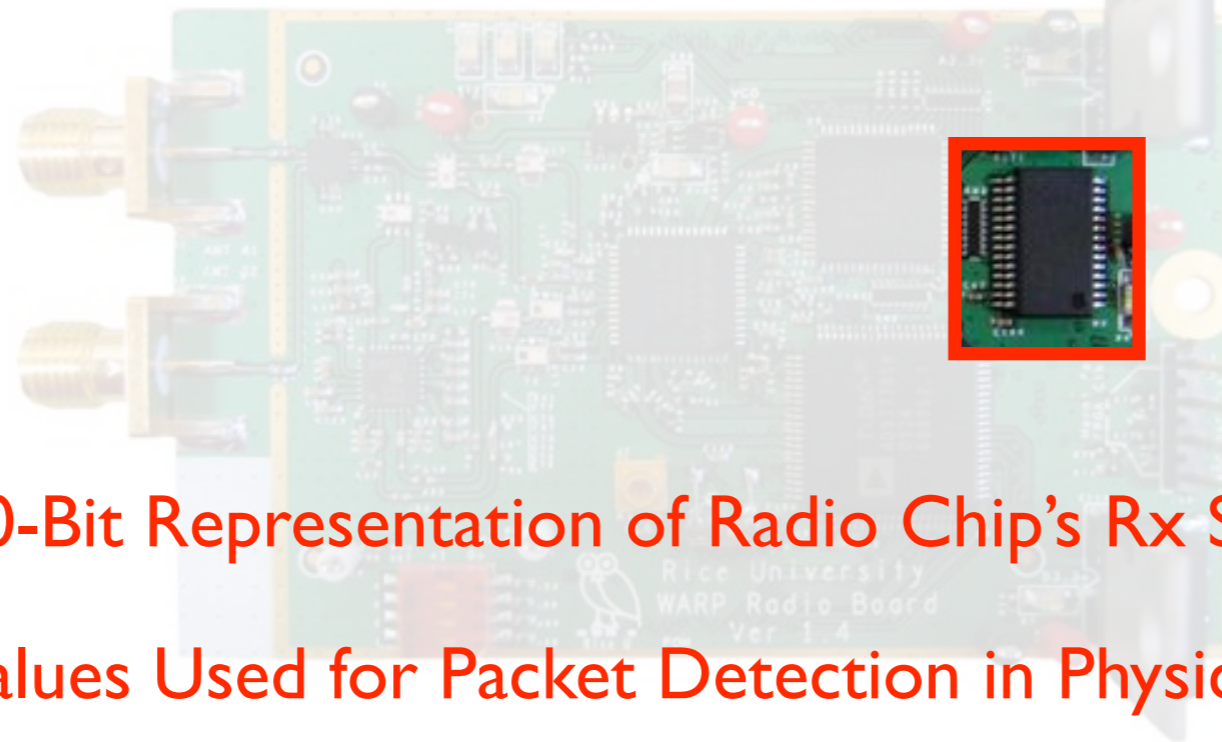
- 16-Bit I & 16-Bit Q Baseband Data
- Dual Converters for Optimum Parametric Matching

FPGA-Radio Interface : Receive A/D Converters

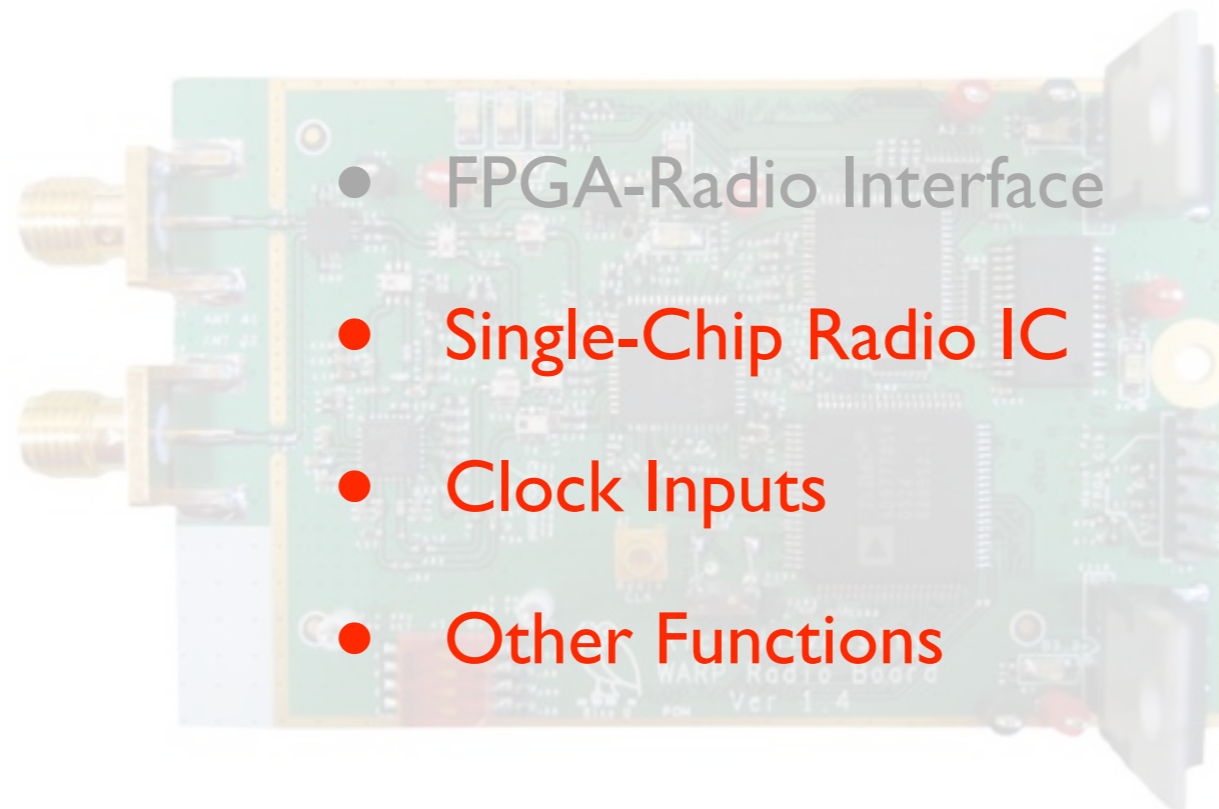


- 14-Bit I & 14-Bit Q Baseband Data
- Dual Converters for Optimum Parametric Matching

FPGA-Radio Interface : RSSI A/D Converter



- 10-Bit Representation of Radio Chip's Rx Signal Strength
- Values Used for Packet Detection in Physical Layer

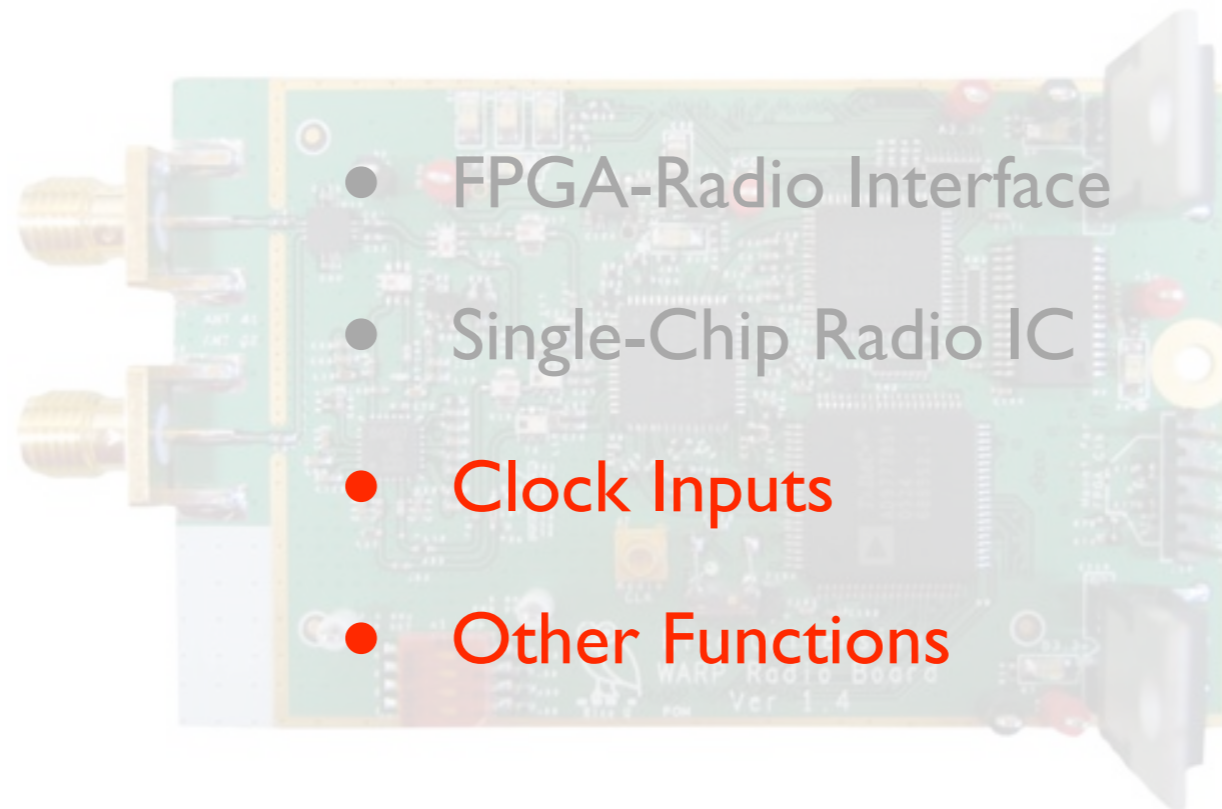


- FPGA-Radio Interface
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Single-Chip Radio IC : MAX2829

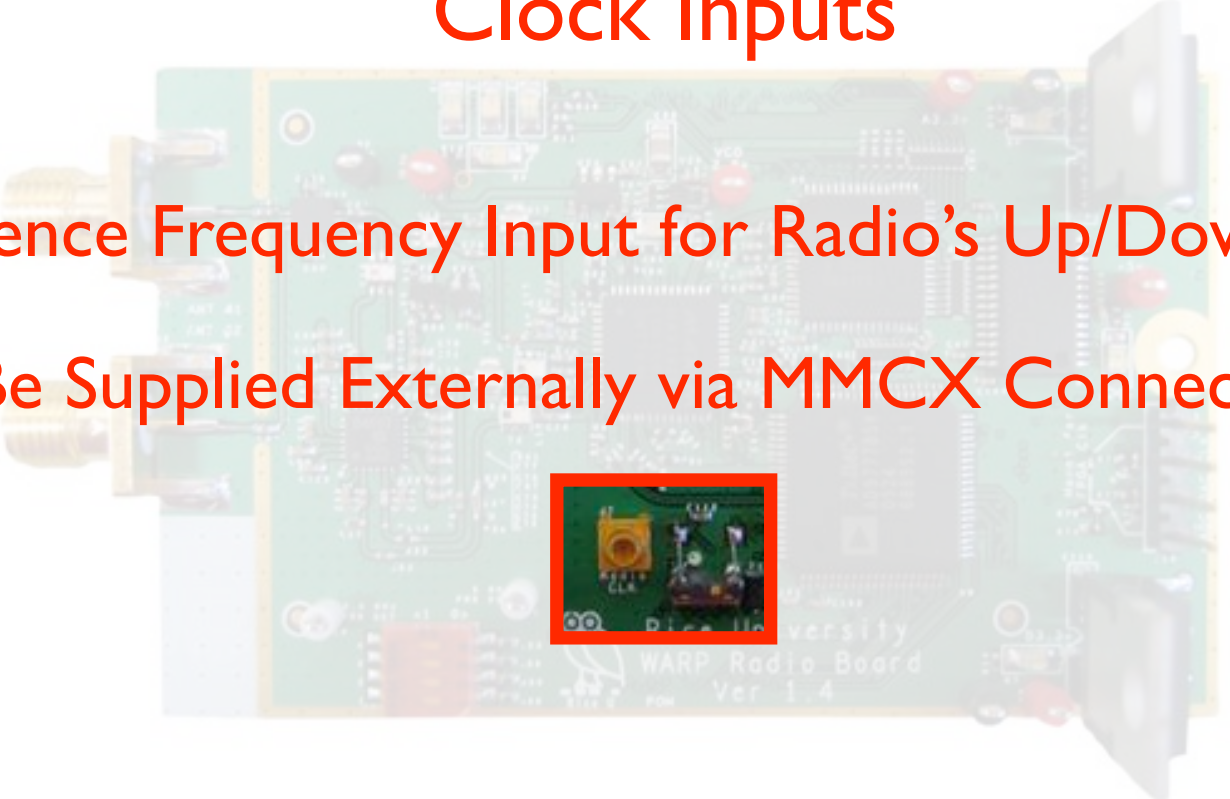


- Dual-Band Operation : 2.4 GHz and 5 GHz
- Direct Conversion Between RF and Baseband
- 40 MHz Bandwidth Independent of Carrier Frequency



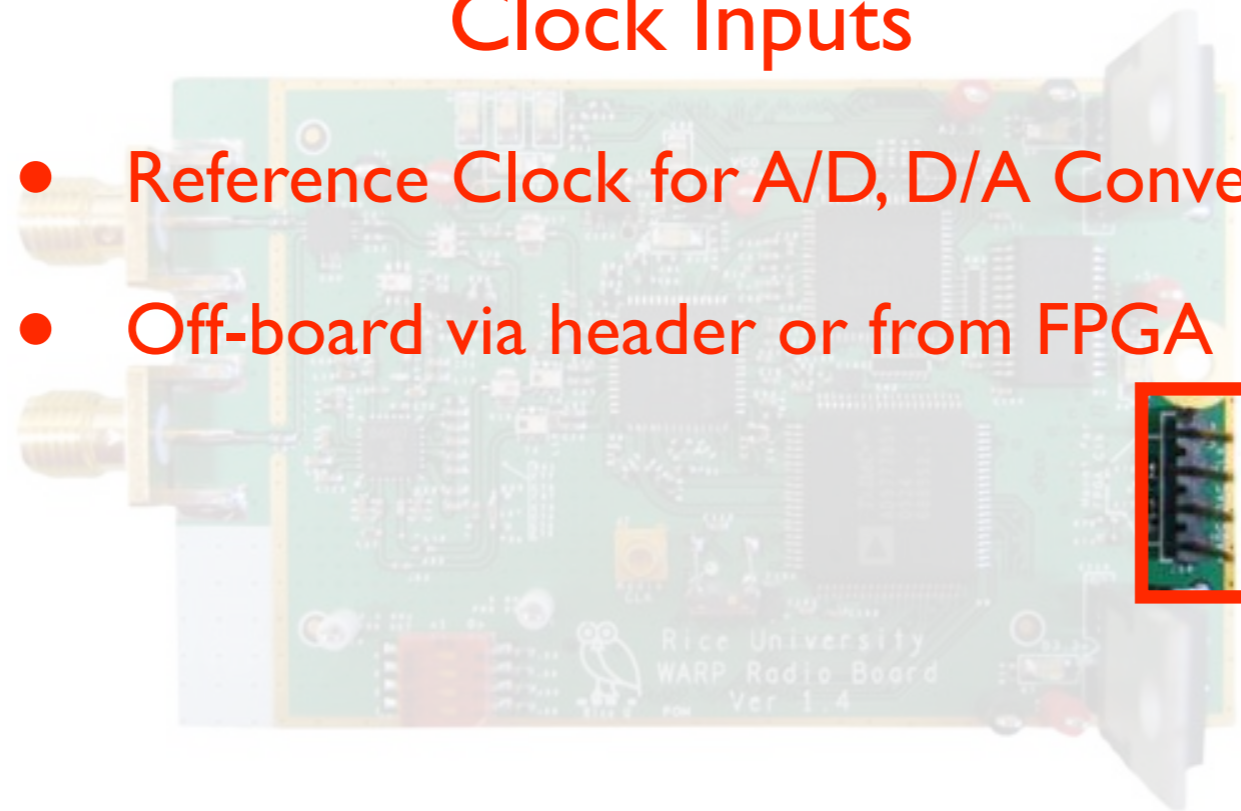
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- Single-Chip Radio IC
- **Clock Inputs**
- **Other Functions**

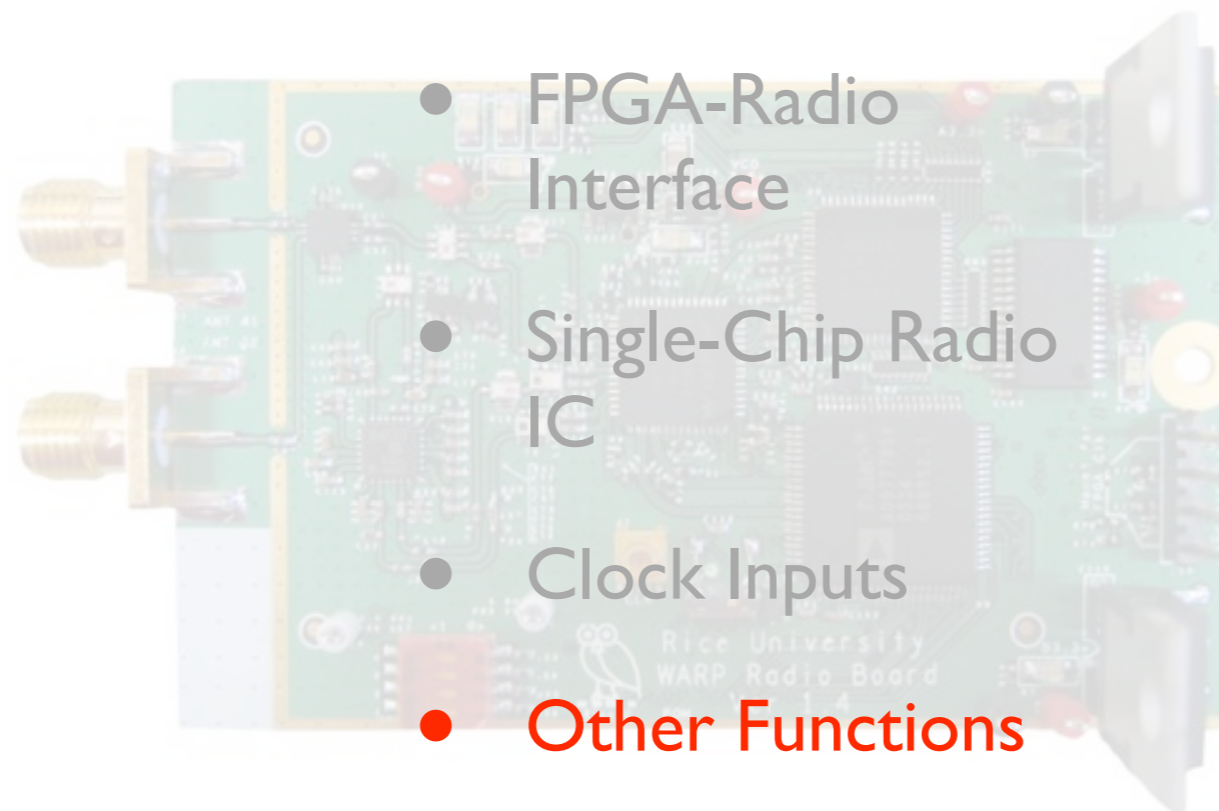
Clock Inputs

- Reference Frequency Input for Radio's Up/Down Conversion
 - May Be Supplied Externally via MMCX Connector
- 
- May Be Supplied Locally via Onboard Oscillator
 - Low-Frequency Signal is Up-Converted by Radio IC

Clock Inputs

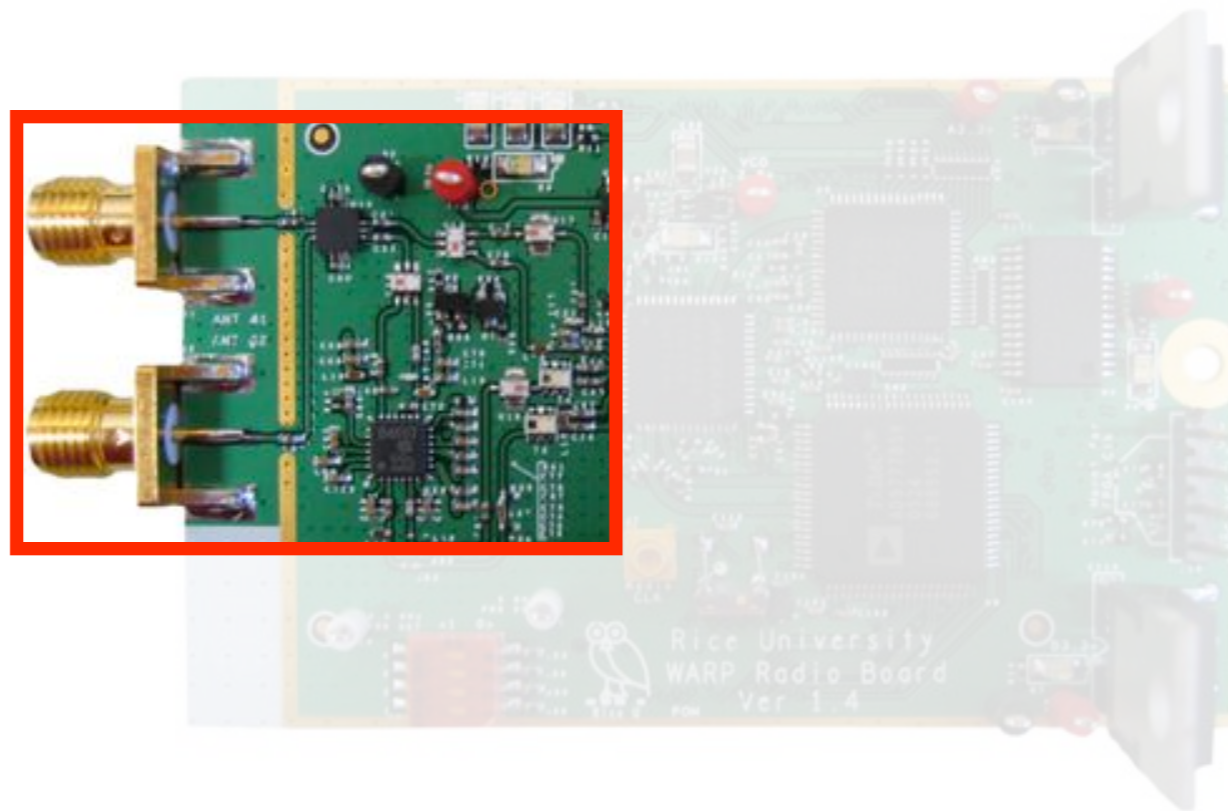
- Reference Clock for A/D, D/A Converters
- Off-board via header or from FPGA



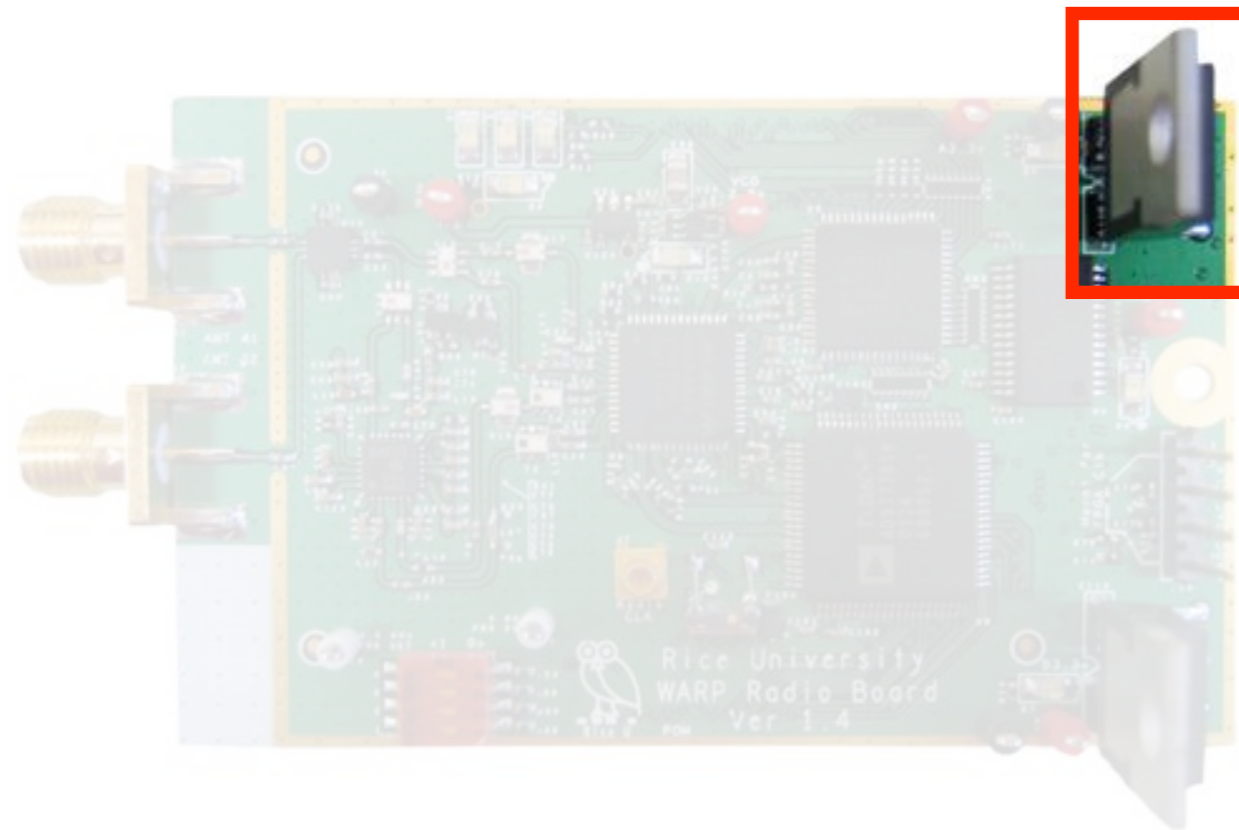


- FPGA-Radio Interface
- Single-Chip Radio IC
- Clock Inputs
- Other Functions

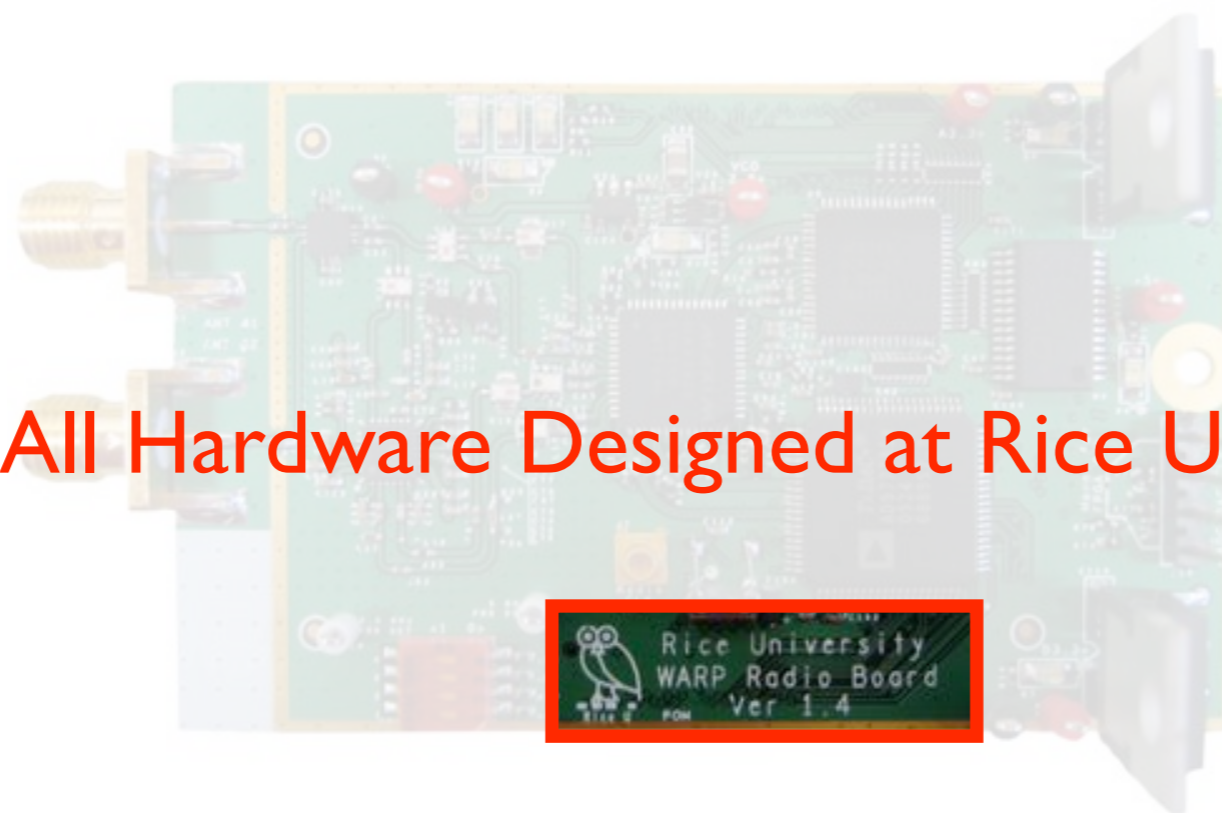
Other Functions : RF Front-End

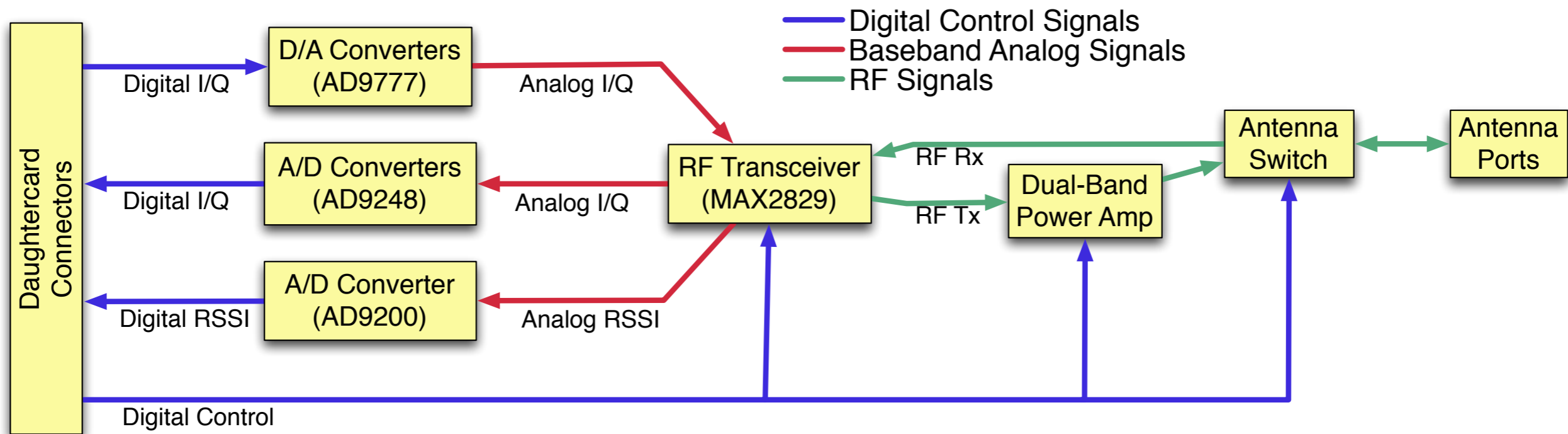


Other Functions : Power Regulators

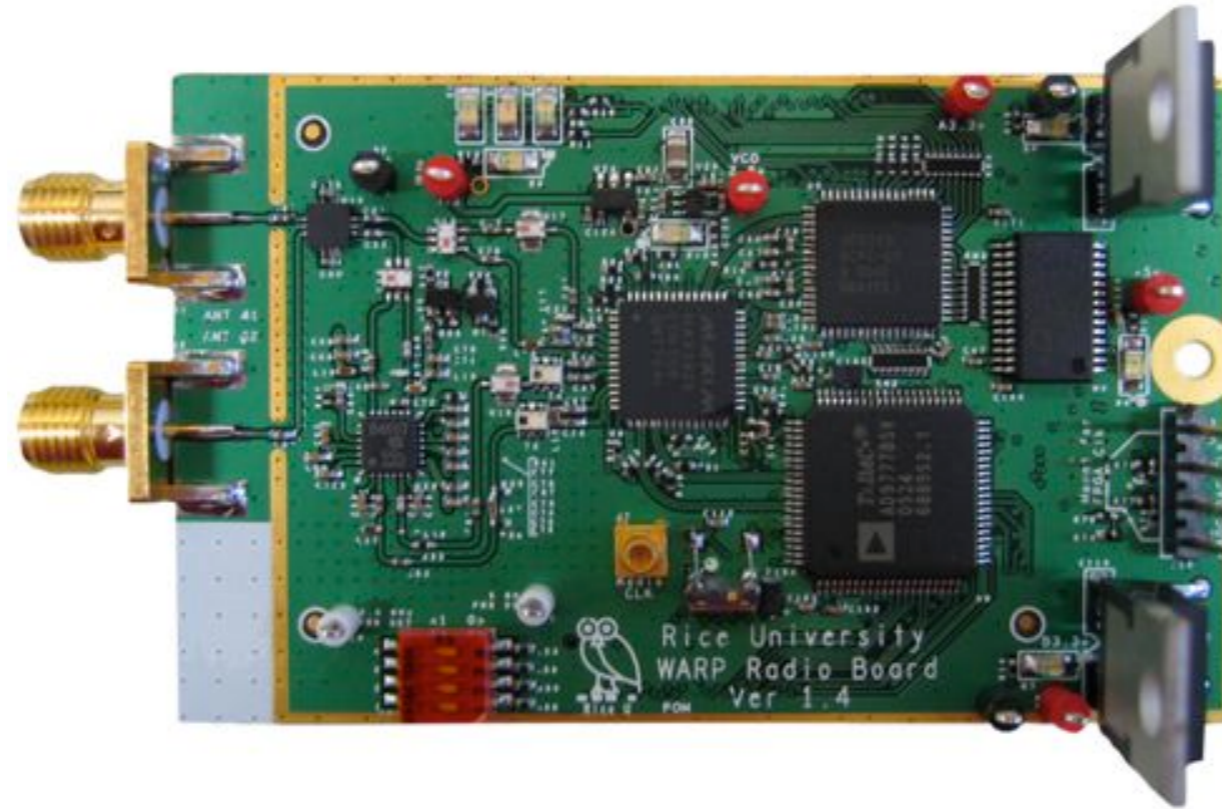


All Hardware Designed at Rice University



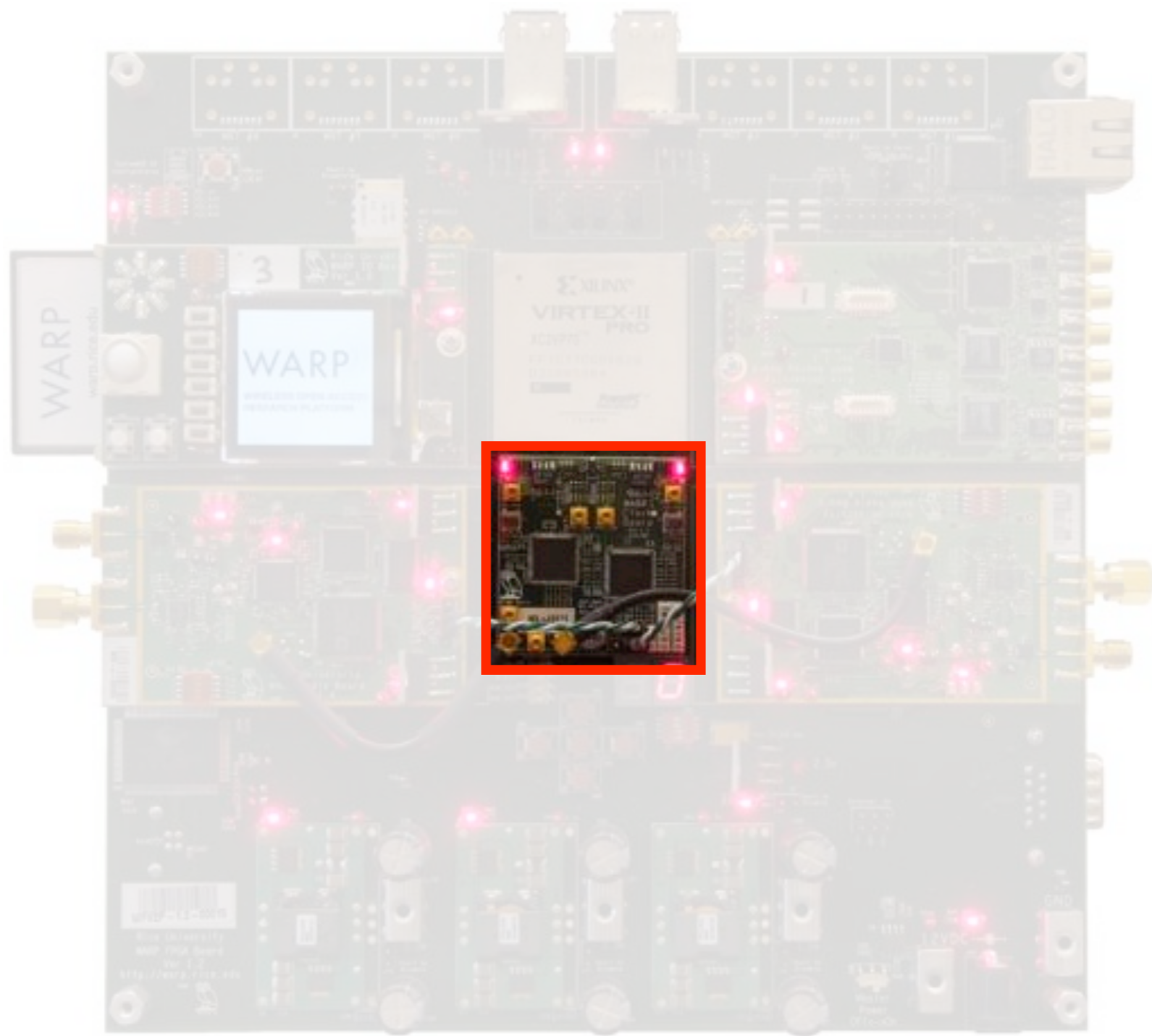


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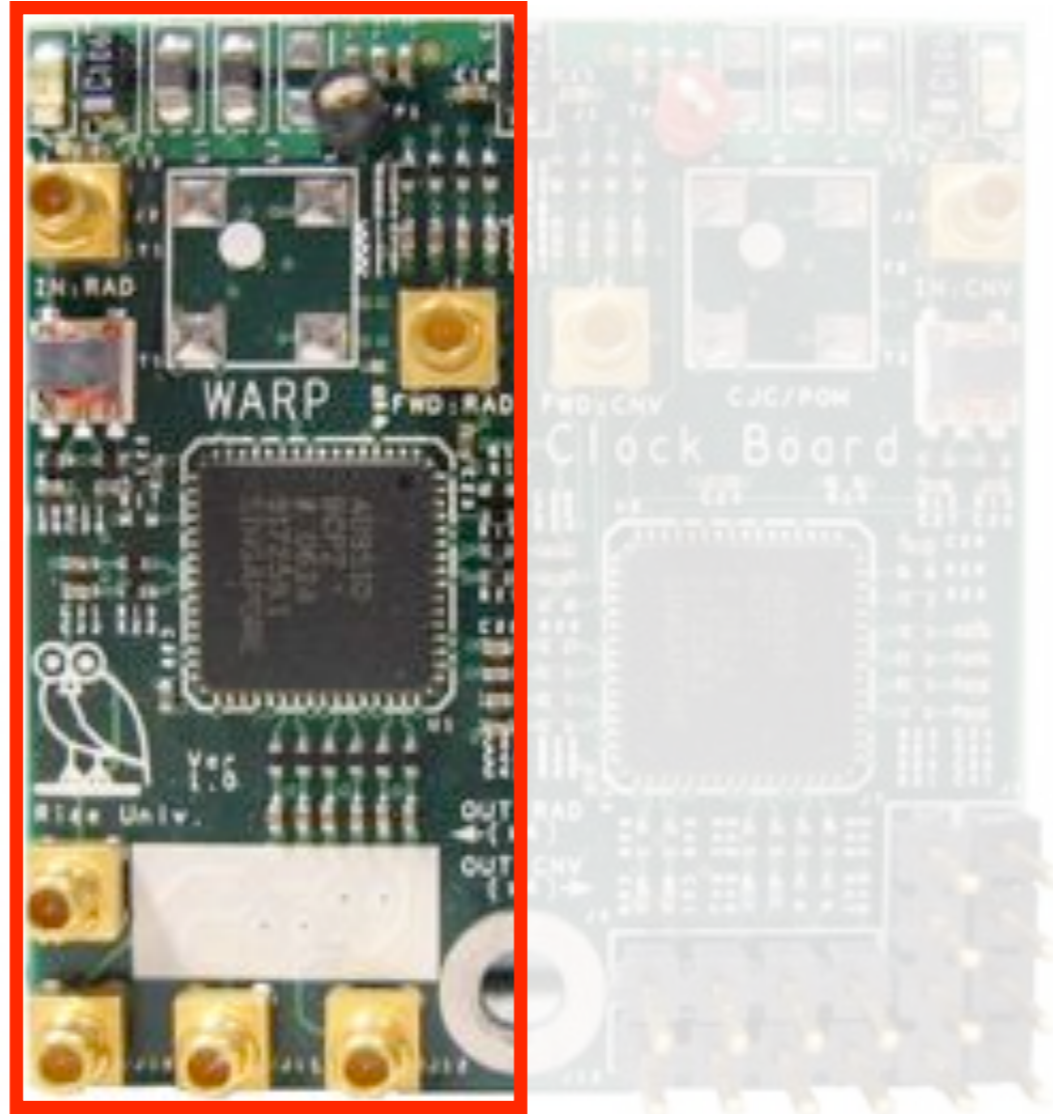
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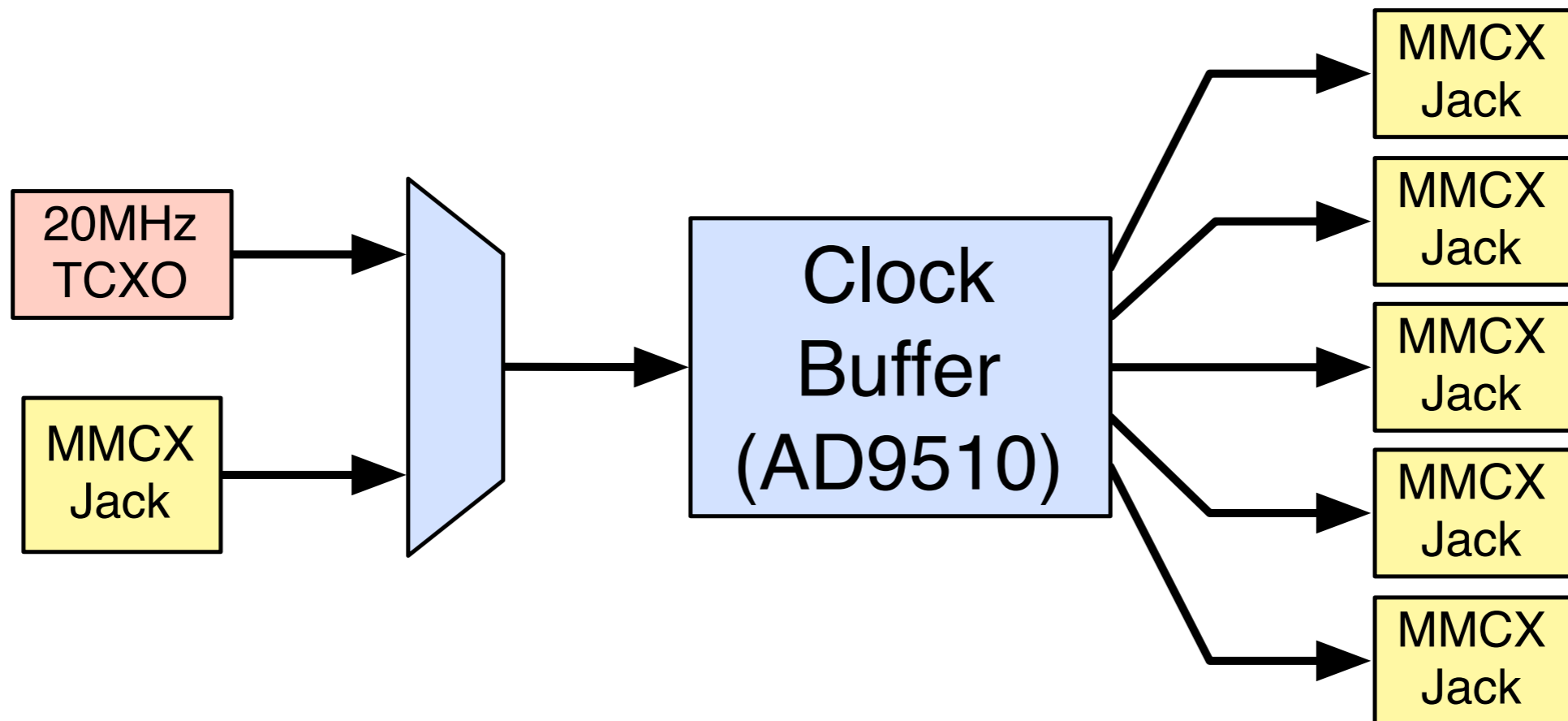


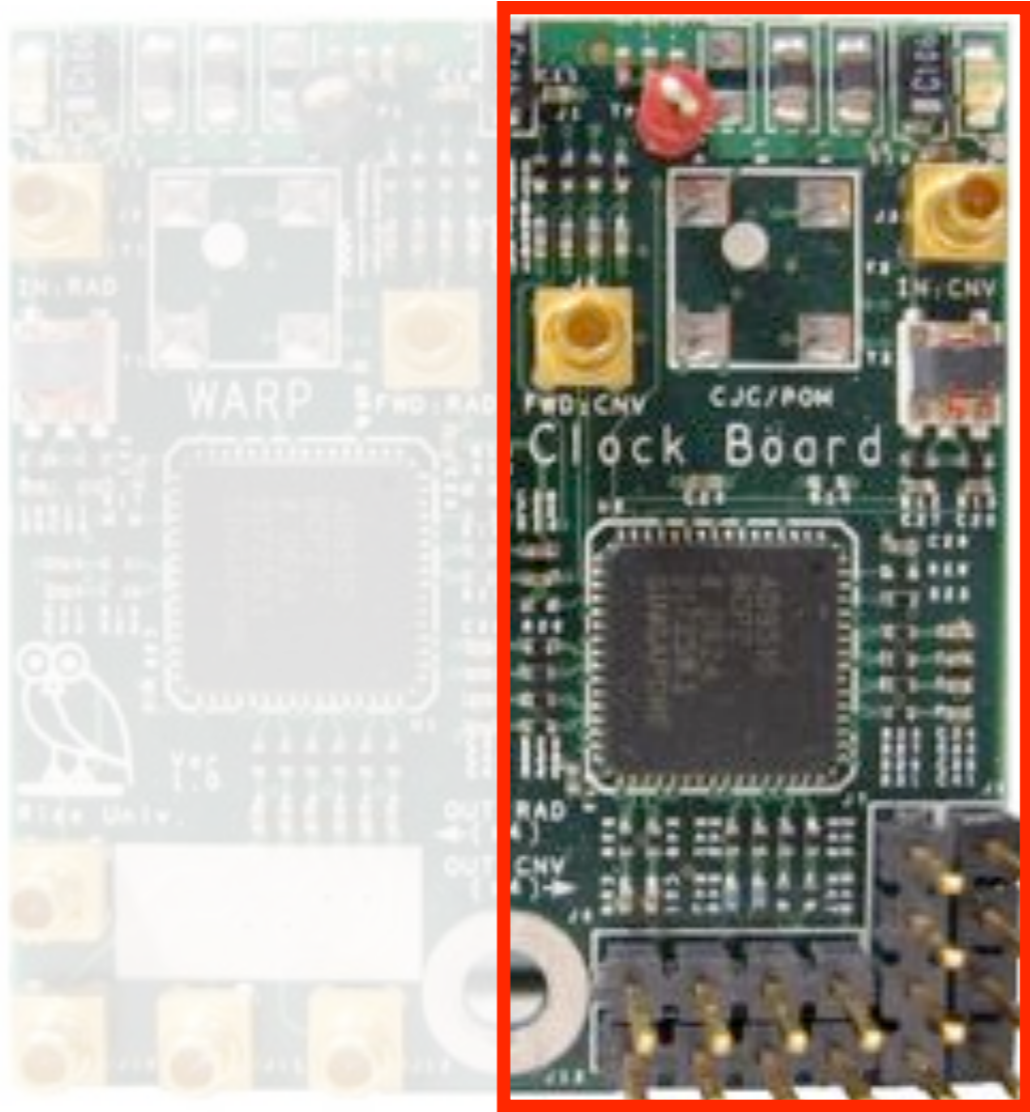


Radio Clock



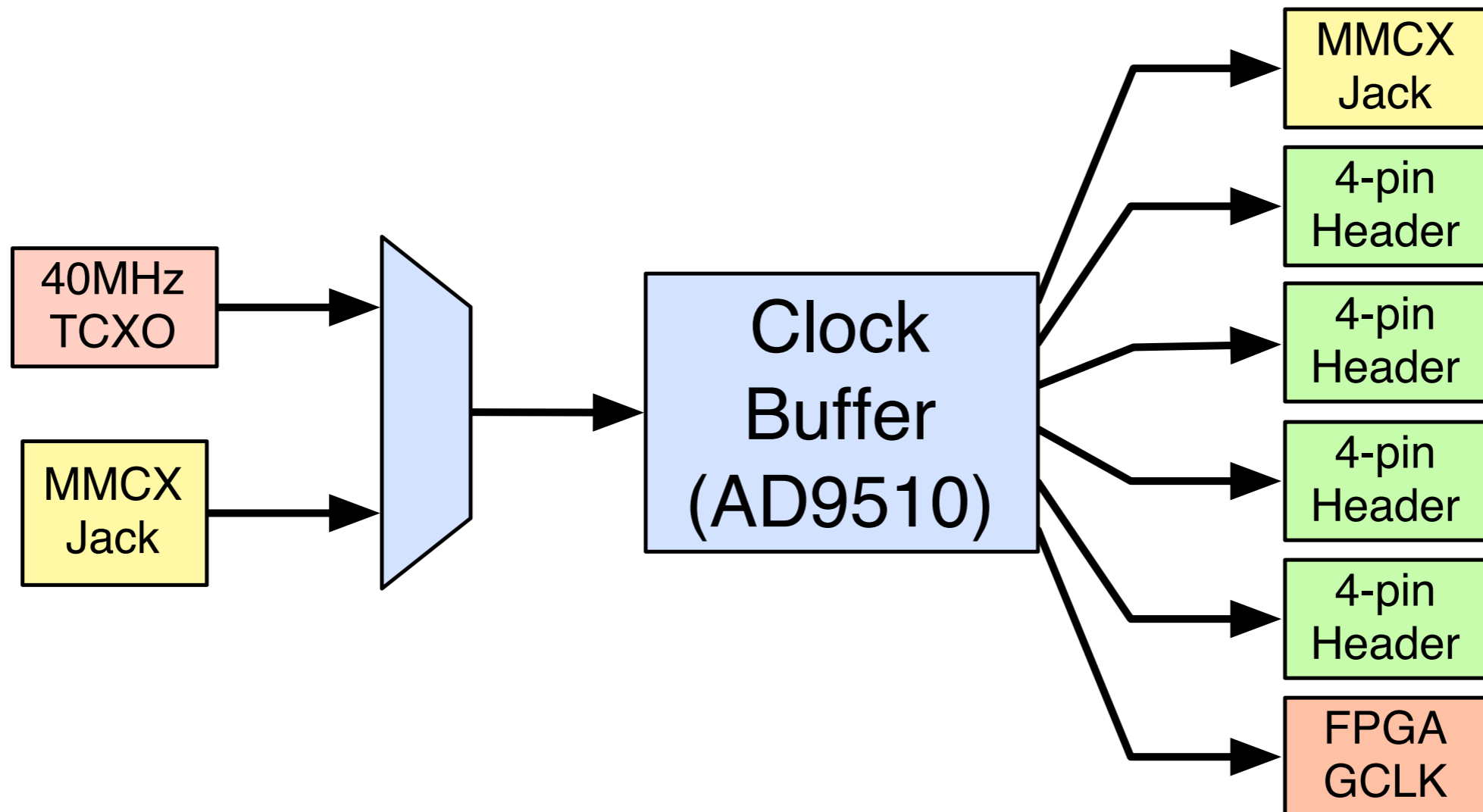
Radio Clock





Logic Clock

Logic Clock



Questions?



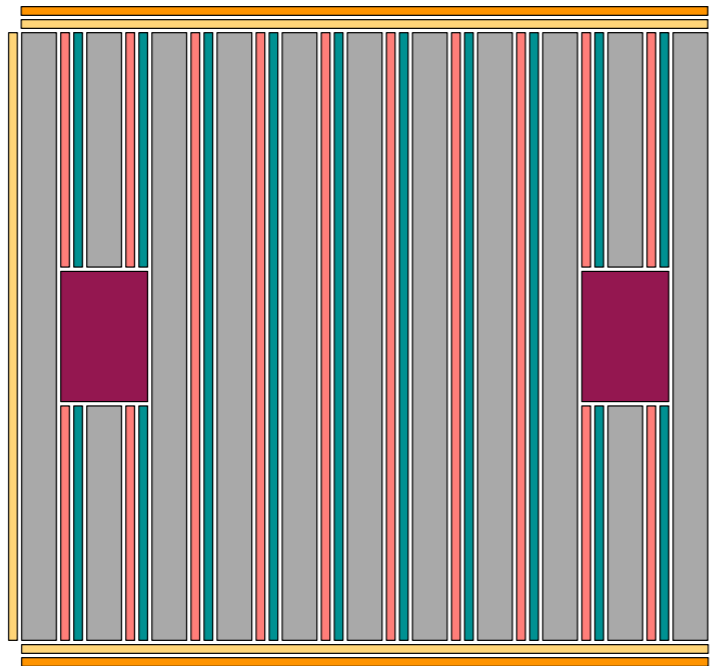
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XC2VP70 Internal Resources

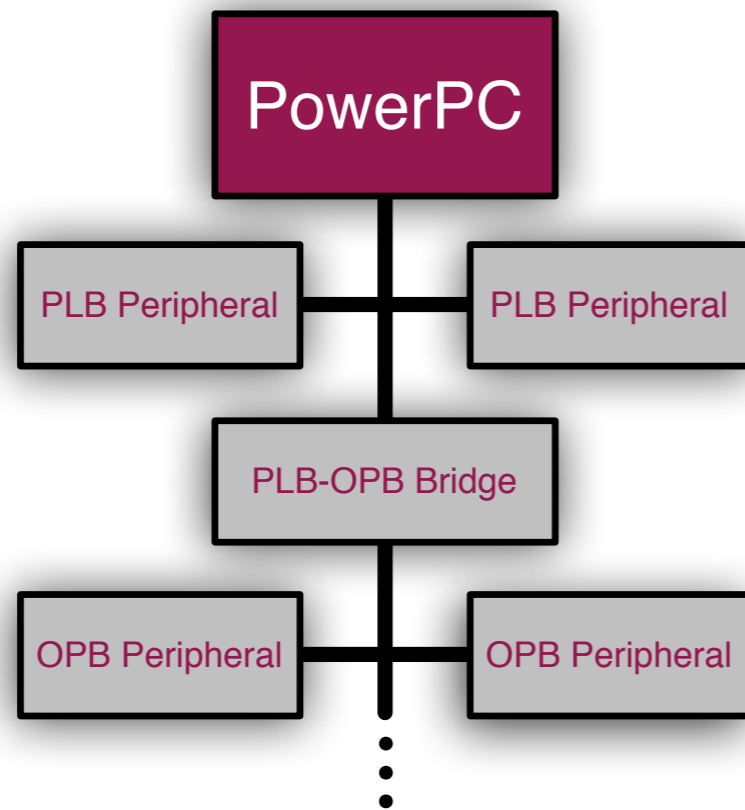


XC2VP70 Resources



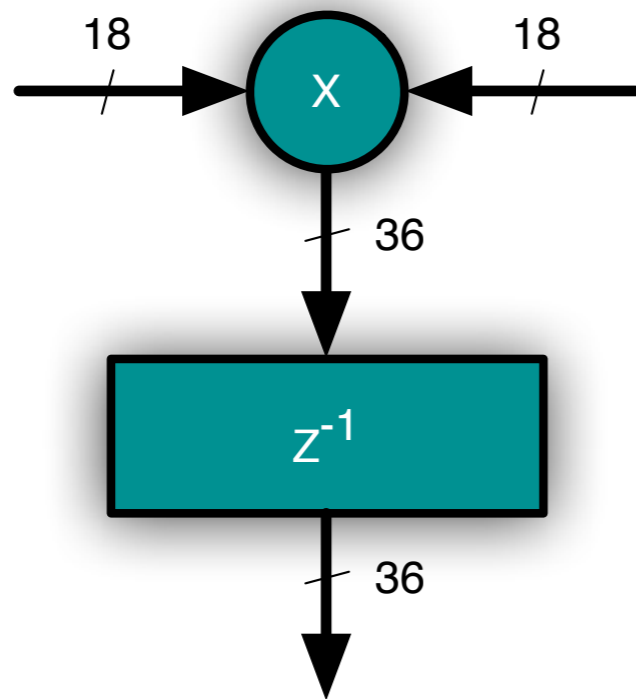
- Embedded PowerPC processors
- 18-Bit by 18-Bit multipliers
- 18 Kbit block RAMs
- General purpose I/Os
- Multi-gigabit transceivers (MGTs)
- Reconfigurable user logic (Fabric)

Embedded PowerPCs



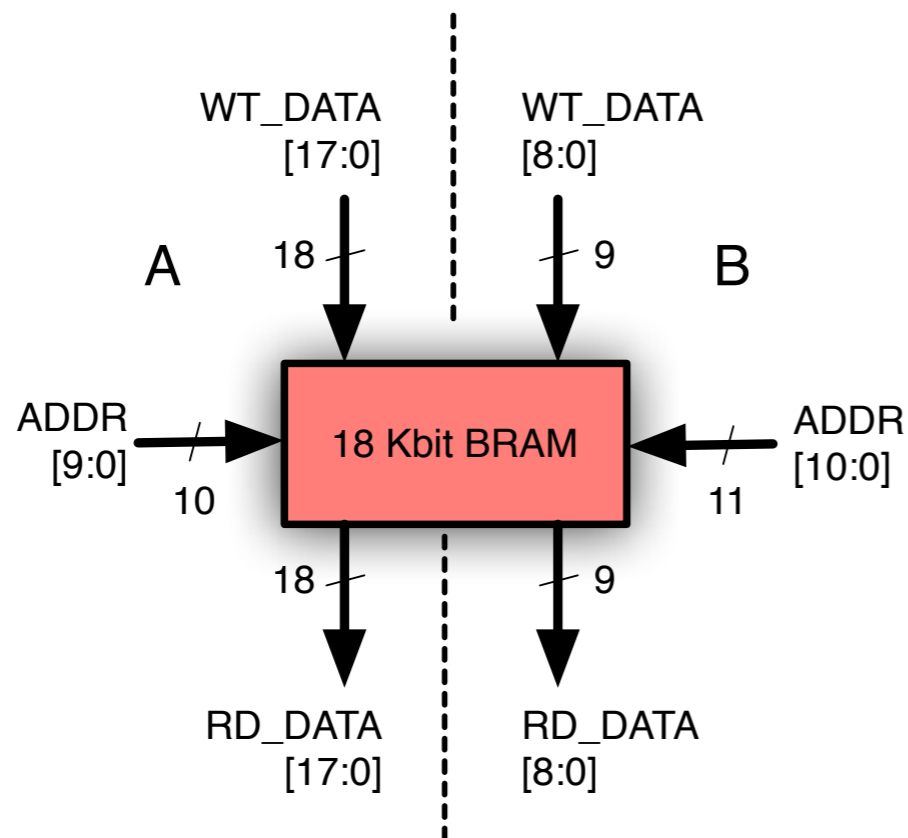
- PPCs connect to peripherals through the IBM Processor Local Bus (PLB)
- Alternative connections via the simpler On-Chip Peripheral Bus (OPB)
- PPCs execute user software for high-level control and data processing
- WARP tools simplify implementation of custom OPB-compliant peripheral cores

18-Bit x 18-Bit Multipliers



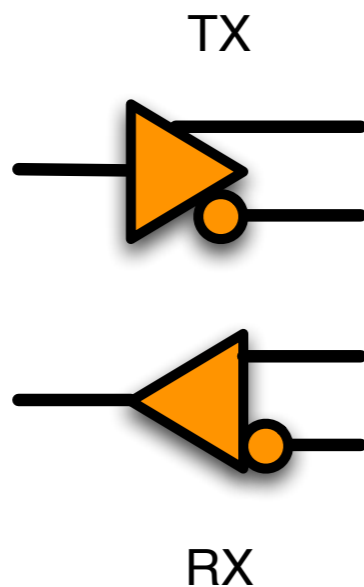
- Signed fixed-point inputs and outputs
- Fully synchronous operation with one result per clock cycle
- Tightly coupled with embedded block RAMs for very high throughput
- Operate independently and in parallel
- May be combined to support larger operands and results

18 Kbit Block RAMs



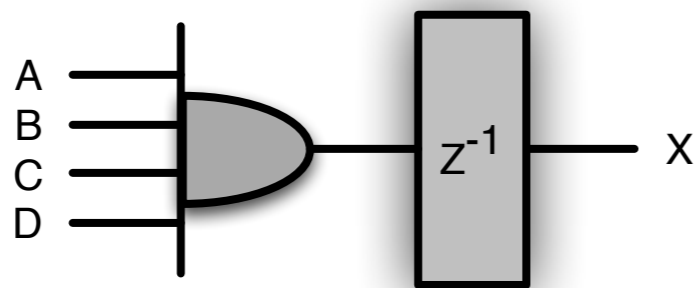
- Dual-ported for simultaneous reads and writes
- Simplifies construction of dual-port FIFOs
- Addressable via different aspect ratio on each port
- Coupled one-to-one with multipliers for extremely high throughput
- Operate independently and in parallel
- May be combined for increased capacity

Multi-Gbit Transceivers



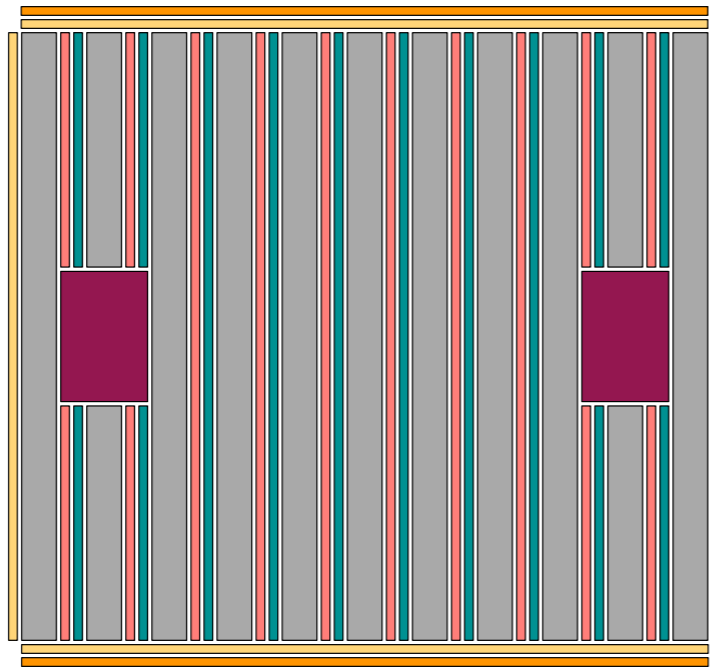
- High-speed serial links : 622 Mbps up to 3.125 Gbps
- Implement Physical Media Attachment and Physical Coding sublayers
- Perform 8b/10b encoding and decoding
- Clock and data recovered from received data stream
- Usable in low latency mode when clocks are matched at Tx and Rx

User Logic (FPGA Fabric)



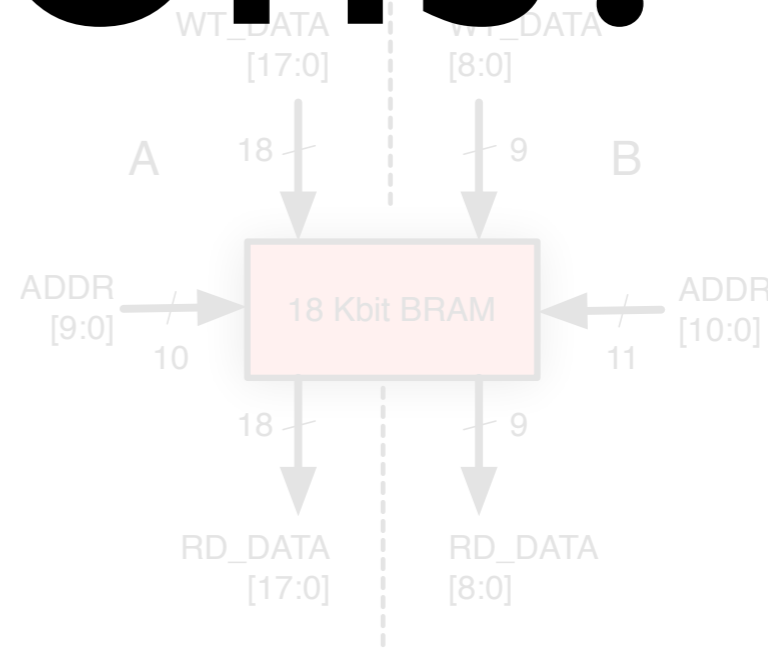
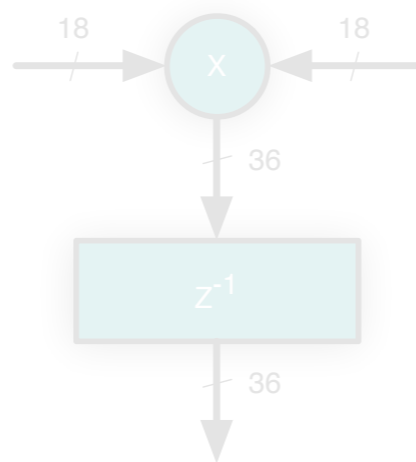
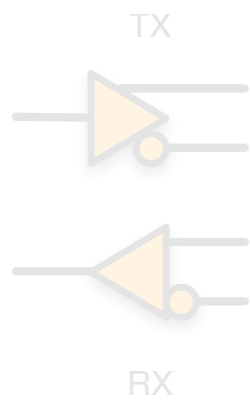
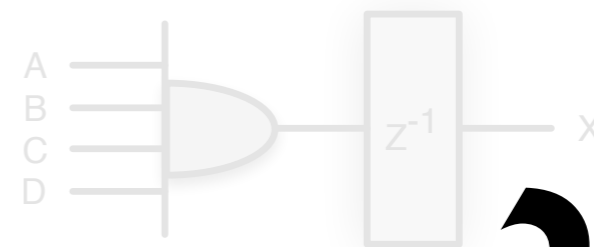
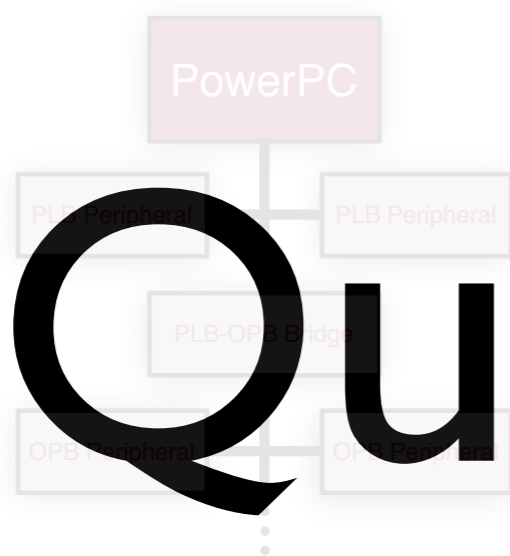
- Fine-grained array of reconfigurable logic based on 4-input LUTs
- Distributed throughout device
- Interspersed with discrete flip-flops for efficient implementation of registered logic
- Implements general purpose user functionality (e.g. WARP OFDM transceivers)
- Glues together and enhances dedicated cores within the FPGA

XC2VP70 Resources



- 2 PowerPC processors
- 328 multipliers
- 328 block RAMs
- 964 general purpose I/Os
- 16 MGTs (8 on WARP FPGA board)
- 66176 4-input LUTs
- 66176 flip-flops (plus I/O registers)

Questions?

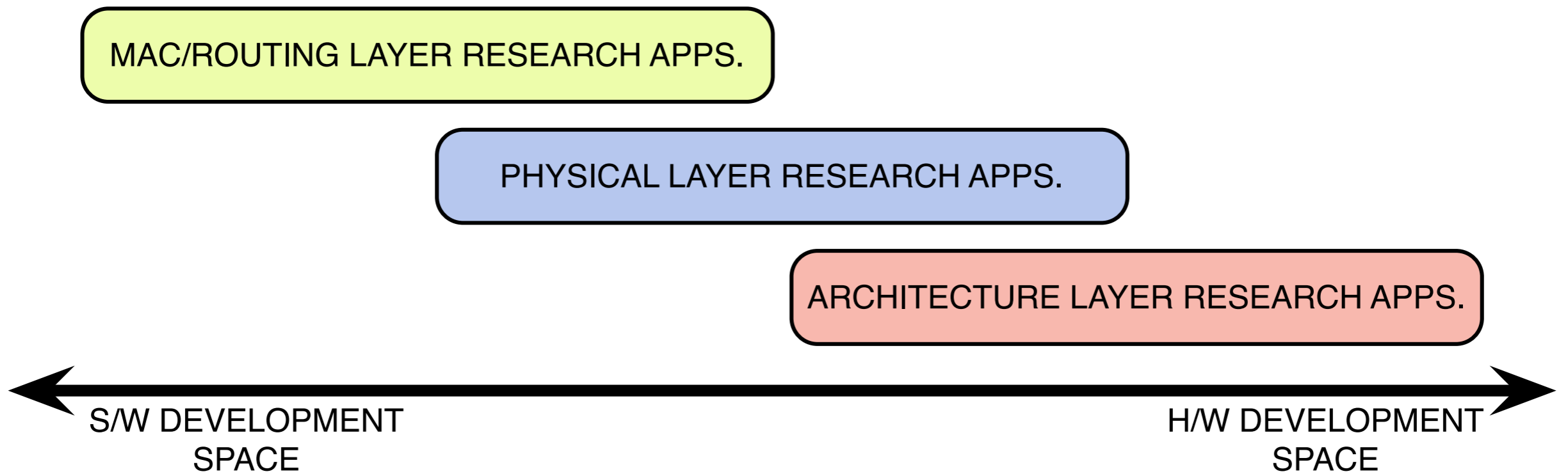


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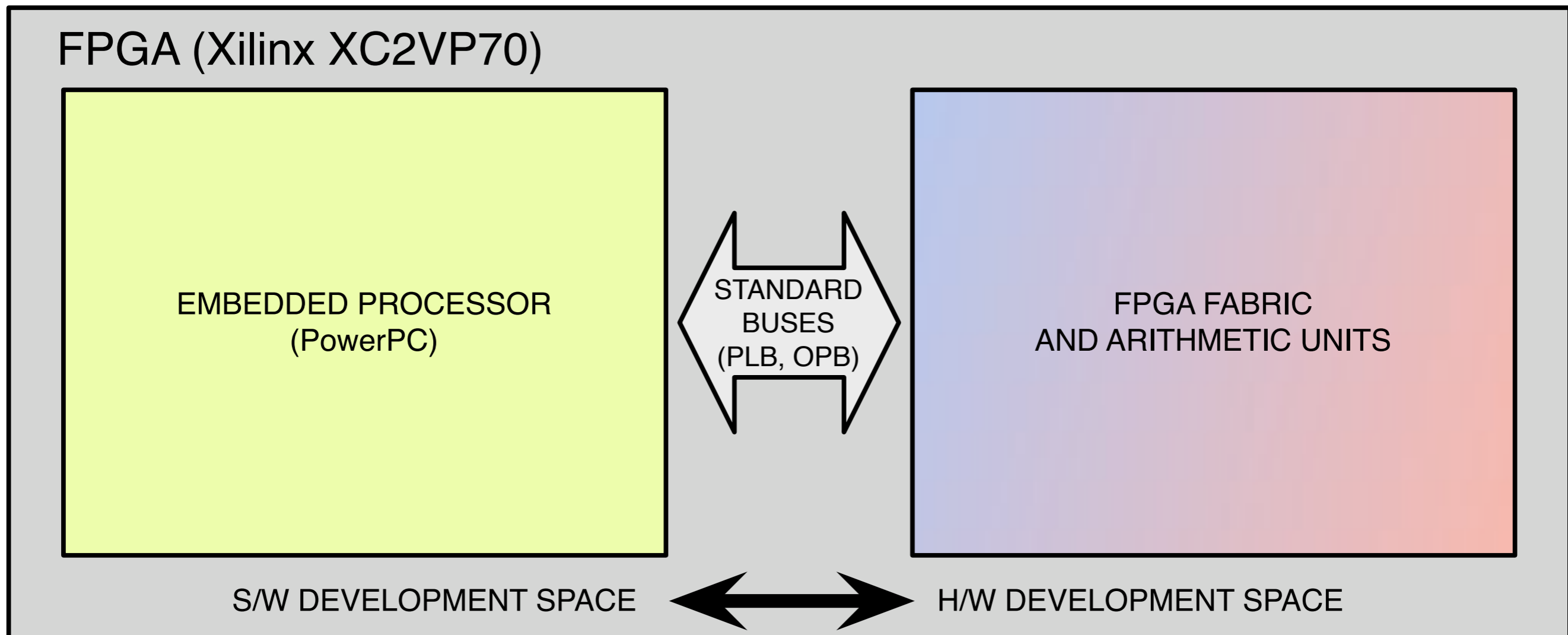
Targeting WARP Hardware

(Classifying Applications by Development Space)



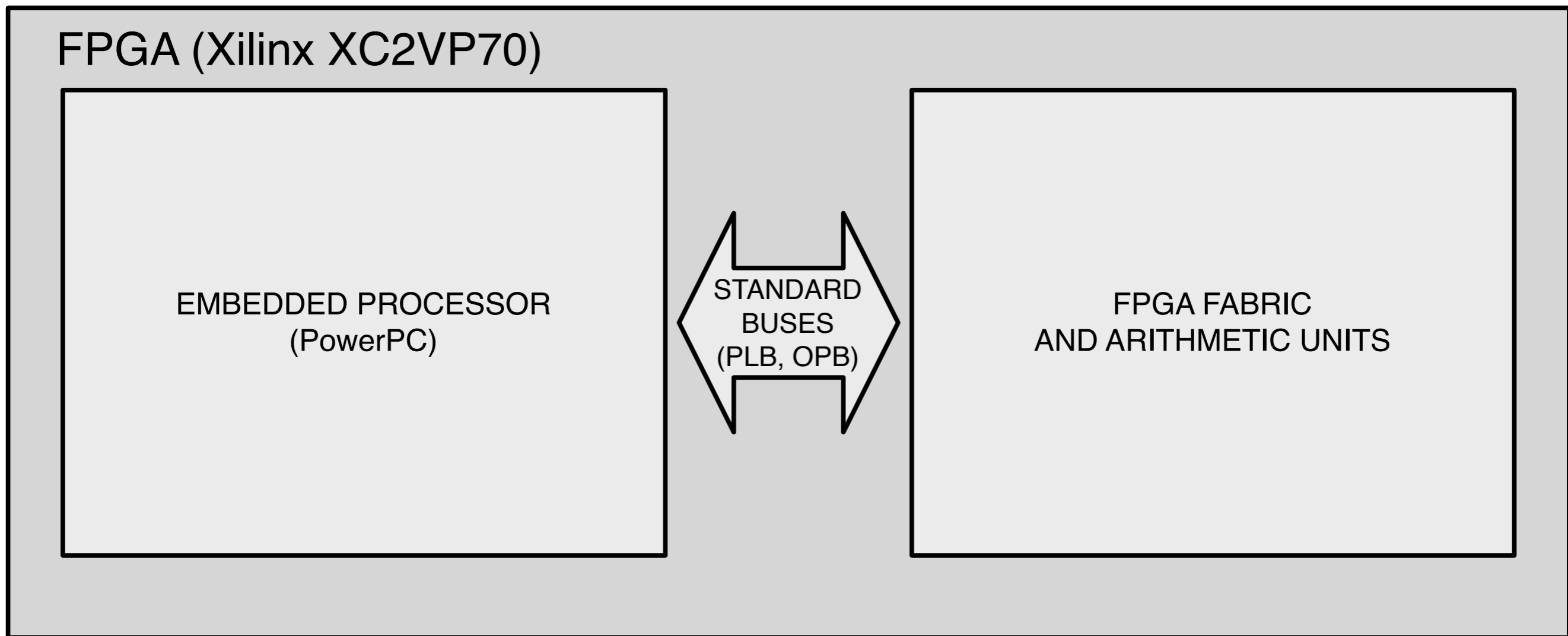
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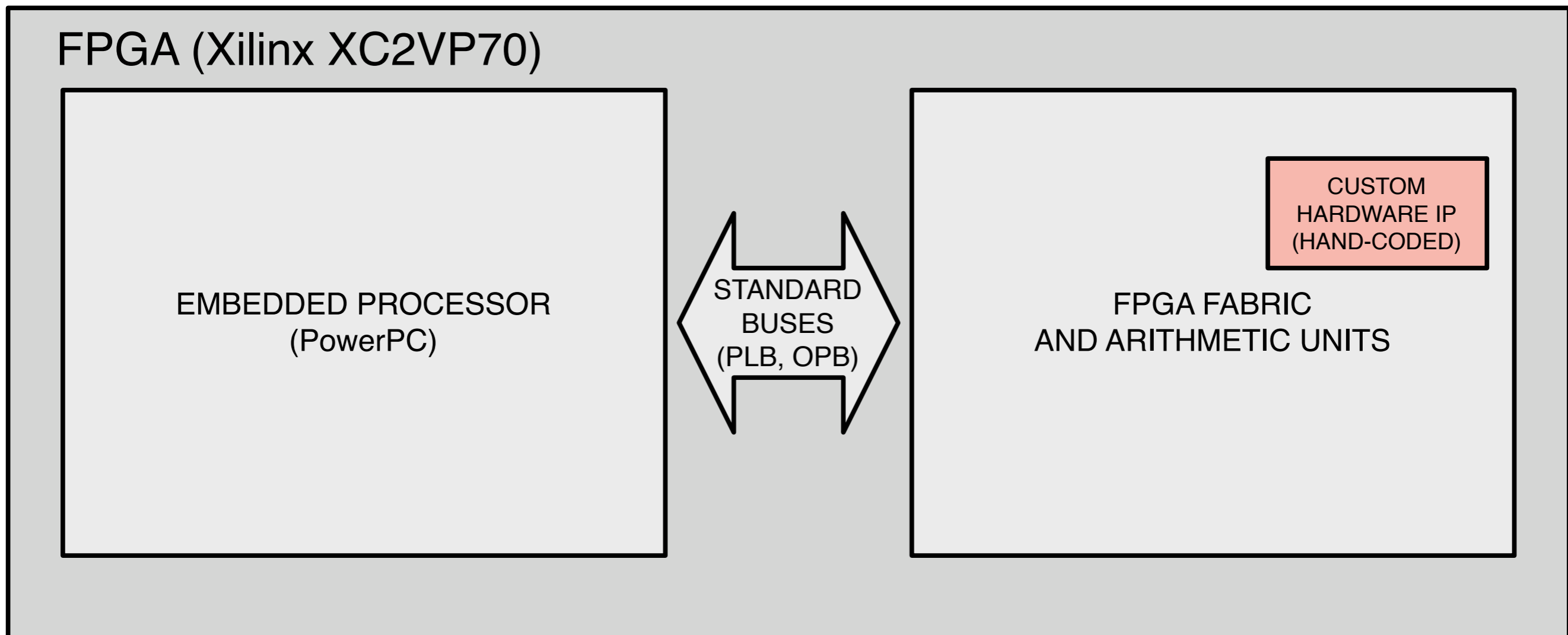
Targeting WARP Hardware

(Understanding the Development Environment)



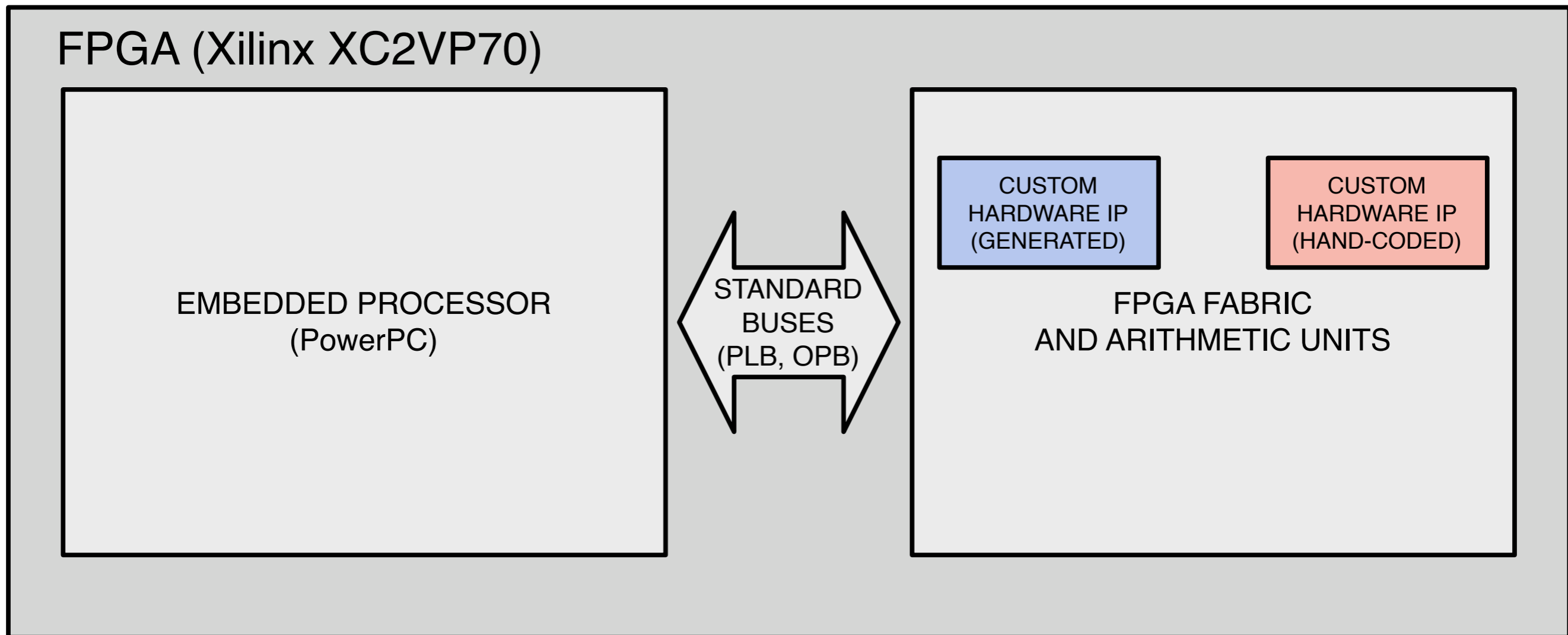
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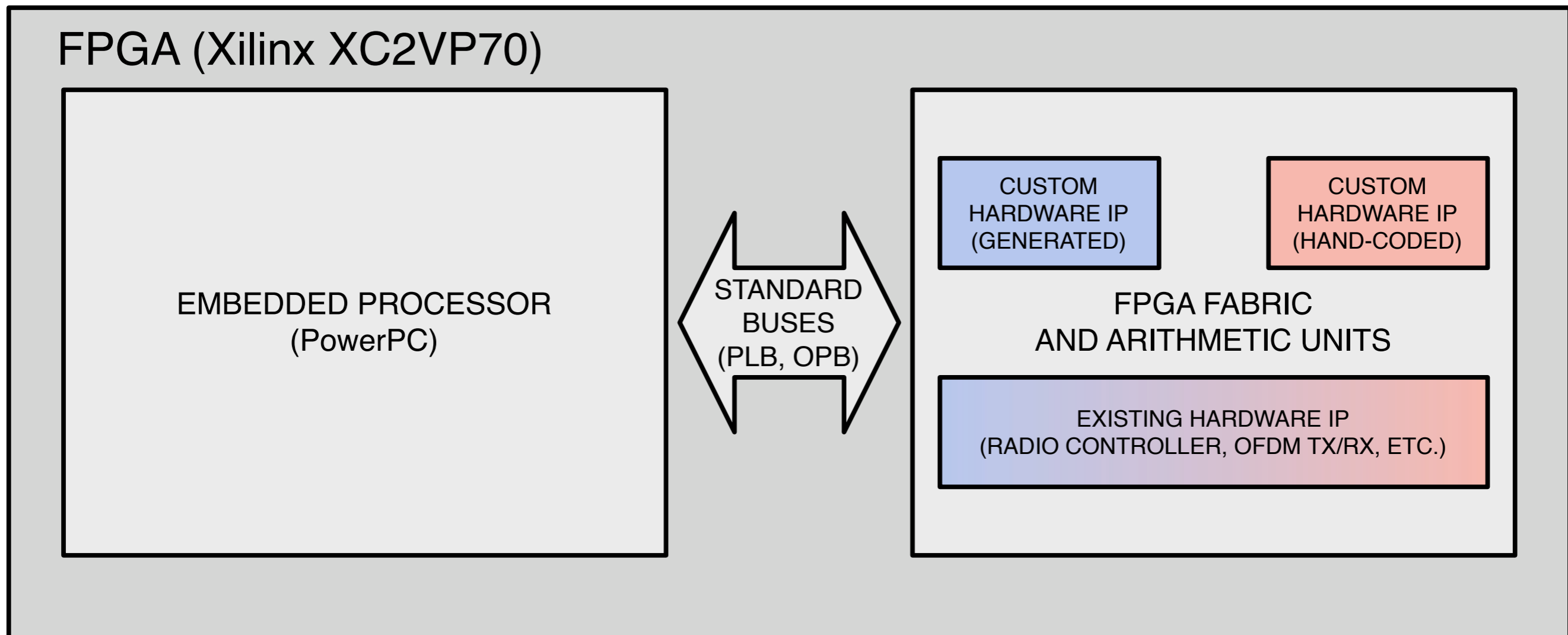
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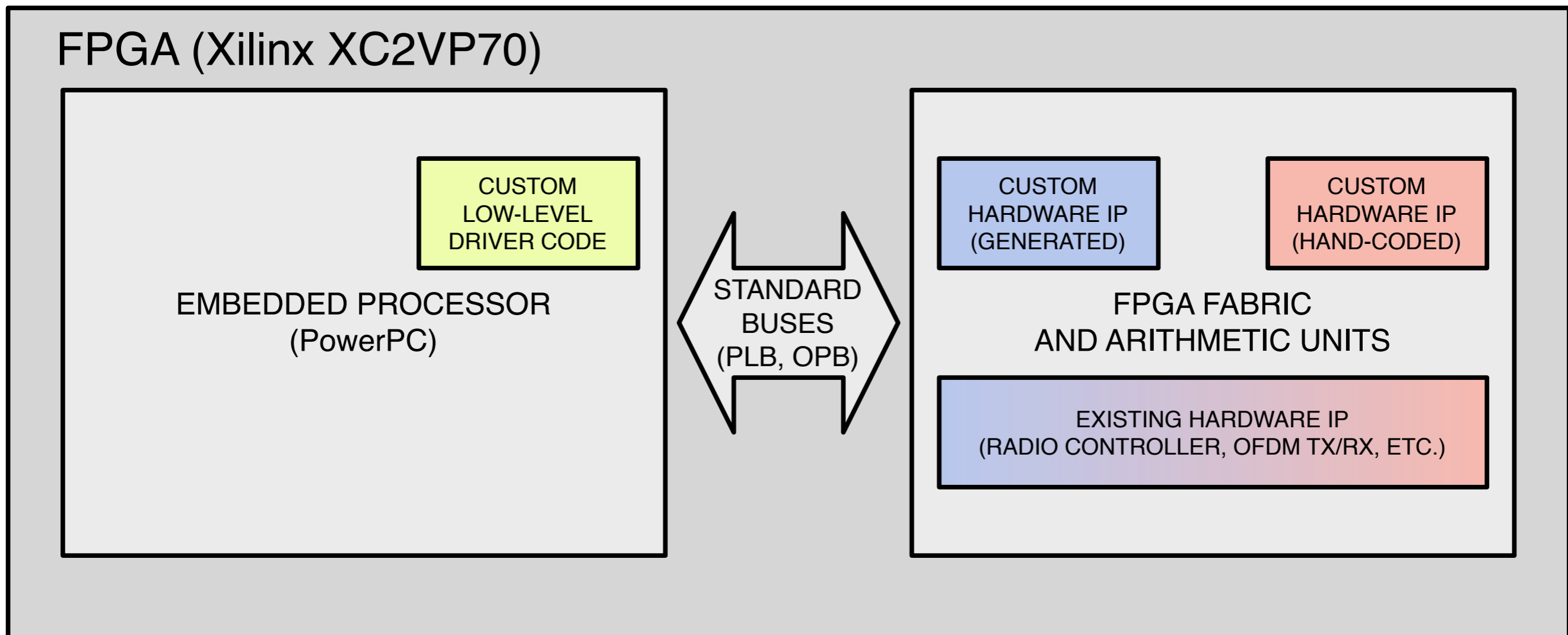
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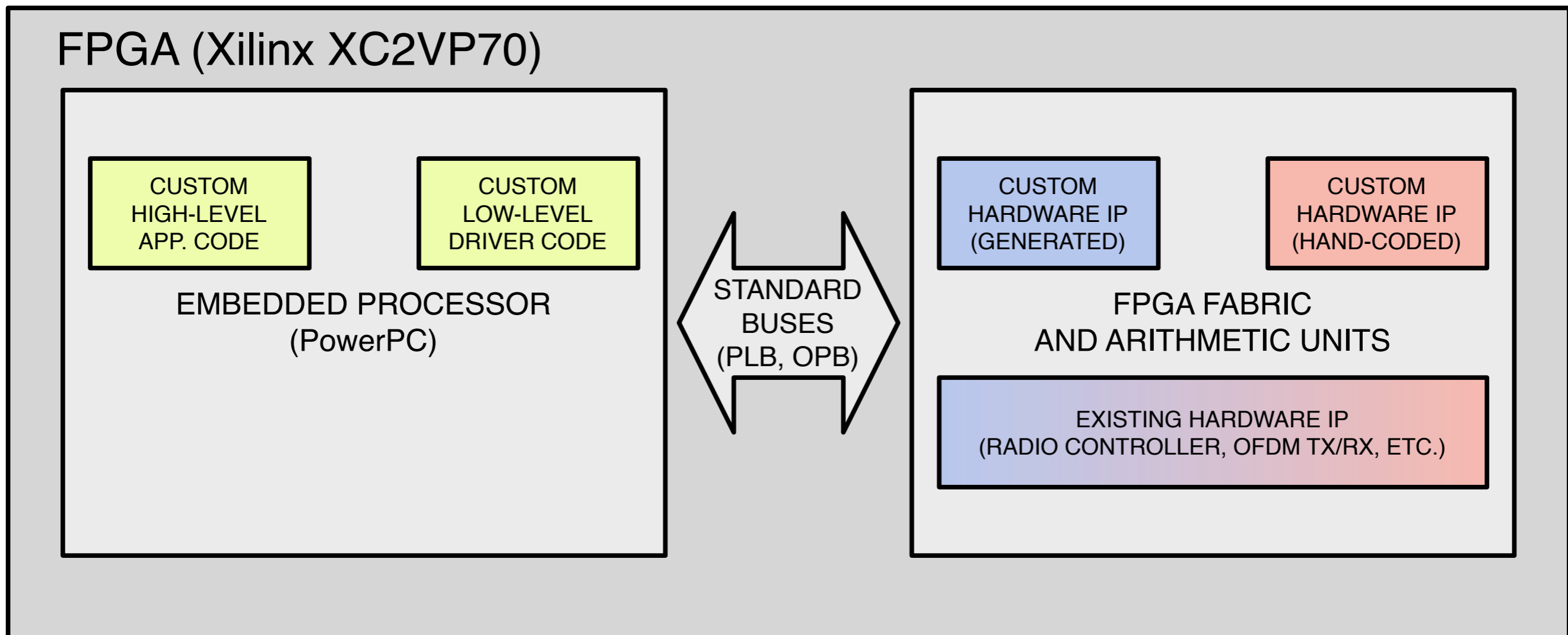
Targeting WARP Hardware

(Understanding the Development Environment)



Targeting WARP Hardware

(Understanding the Development Environment)



Targeting WARP Hardware

(Understanding the Development Environment)

FPGA (Xilinx XC2VP70)

CUSTOM
HIGH-LEVEL
APP. CODE

CUSTOM
LOW-LEVEL
DRIVER CODE

EMBEDDED PROCESSOR
(PowerPC)

WARP/XILINX SUPPORT SOFTWARE
(LIBRARIES, DRIVERS, ETCETERA)

STANDARD
BUSES
(PLB, OPB)

CUSTOM
HARDWARE IP
(GENERATED)

CUSTOM
HARDWARE IP
(HAND-CODED)

FPGA FABRIC
AND ARITHMETIC UNITS

EXISTING HARDWARE IP
(RADIO CONTROLLER, OFDM TX/RX, ETC.)

Targeting WARP Hardware

(MAC/Routing Layer Development Space)

FPGA (Xilinx XC2VP70)

CUSTOM
HIGH-LEVEL
APP. CODE

CUSTOM
LOW-LEVEL
DRIVER CODE

EMBEDDED PROCESSOR
(PowerPC)

WARP/XILINX SUPPORT SOFTWARE
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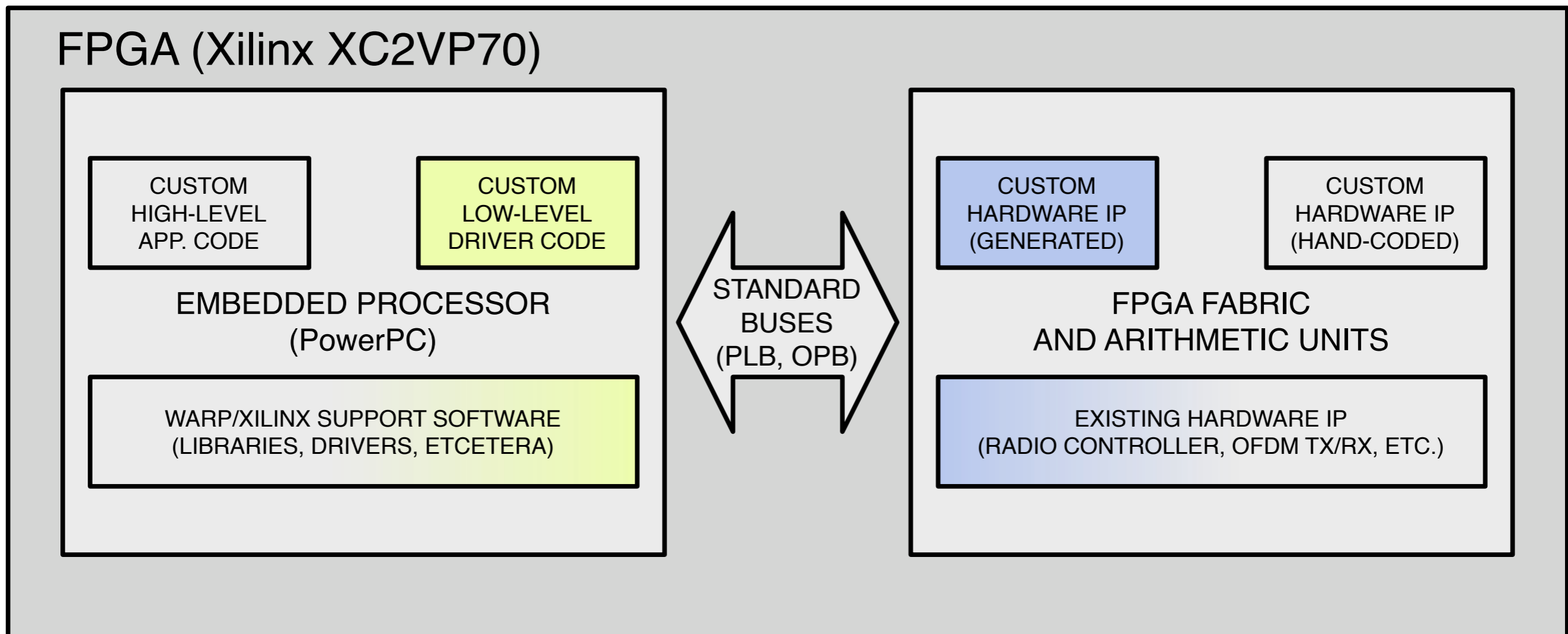
CUSTOM
HARDWARE IP
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FPGA FABRIC
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EXISTING HARDWARE IP
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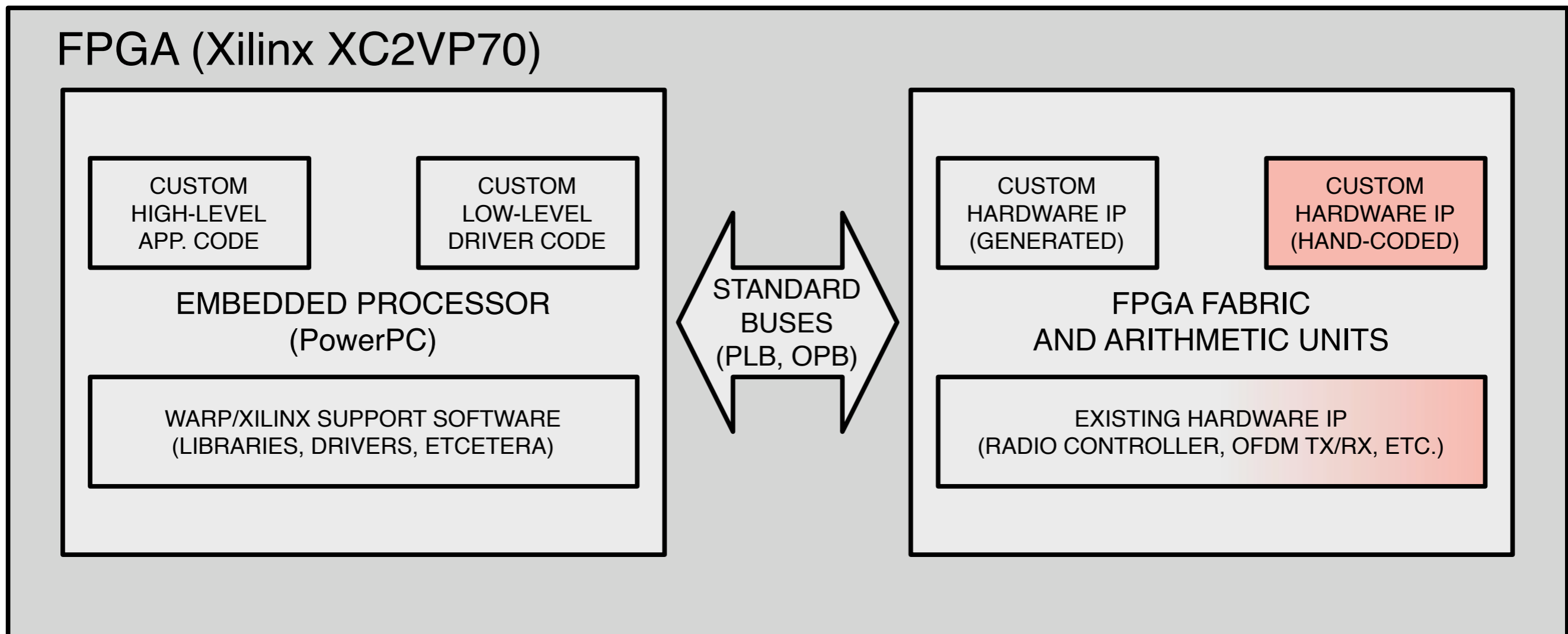
Targeting WARP Hardware

(Physical Layer Development Space)



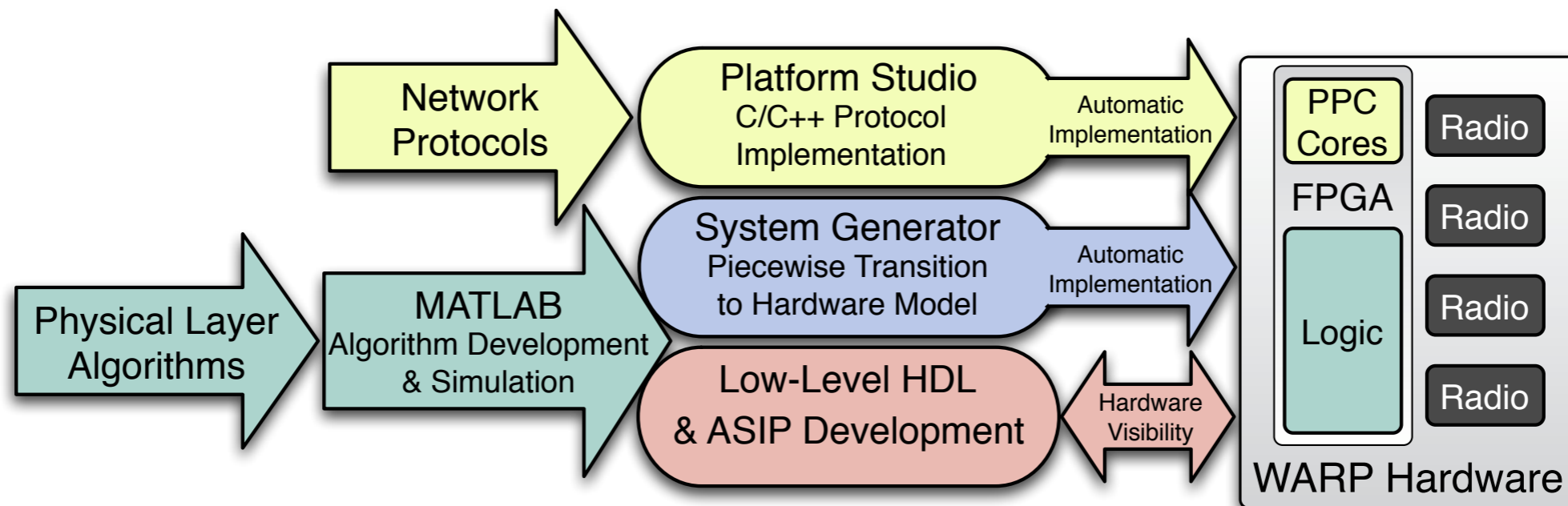
Targeting WARP Hardware

(Architecture Layer Development Space)



Targeting WARP Hardware

(Introducing Development Tools)





Lab 1: EDK Intro

- Intro to Xilinx Platform Studio
 - Building a simple hardware platform
 - Interacting with the WARP hardware