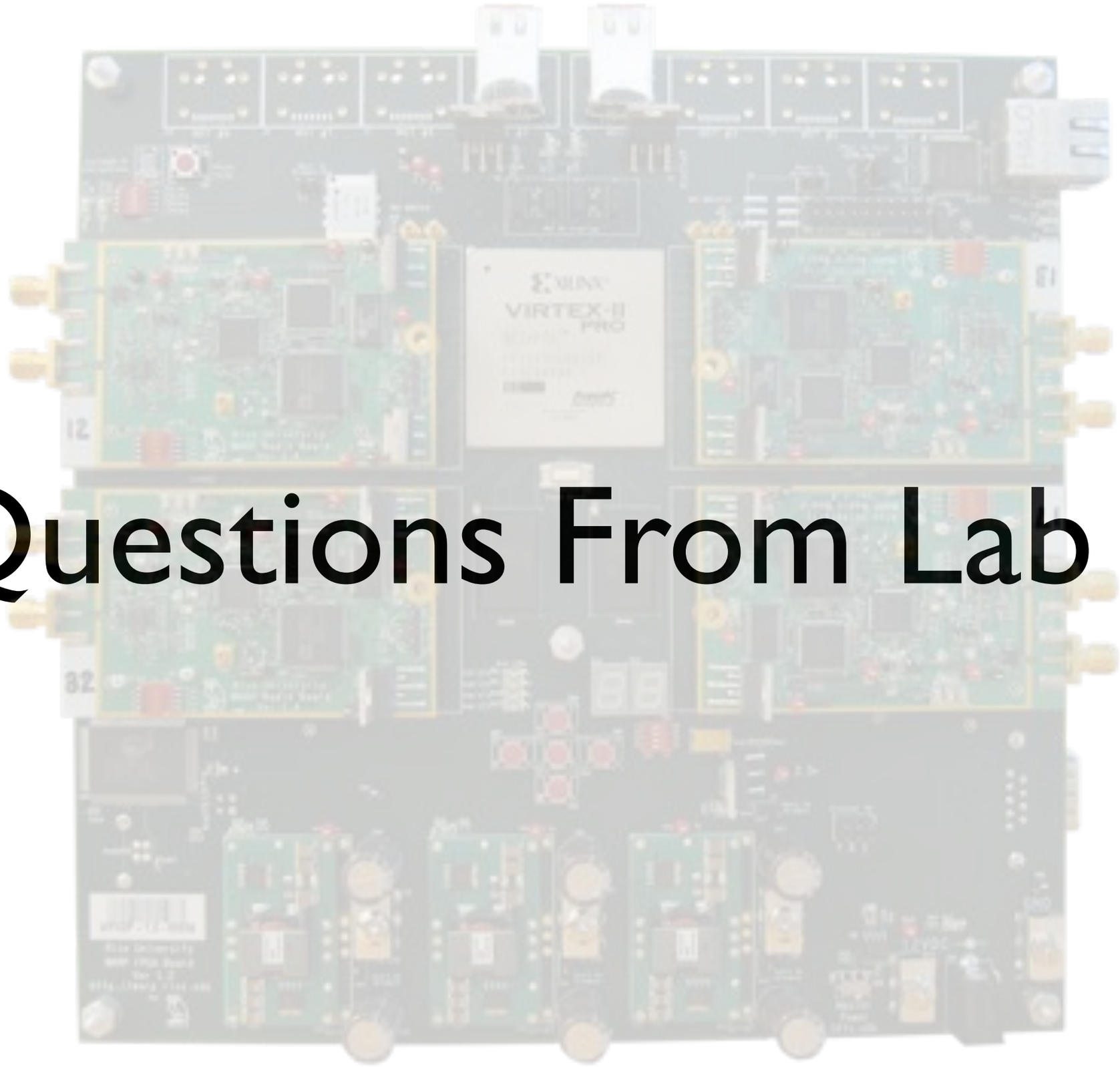
WARP: Hardware

Sid Gupta & Patrick Murphy

WARP Workshop
Rice University
March 29, 2010

warp.rice.edu

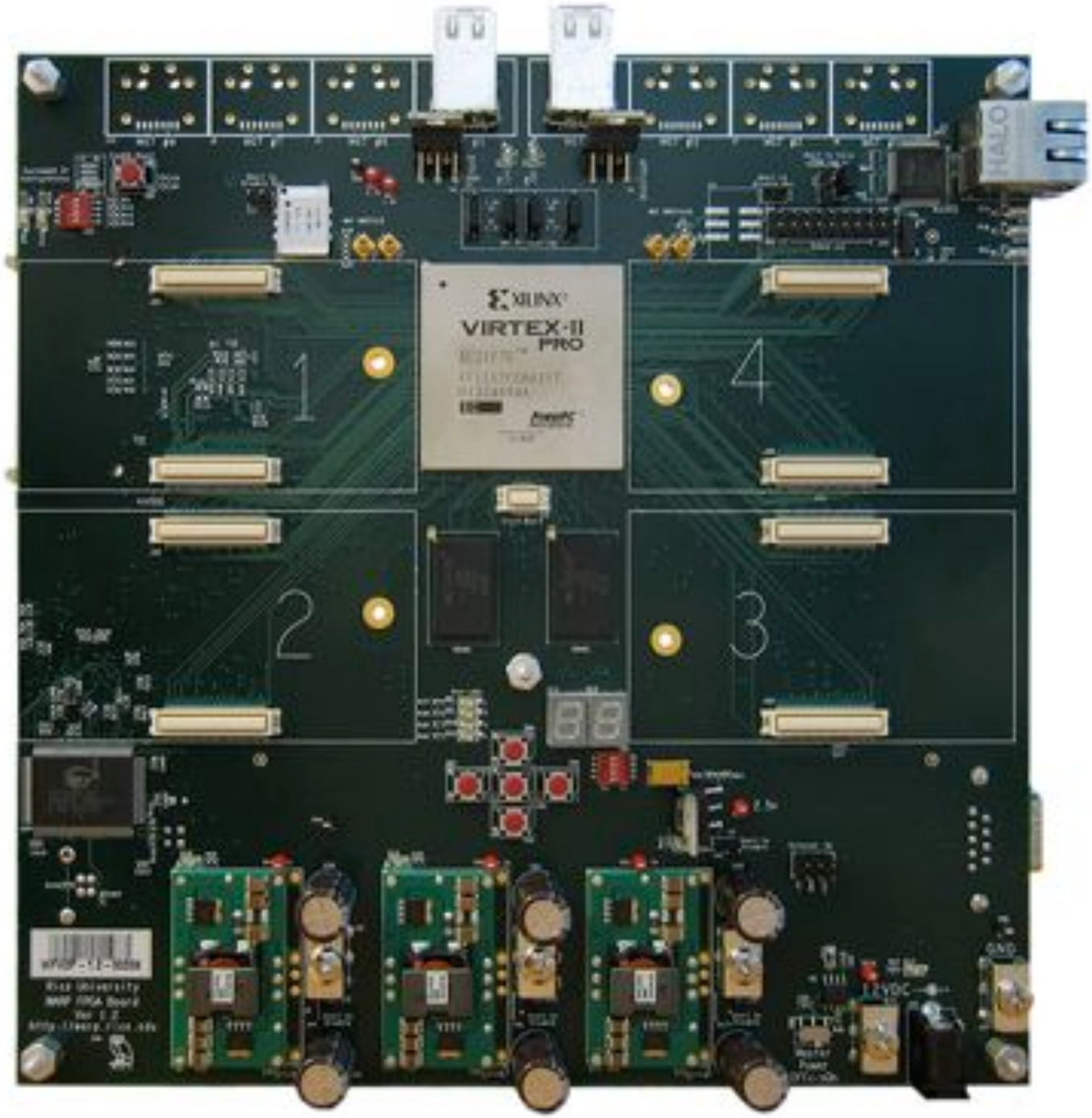


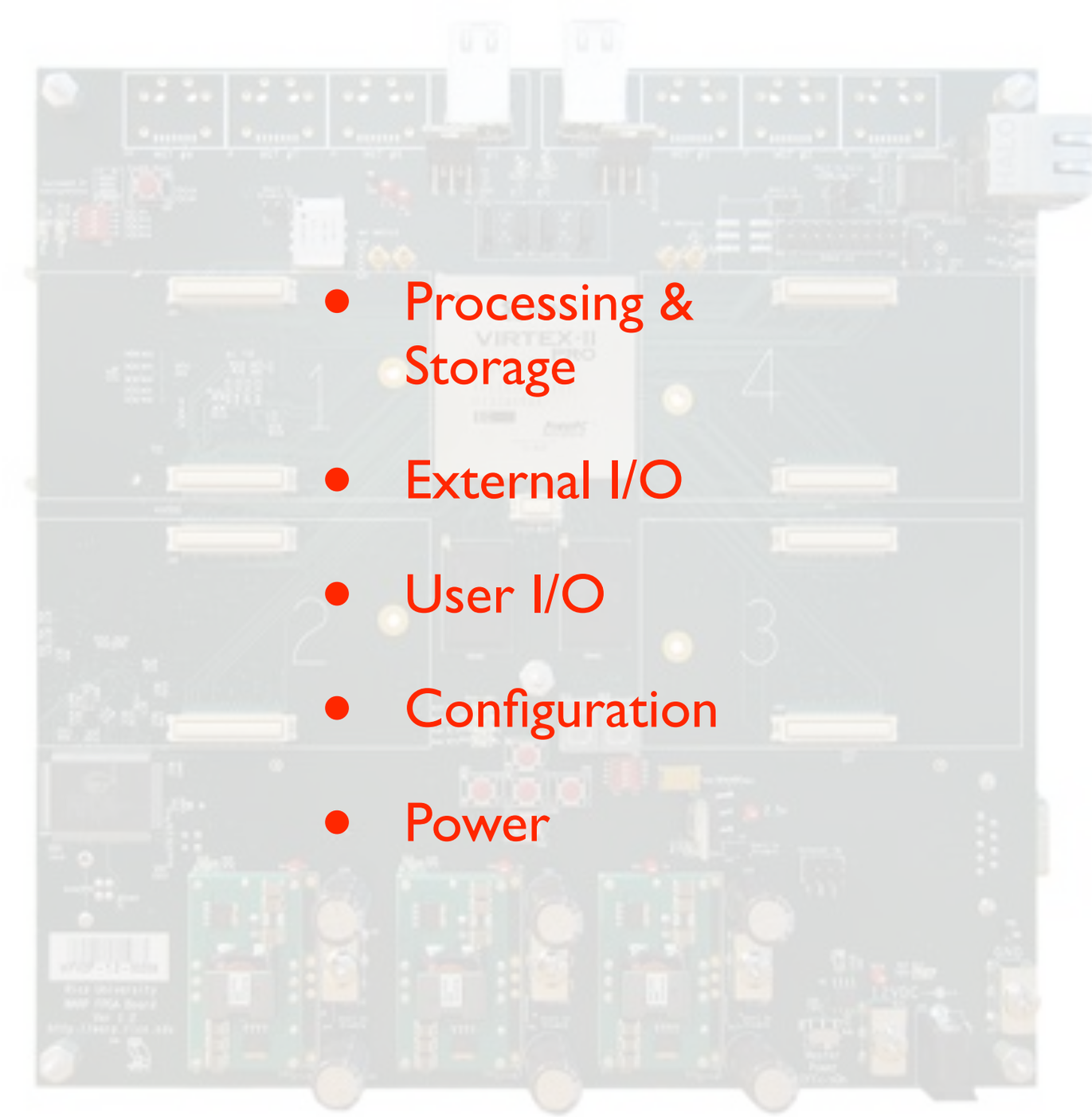
Questions From Lab1?

WARP Hardware

- WARP Hardware Components
  - FPGA Board
  - Radio Board
  - Clock Board
- FPGA Architecture
- Xilinx Platform Studio


WARP
3
WARP
VIRTEX-II
PRO


XILINX
VIRTEX-II
PRO
1
2
3
4



- Processing & Storage
- External I/O
- User I/O
- Configuration
- Power

Xilinx XC2VP70 FPGA

- Extensive I/O & Logic Resources
- Embedded CPUs
- Extremely Flexible
- Powerful and Easy-to-Use Development Tools

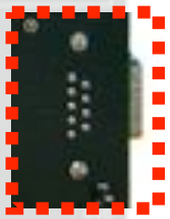
4 MByte Onboard SRAM

- Augments FPGA's Internal RAM Resources
- Usable as Instruction and/or Data Memory
- Two ICs, Each 512K x 32

Multi-Gigabit Transceivers

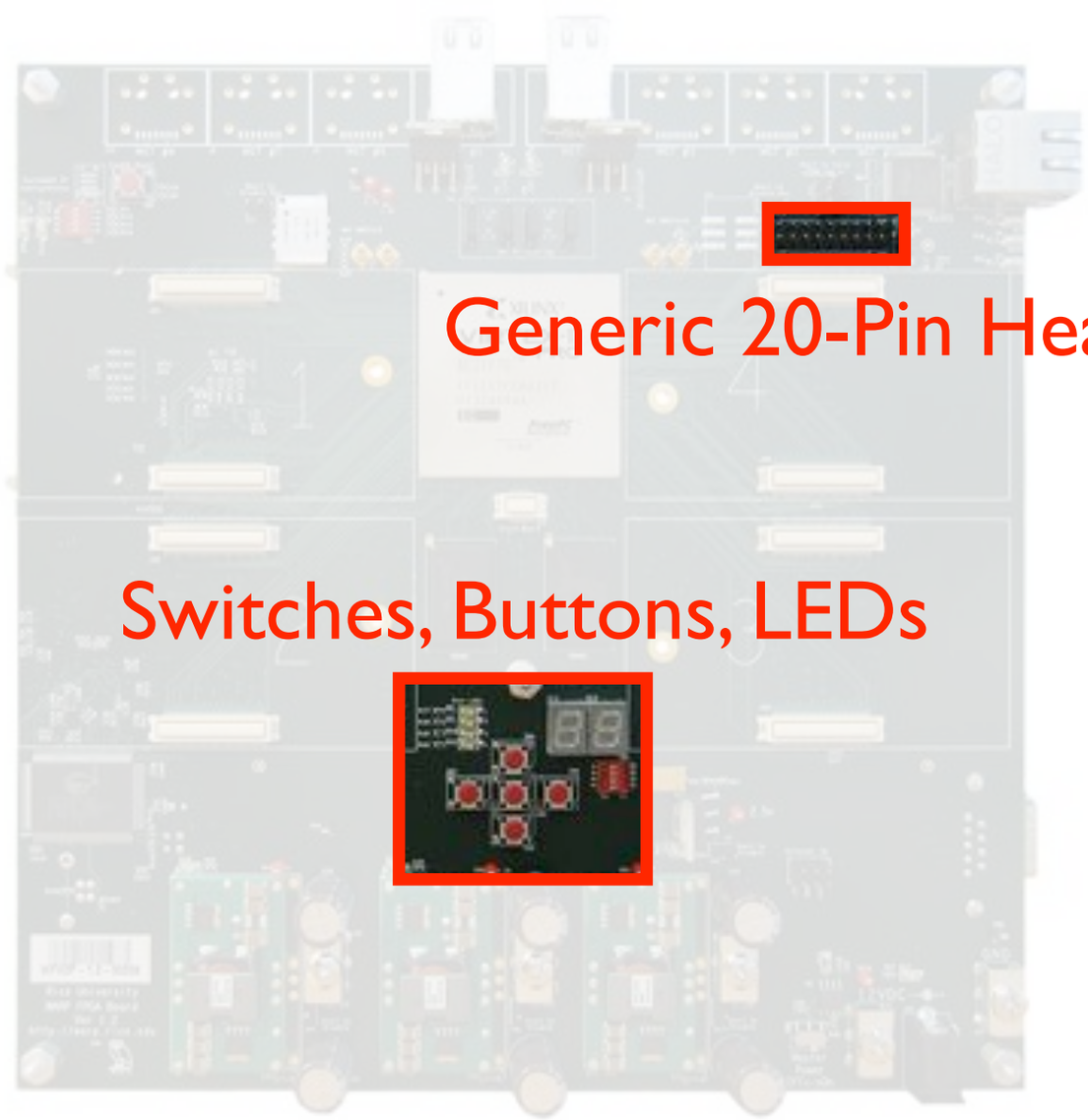
Ethernet Port

Serial Port



Daughtercard Connectors

- Provide Expanded Functionality via Custom Daughtercards
- Connect to FPGA Through General Purpose Digital I/Os
- Protocol Defined By Logic and Software Residing in FPGA
- Supports Radios, Video Cards, A/D & D/A Cards, Others



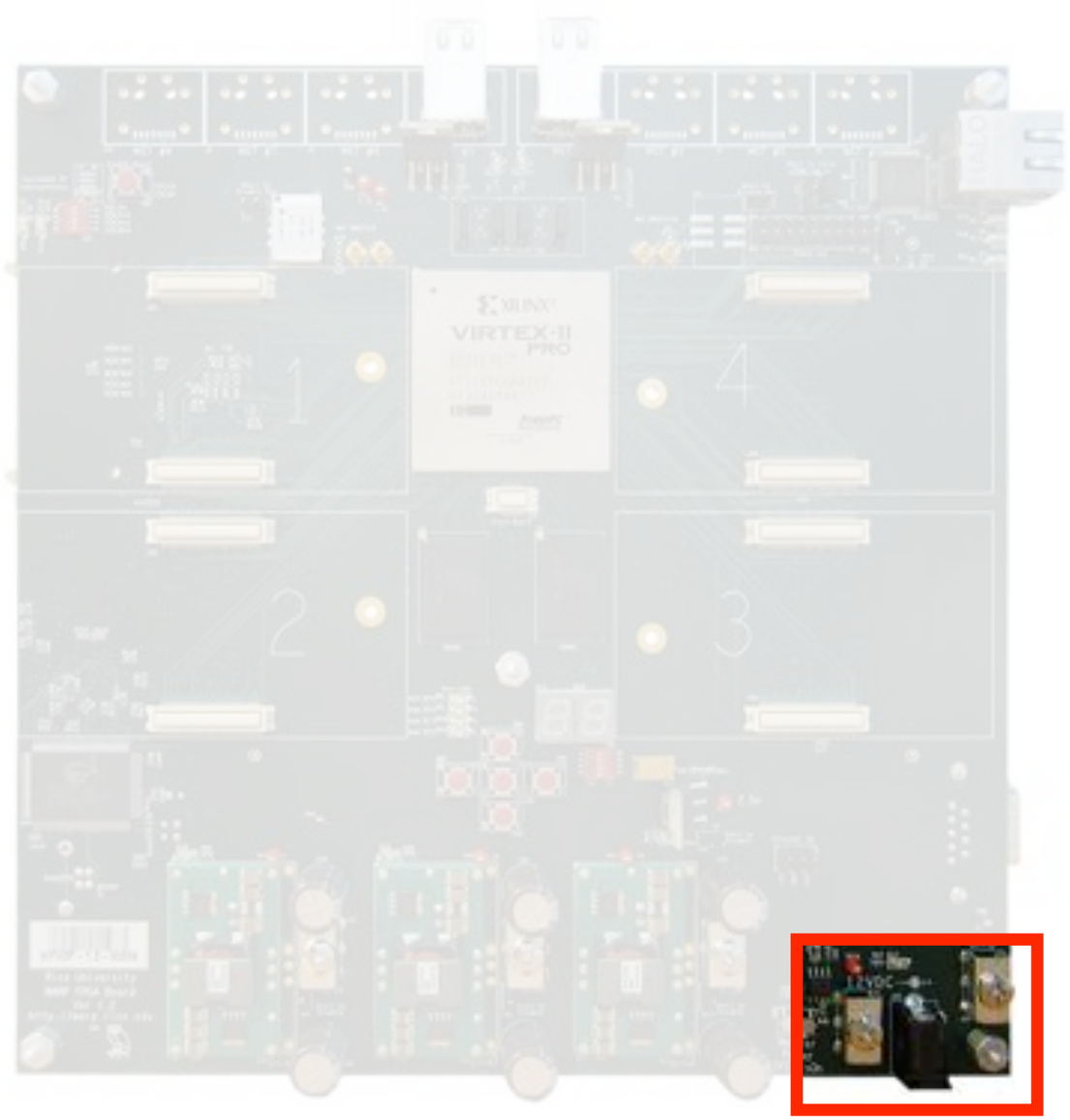
Generic 20-Pin Header

Switches, Buttons, LEDs

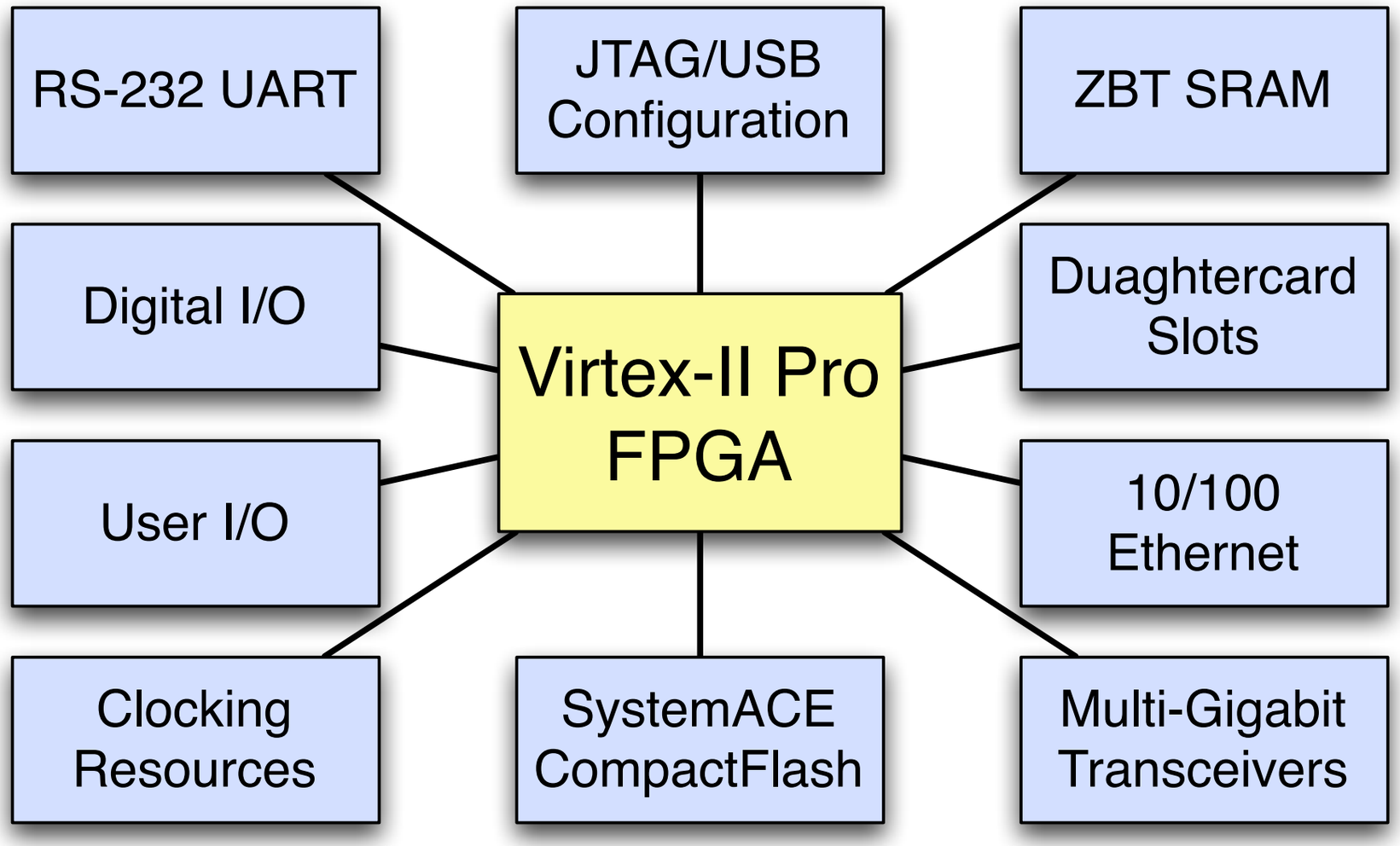
Compact Flash Slot

JTAG Header

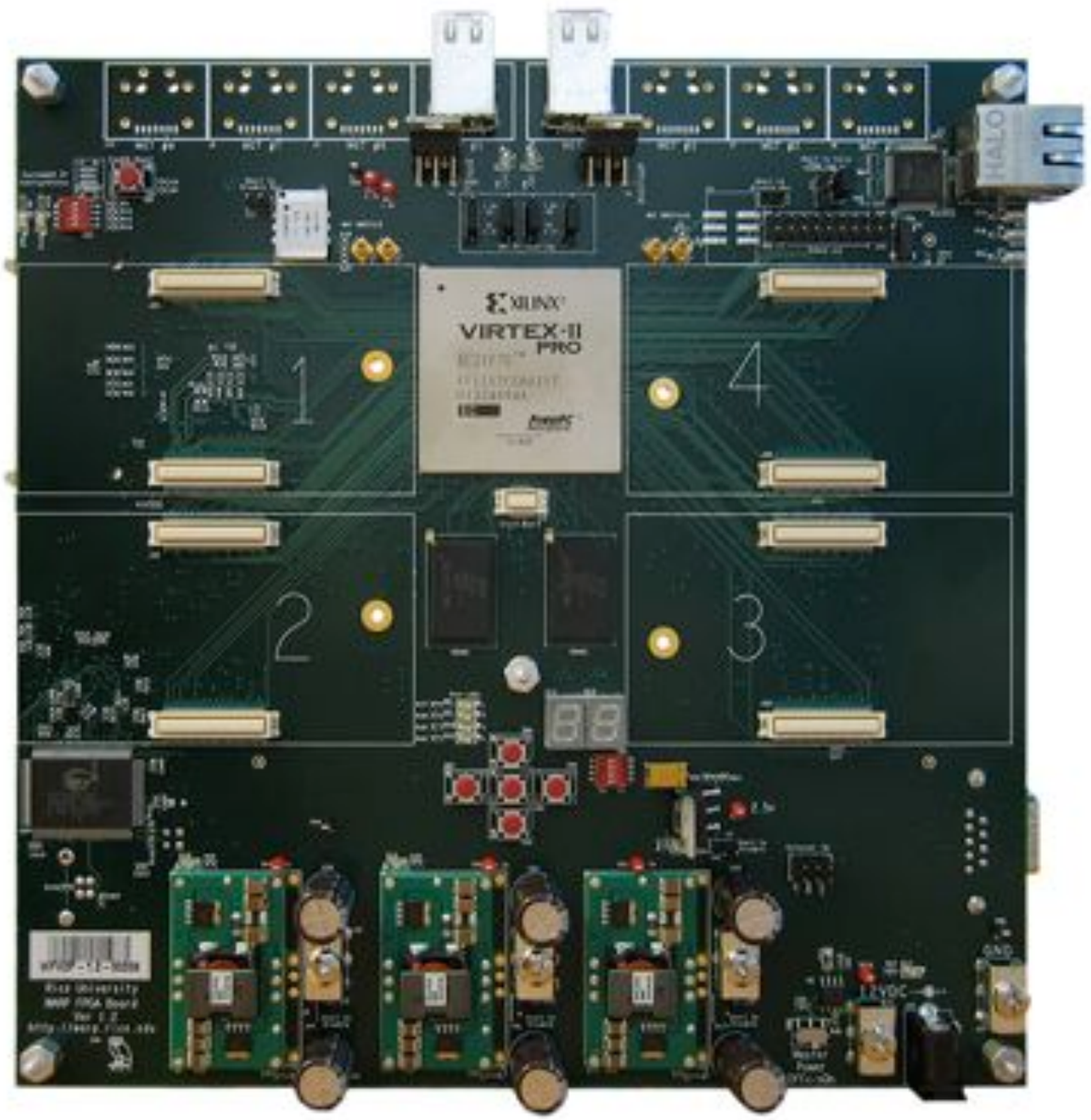
USB Connector

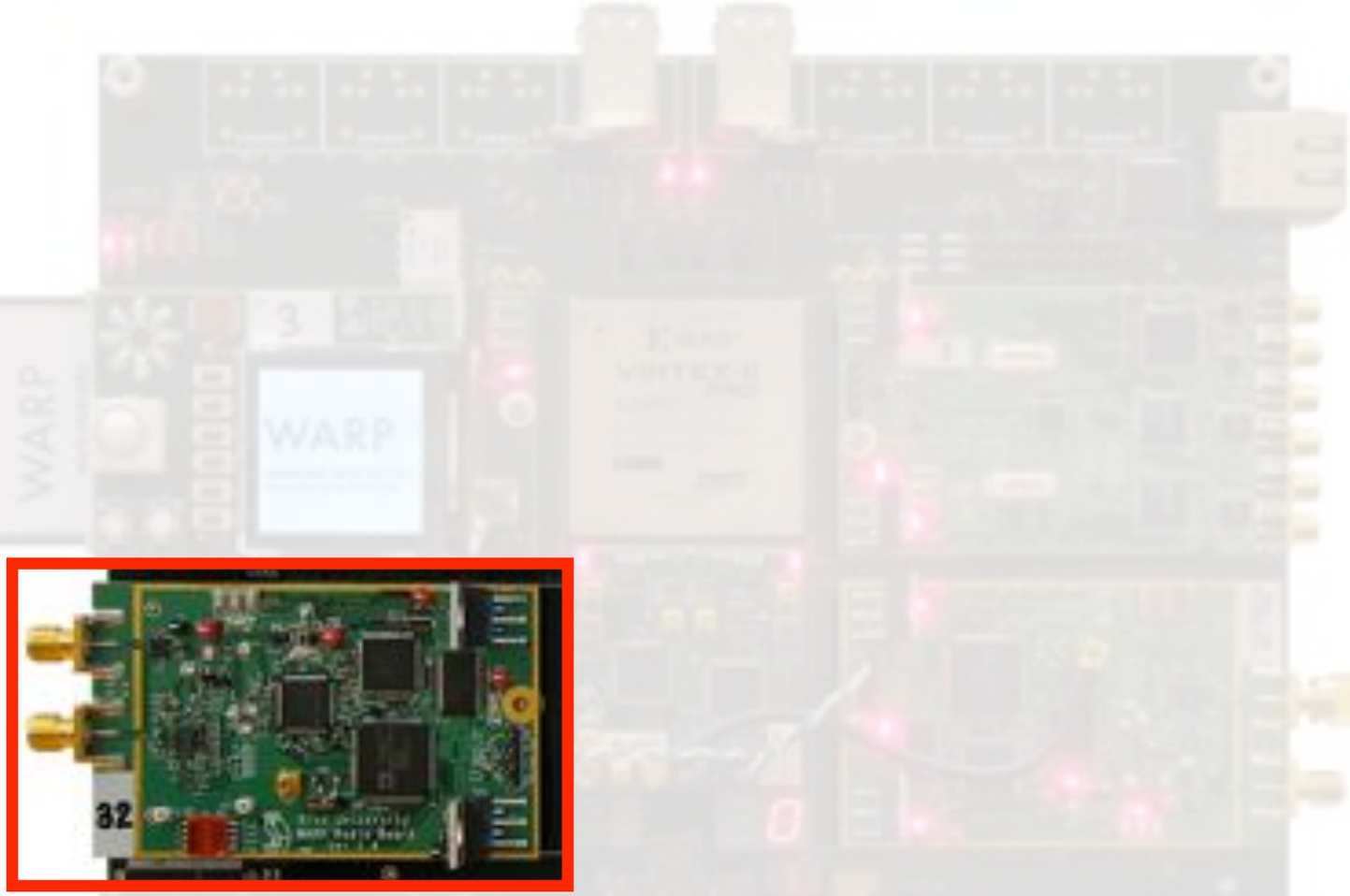


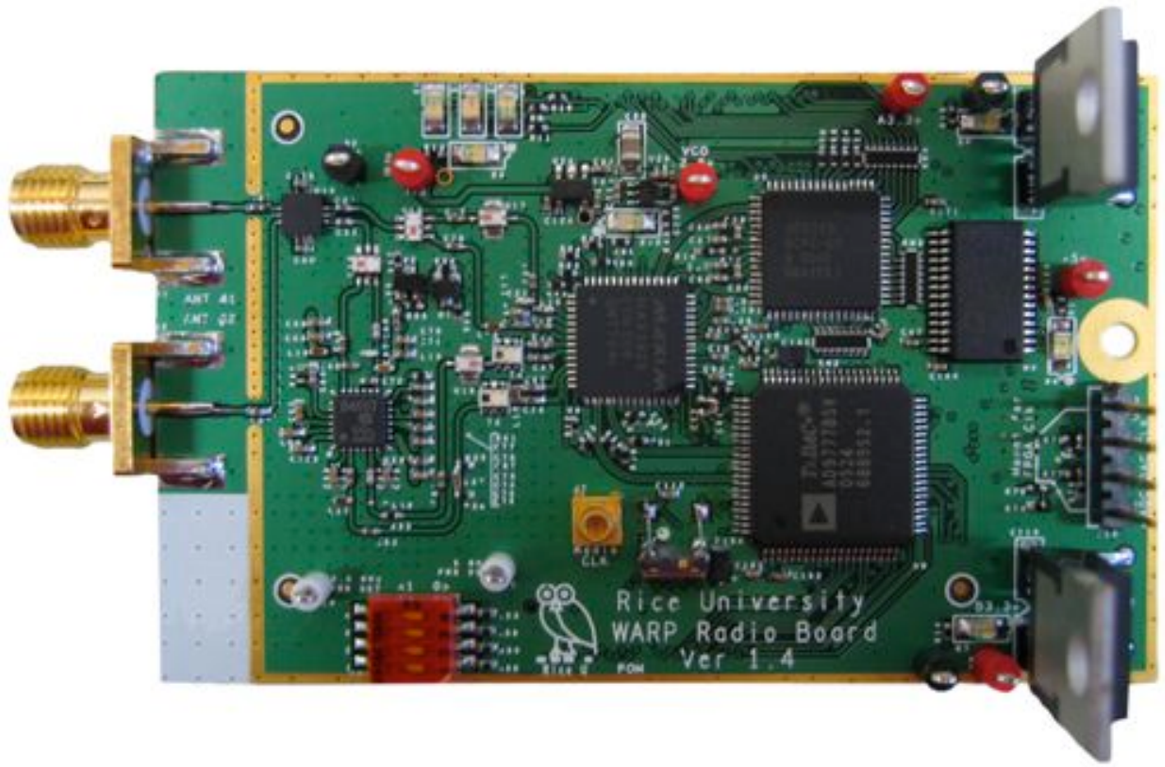
12V DC Voltage Input

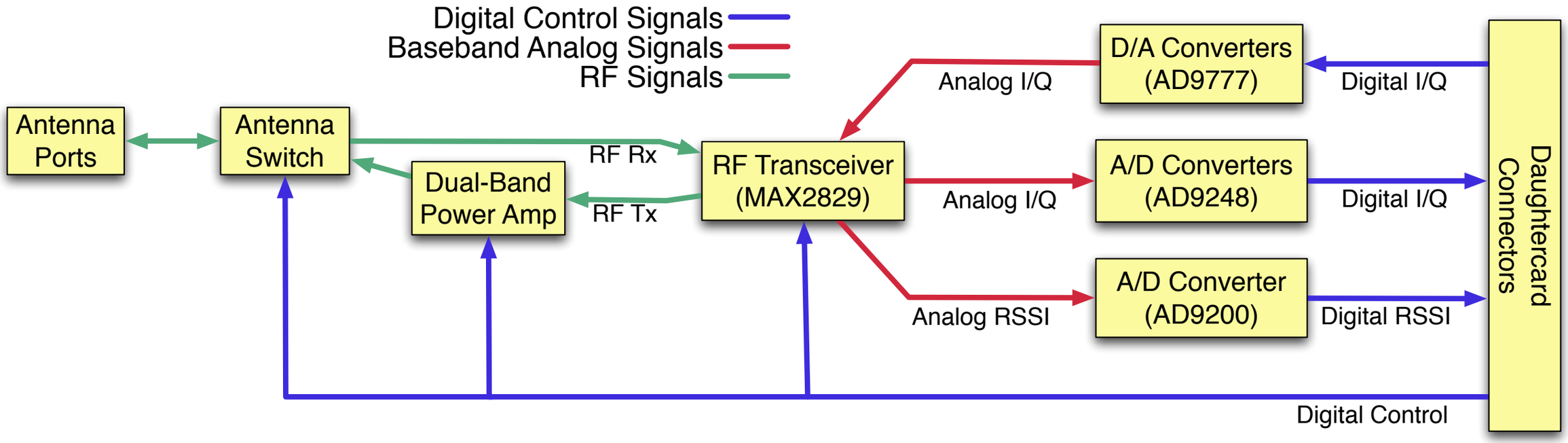

RS-232 UART
JTAG/USB Configuration
ZBT SRAM
Digital I/O
Duaghtercard Slots
Virtex-II Pro FPGA
User I/O
10/100 Ethernet
Clocking Resources
SystemACE CompactFlash
Multi-Gigabit Transceivers

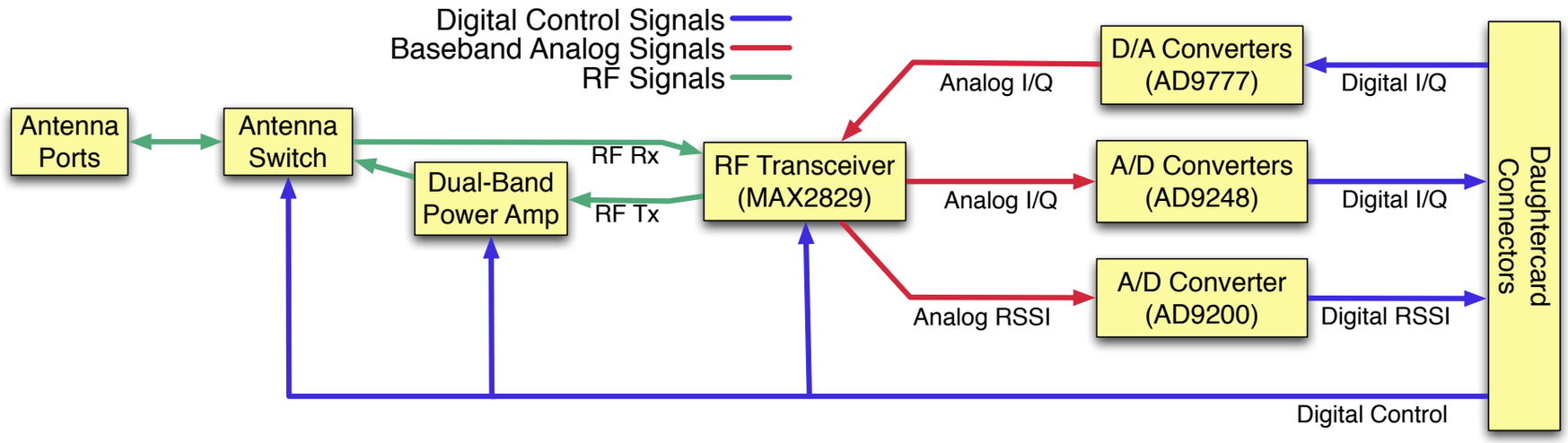
Questions?



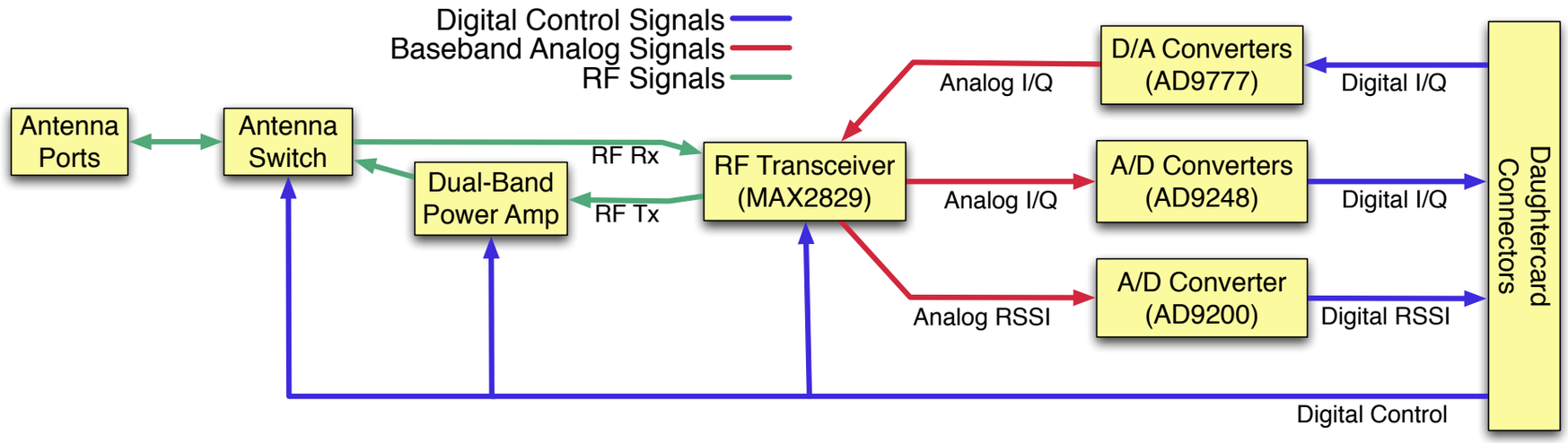



Rice University
WARP Radio Board
Ver 1.4


Digital Control Signals
Baseband Analog Signals
RF Signals
Antenna Ports
Antenna Switch
Dual-Band Power Amp
RF Rx
RF Tx
RF Transceiver (MAX2829)
Analog I/Q
D/A Converters (AD9777)
Digital I/Q
A/D Converters (AD9248)
Analog I/Q
Digital I/Q
A/D Converter (AD9200)
Analog RSSI
Digital RSSI
Digital Control
Daughtercard Connectors



D/A Converters
AD9777


Digital Control Signals
Baseband Analog Signals
RF Signals
Antenna Ports
Antenna Switch
Dual-Band Power Amp
RF Rx
RF Tx
RF Transceiver (MAX2829)
Analog I/Q
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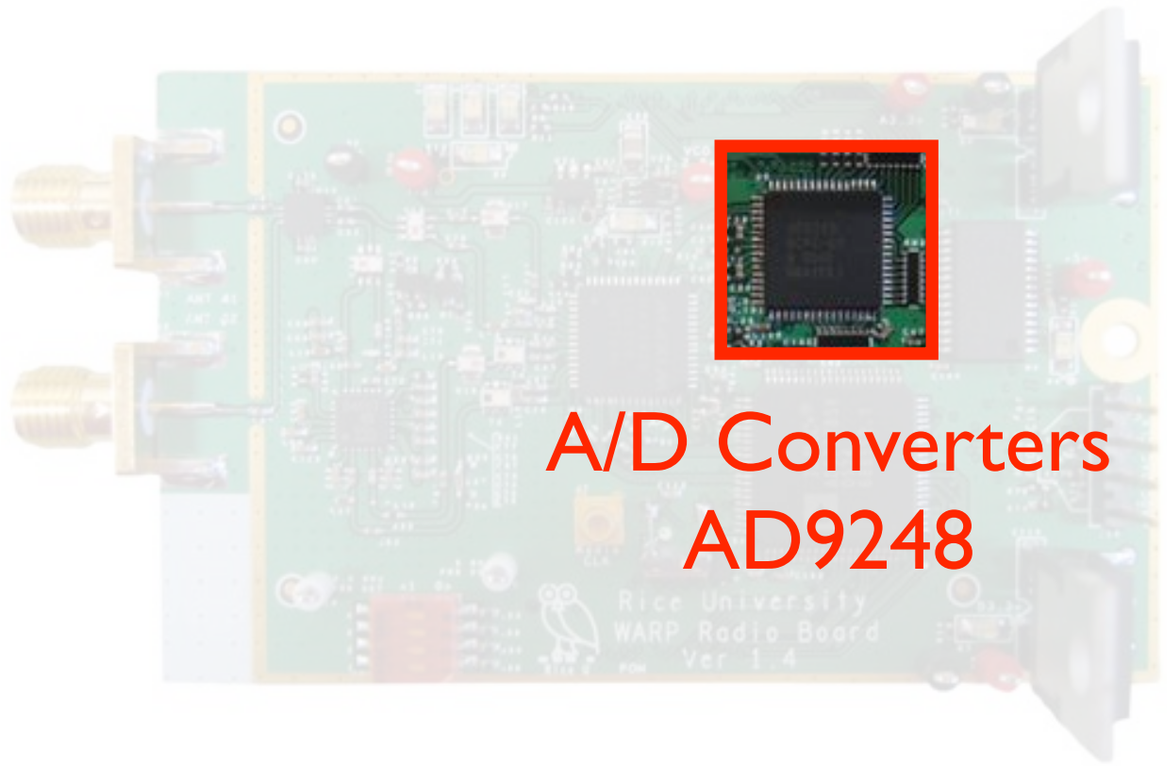
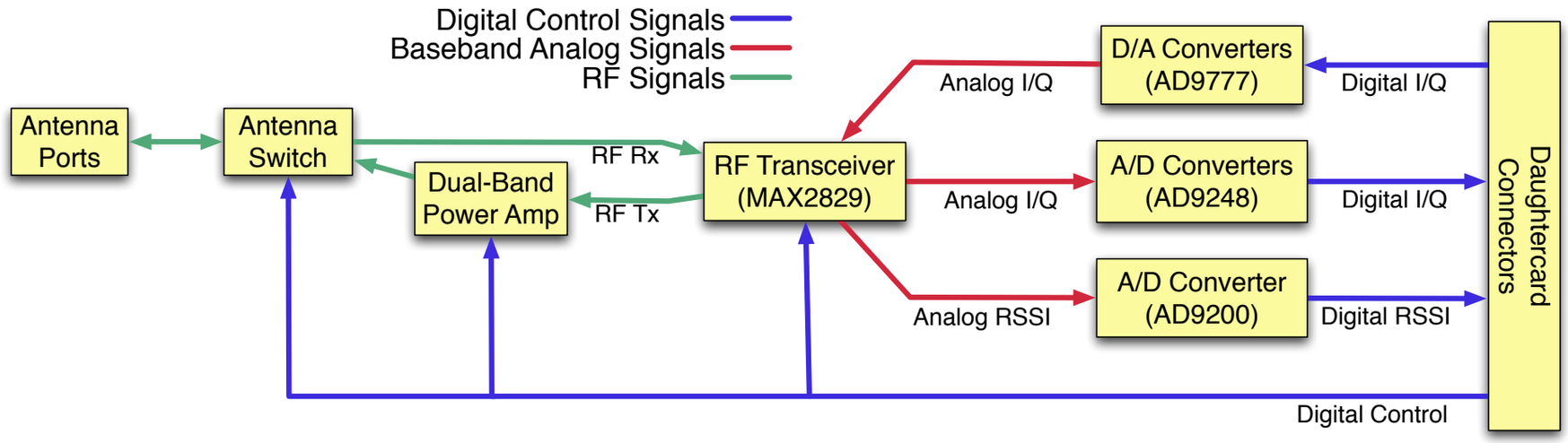
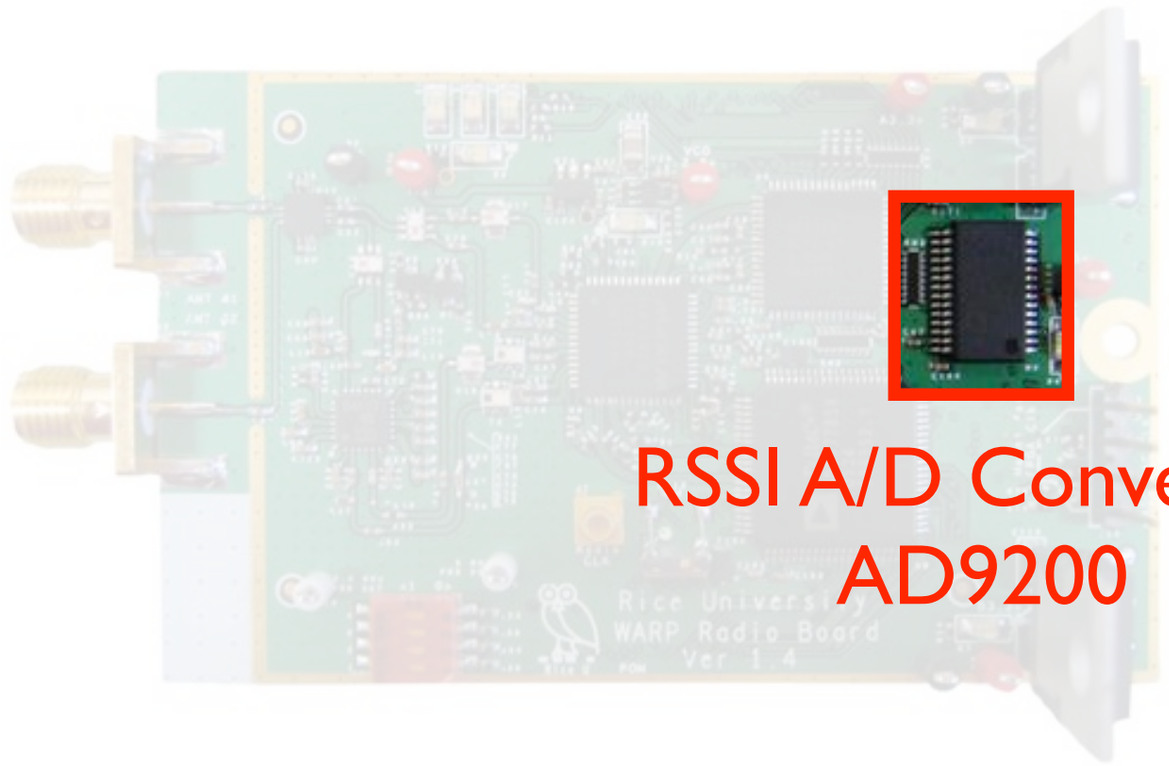
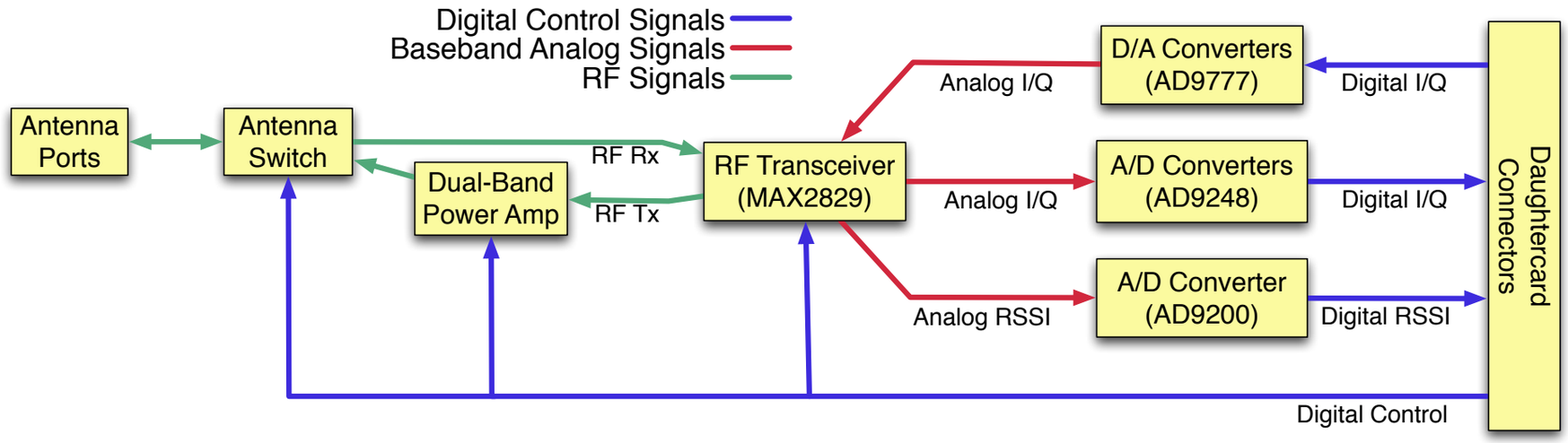
Digital I/Q
Digital I/Q
Digital RSSI
Daughtercard Connectors
Digital Control


A/D Converters
AD9248





RSSI A/D Converter
AD9200



MAX2829

- Dual-Band Operation : 2.4 GHz and 5 GHz
- Direct Conversion Between RF and Baseband
- 40 MHz Bandwidth Independent of Carrier Frequency

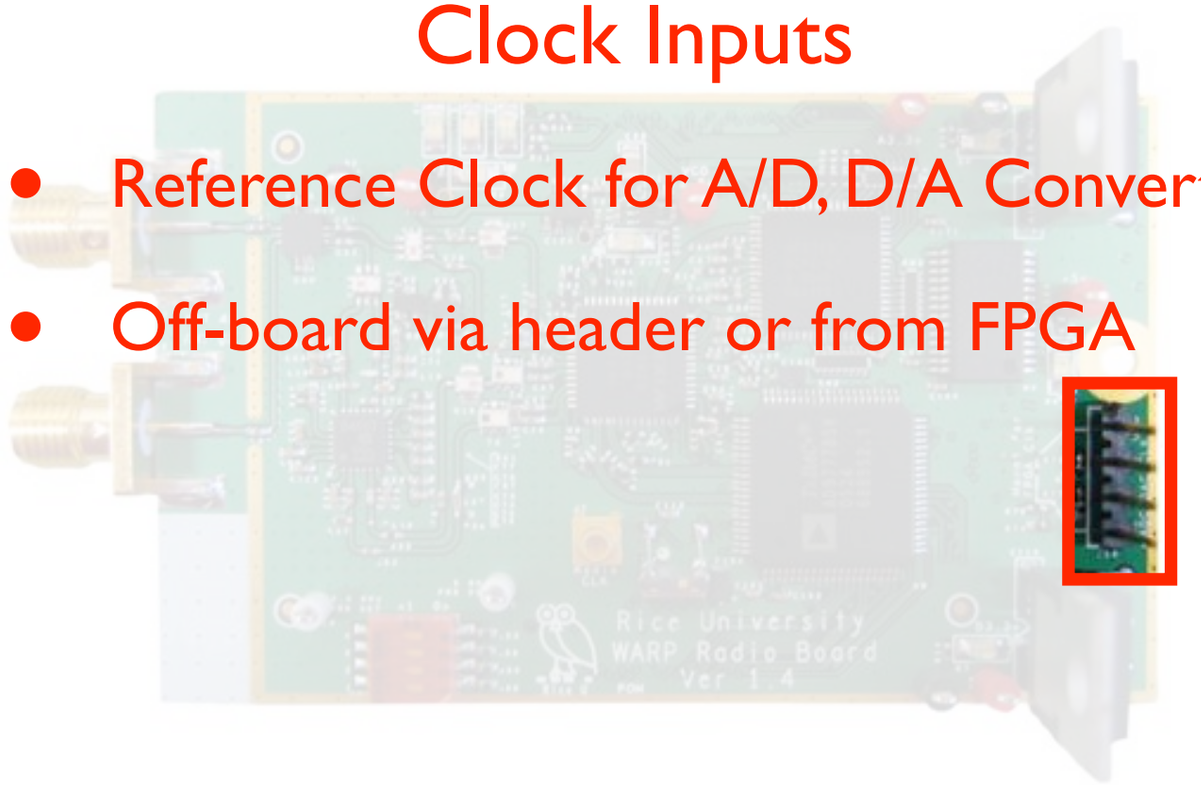
Clock Inputs

- Reference Frequency Input for Radio's Up/Down Conversion
- May Be Supplied Externally via MMCX Connector

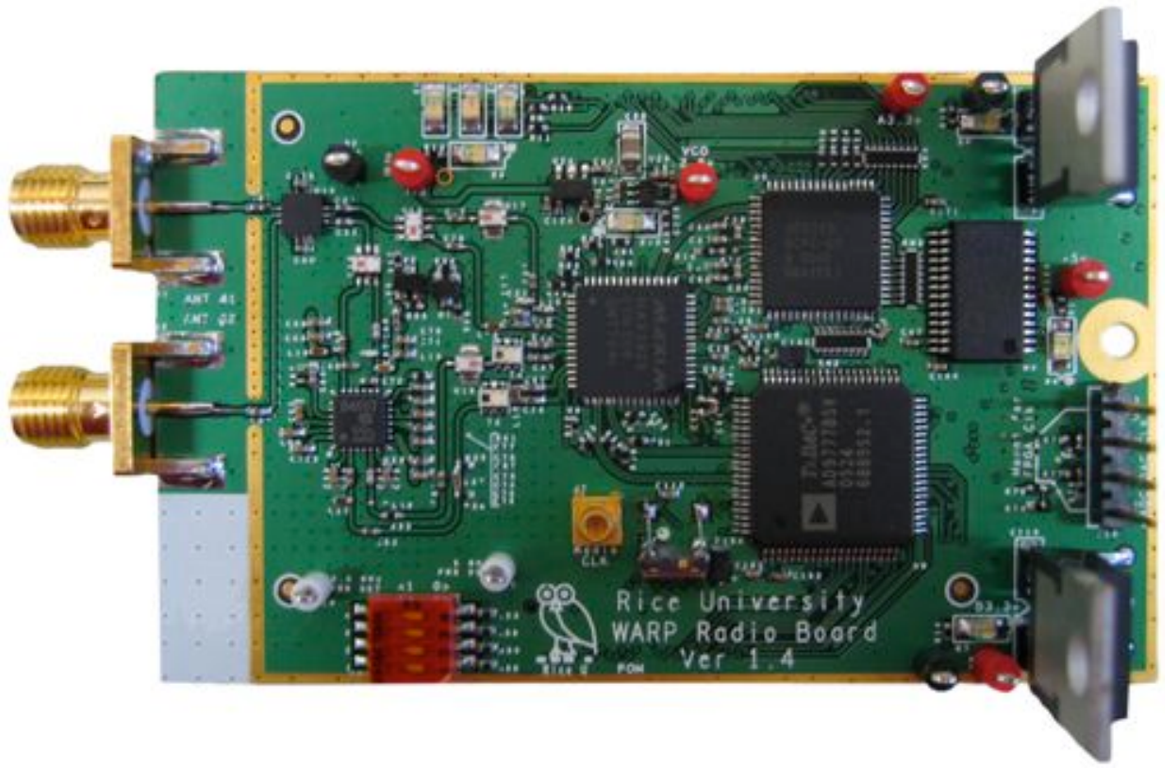
- May Be Supplied Locally via Onboard Oscillator
- Low-Frequency Signal is Up-Converted by Radio IC

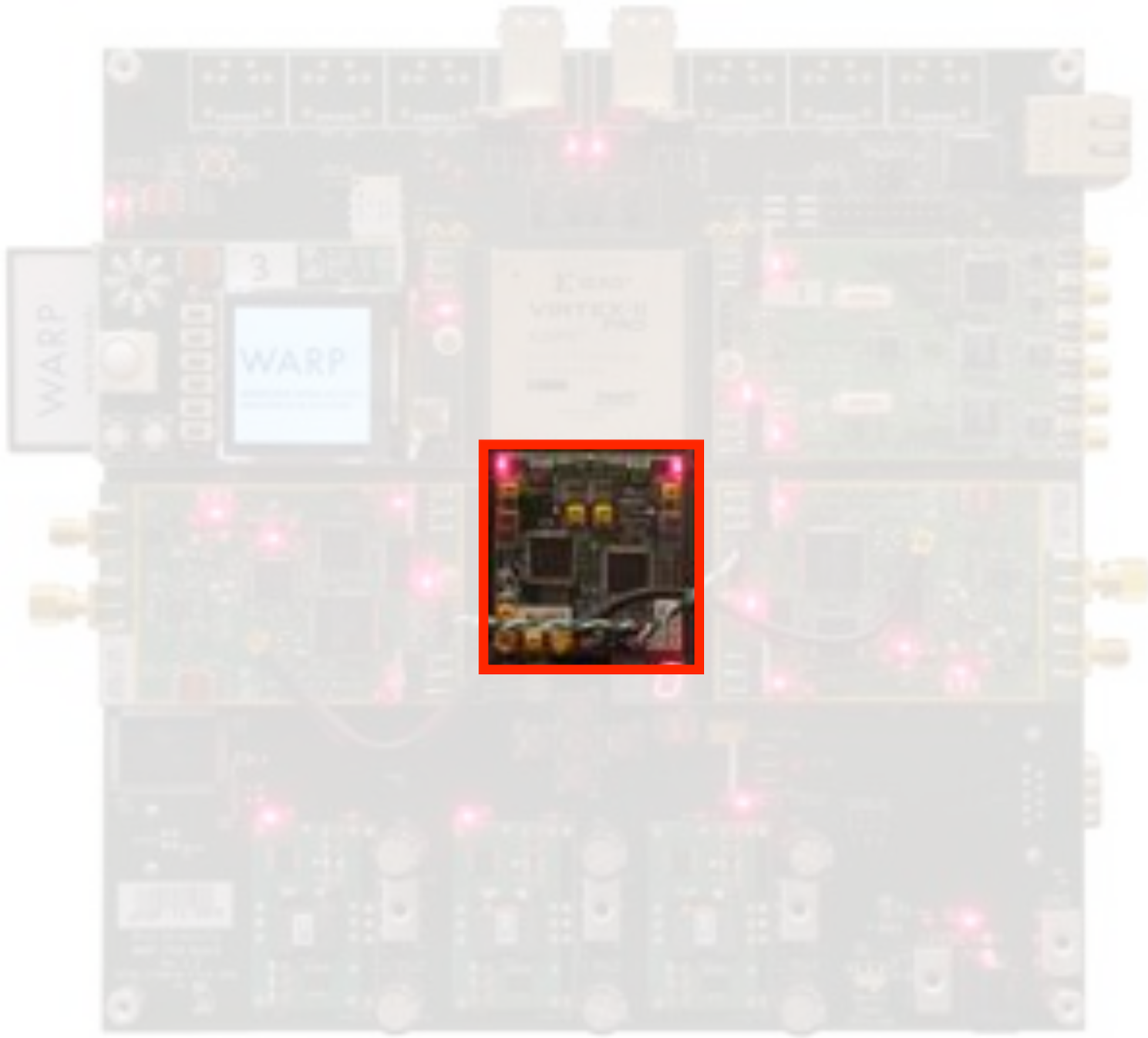
Clock Inputs

- Reference Clock for A/D, D/A Converters
- Off-board via header or from FPGA



Questions?






WARP
Clock
Board
Ver 1.1
CJC/SG
WX-a-00033

Radio Reference Clock

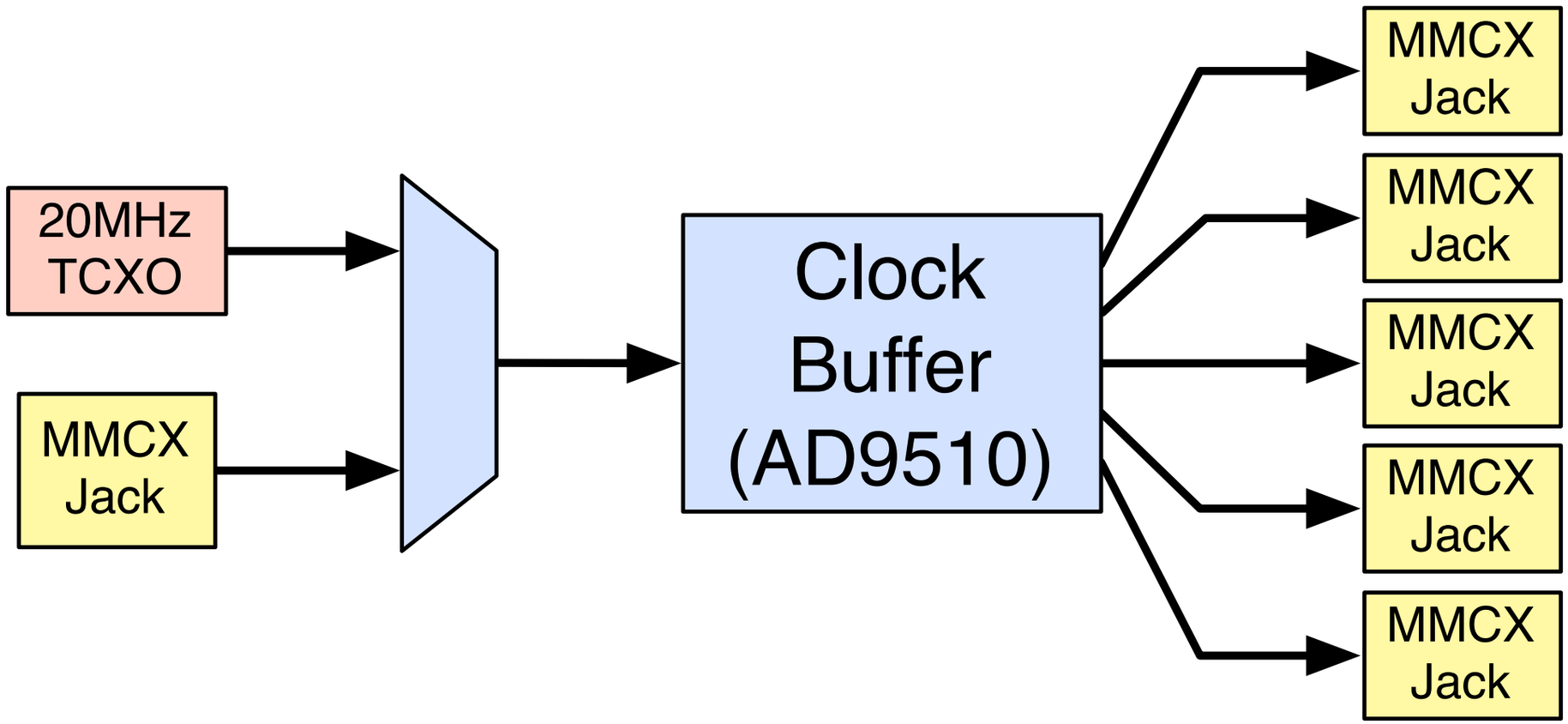
- 20 MHz Output
- High-Precision Oscillator

External Input

Forwarding Output

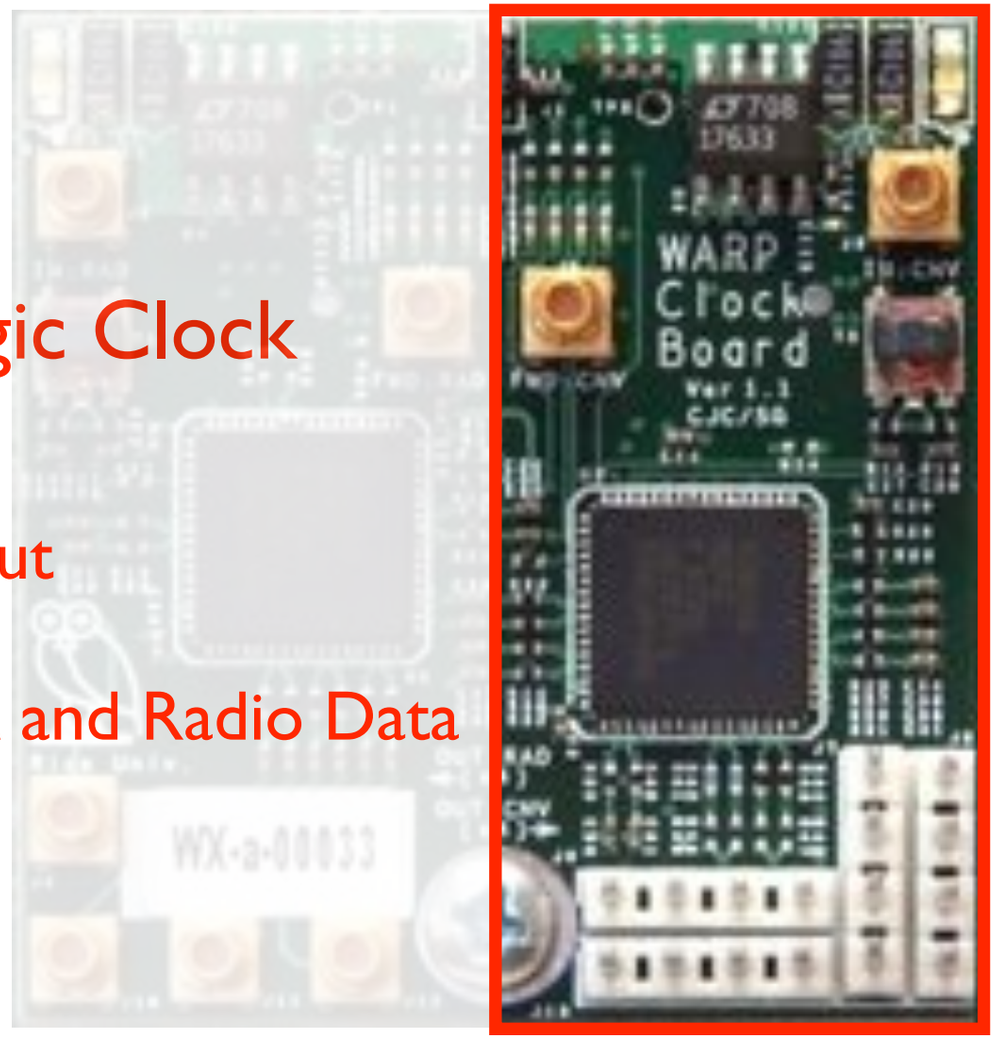
Four MMCX
Daughtercard Outputs

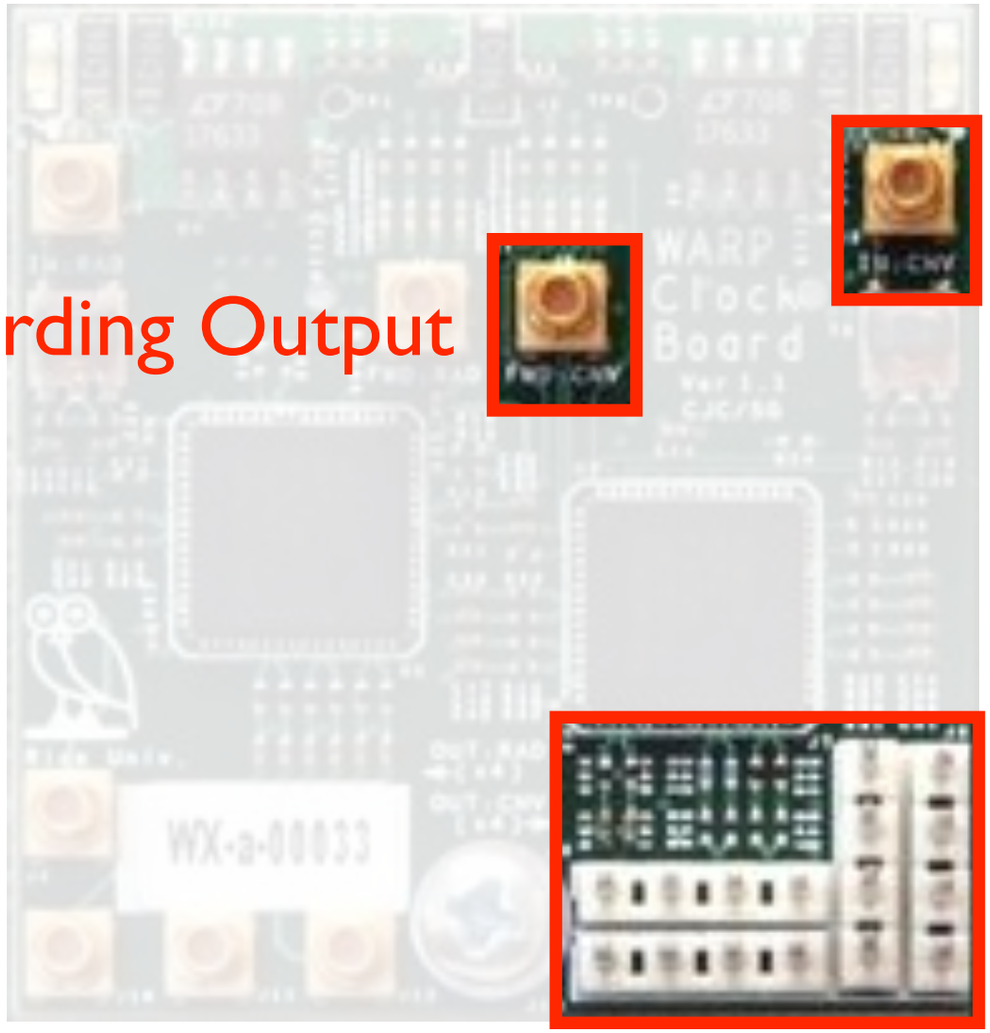
Radio Clock


20MHz
TCXO
MMCX
Jack
Clock
Buffer
(AD9510)
MMCX
Jack
MMCX
Jack
MMCX
Jack
MMCX
Jack
MMCX
Jack

FPGA Logic Clock

- 40MHz Output
- Clocks FPGA and Radio Data



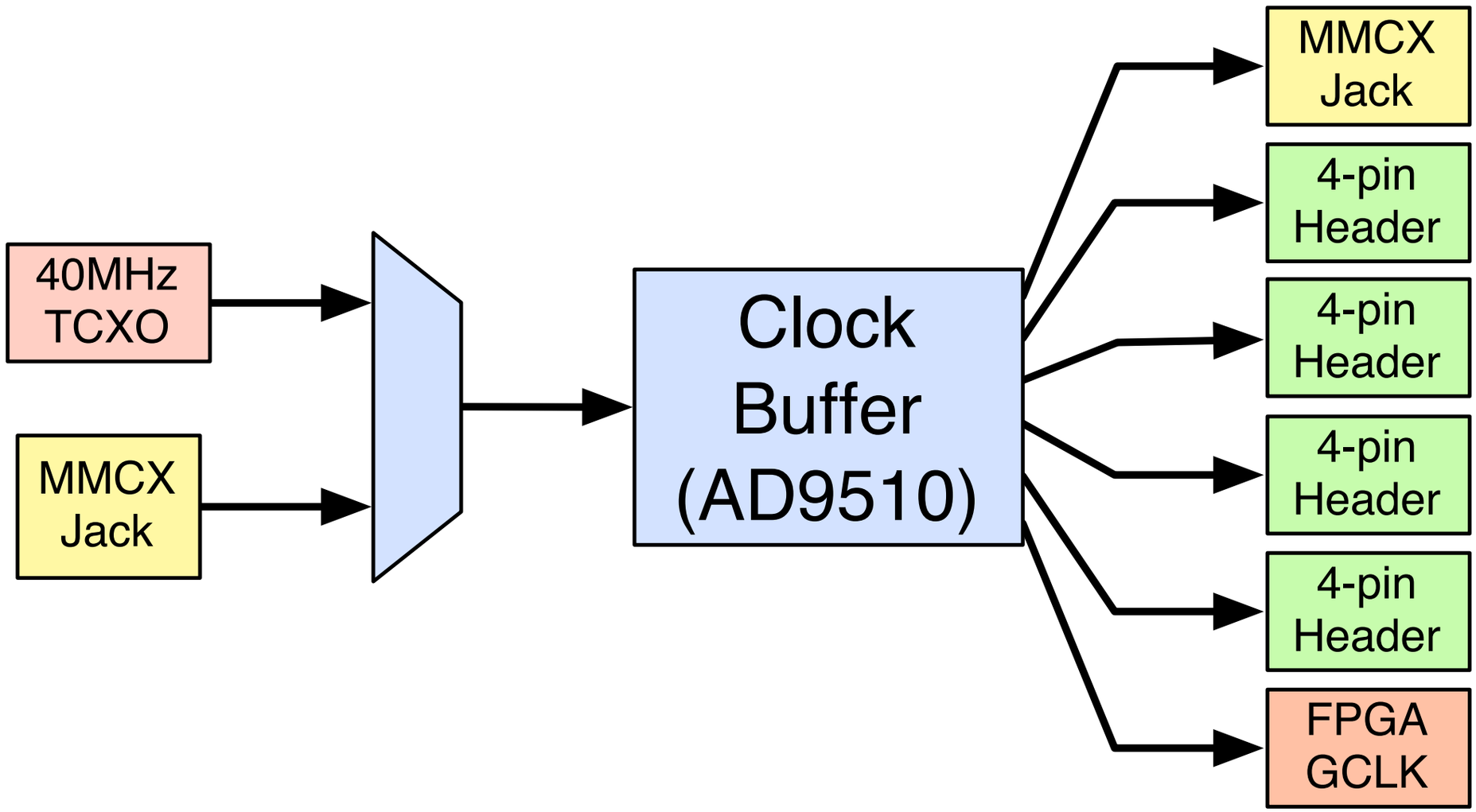


Forwarding Output

External Input

Four Twisted-Pair
Daughtercard Outputs

Logic Clock


40MHz
TCXO
MMCX
Jack
Clock
Buffer
(AD9510)
MMCX
Jack
4-pin
Header
4-pin
Header
4-pin
Header
4-pin
Header
FPGA
GCLK

Questions?

http://warp.rice.edu/trac

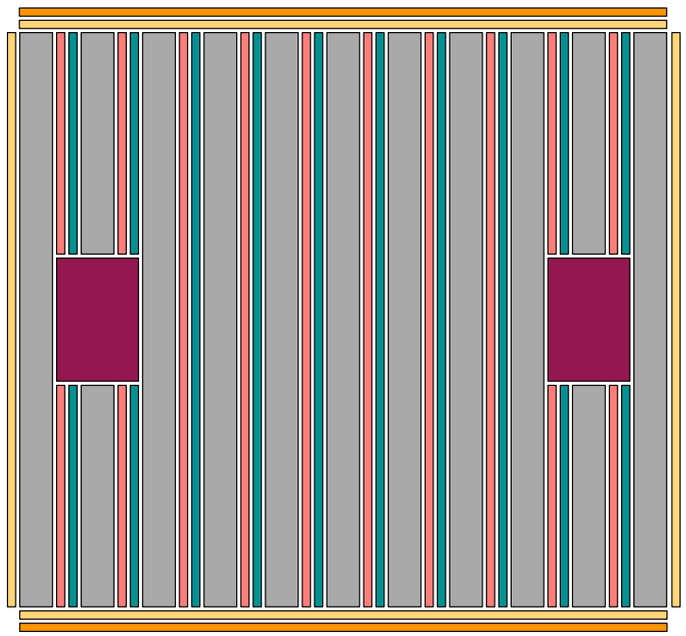
Hardware Platform

WARP Hardware

- WARP Hardware Components
  - FPGA Board
  - Radio Board
  - Clock Board
- FPGA Architecture
- Xilinx Platform Studio

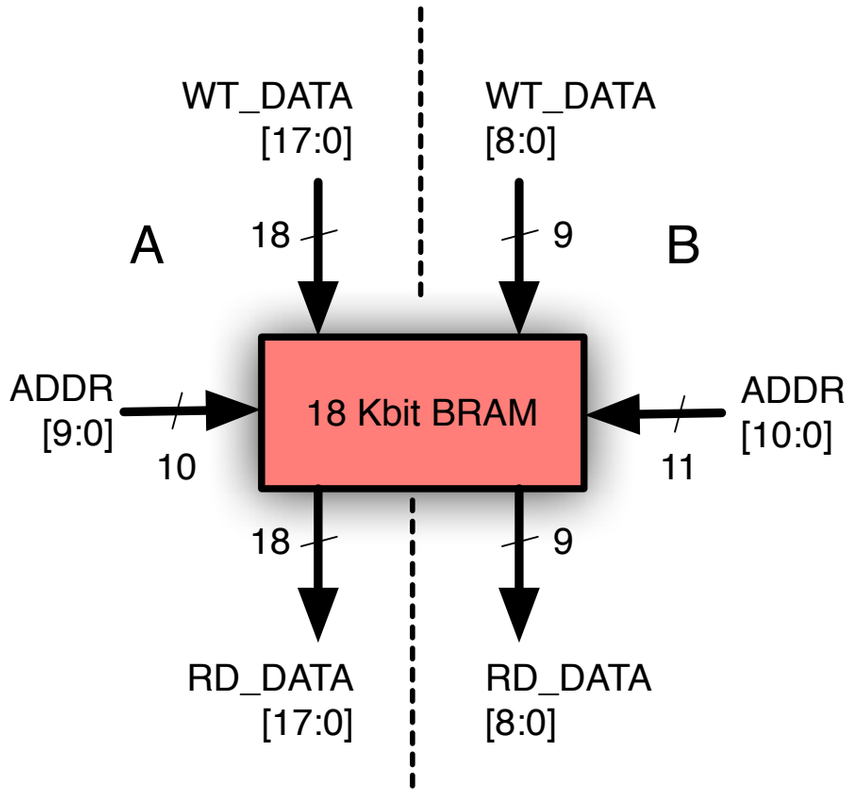
XC2VP70 Resources

XC2VP70 Resources



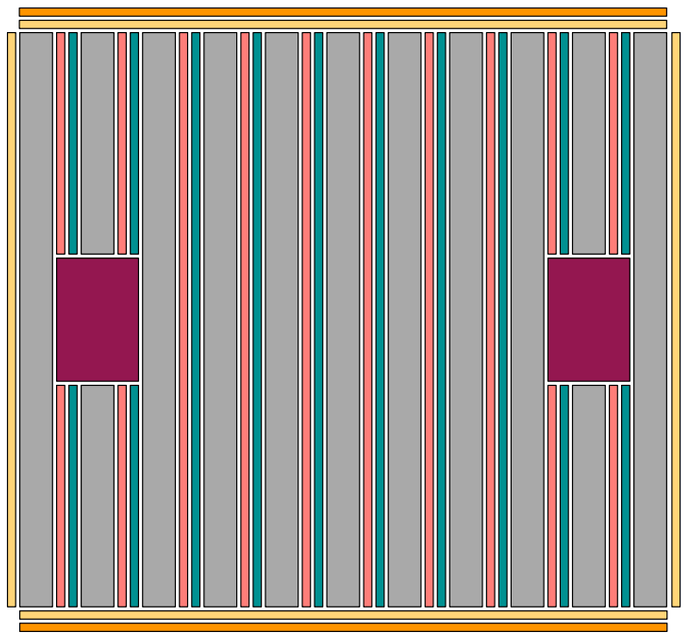
- Embedded PowerPC processors
- 18-Bit by 18-Bit multipliers
- 18 Kbit block RAMs
- General purpose I/Os
- Multi-gigabit transceivers (MGTs)
- Reconfigurable user logic (Fabric)

18 Kbit Block RAMs



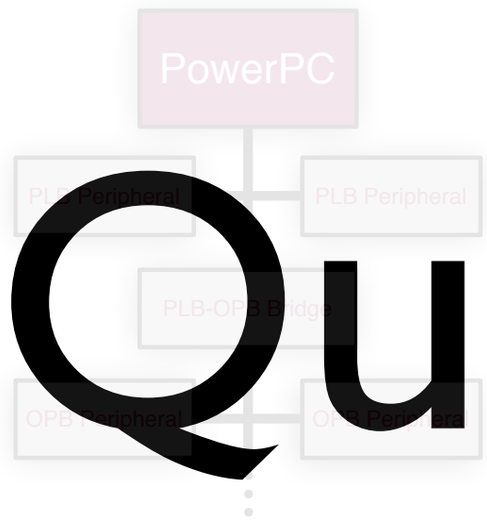
- Dual-ported for simultaneous reads and writes
- Simplifies construction of dual-port FIFOs
- Addressable via different aspect ratio on each port
- Coupled one-to-one with multipliers for extremely high throughput
- Operate independently and in parallel
- May be combined for increased capacity

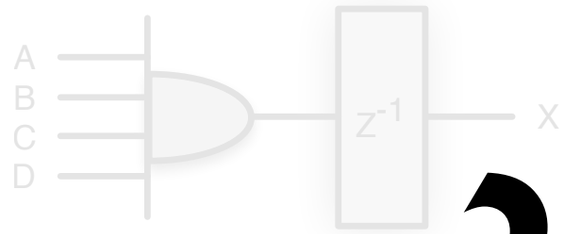
XC2VP70 Resources



- 2 PowerPC processors
- 328 multipliers
- 328 block RAMs
- 964 general purpose I/Os
- 16 MGTs (8 on WARP FPGA board)
- 66176 4-input LUTs
- 66176 flip-flops (plus I/O registers)

Questions?


PowerPC
PLB Peripheral
PLB-OPB Bridge
OPB Peripheral


A
B
C
D
Z-1
X

TX
RX

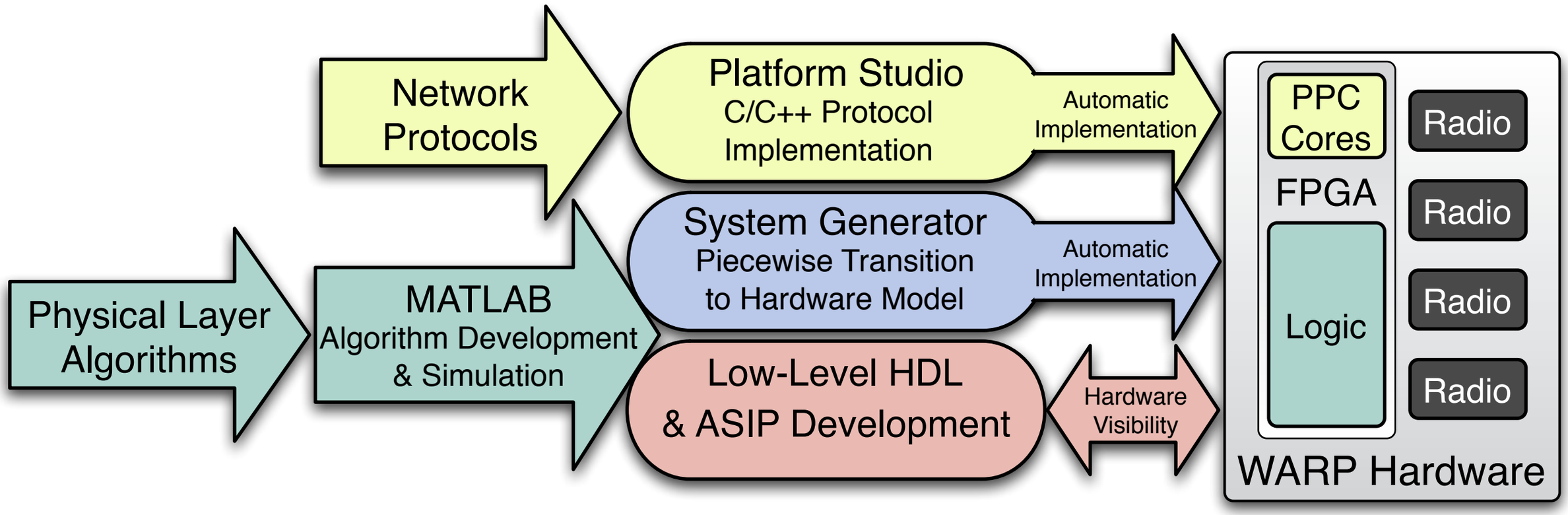
18
18
X
36
Z-1
36

WT_DATA
[17:0]
WT_DATA
[8:0]
A
18
9
B
ADDR
[9:0]
10
18 Kbit BRAM
11
ADDR
[10:0]
18
9
RD_DATA
[17:0]
RD_DATA
[8:0]

WARP Hardware

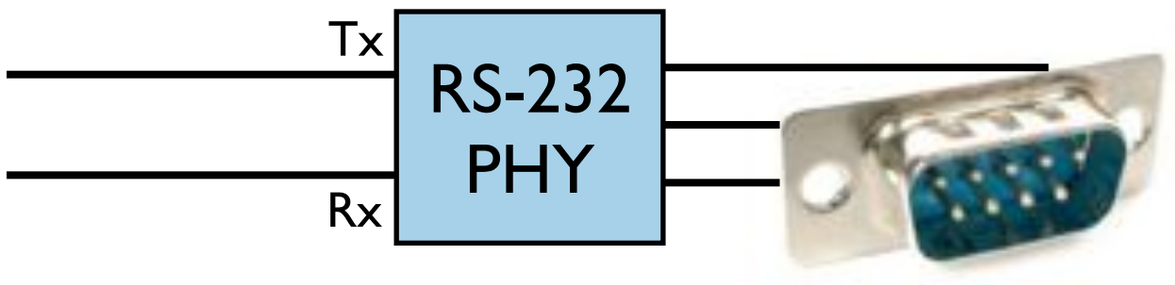
- WARP Hardware Components
  - FPGA Board
  - Radio Board
  - Clock Board
- FPGA Architecture
- Xilinx Platform Studio

Development Tools

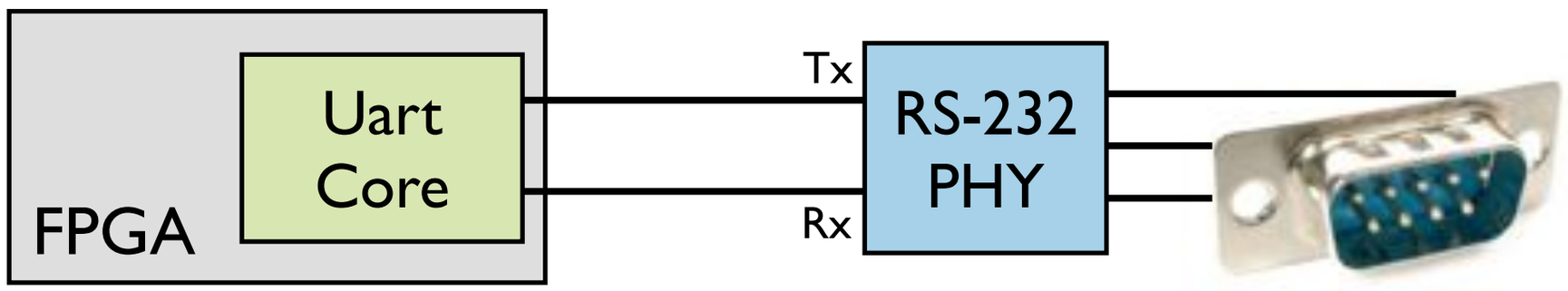


Hello World

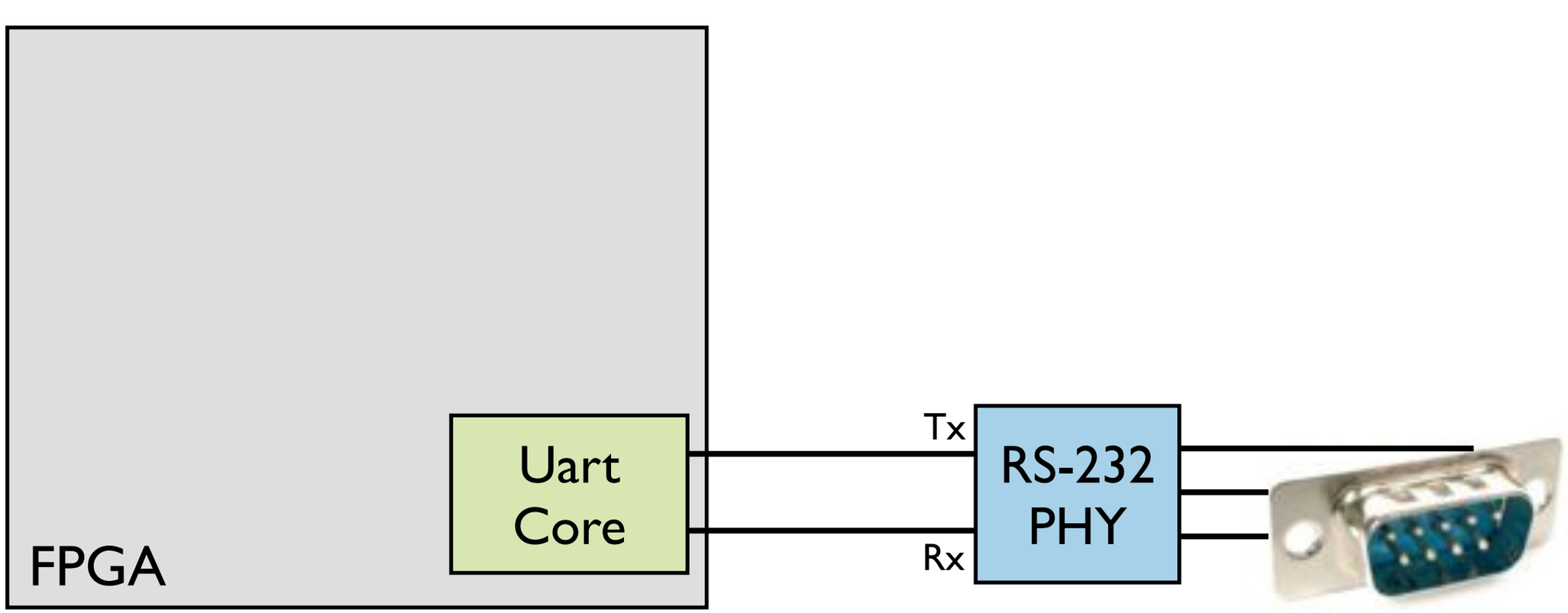
Hello World



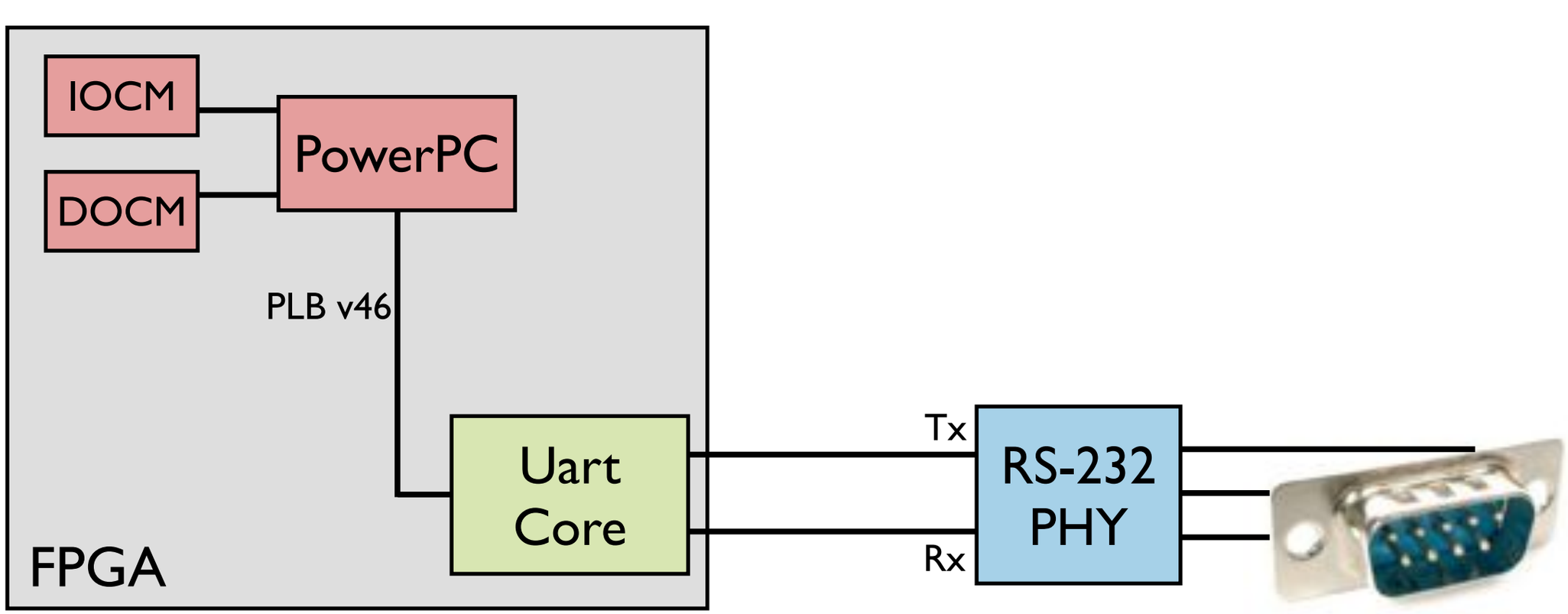
Hello World



Hello World



Hello World



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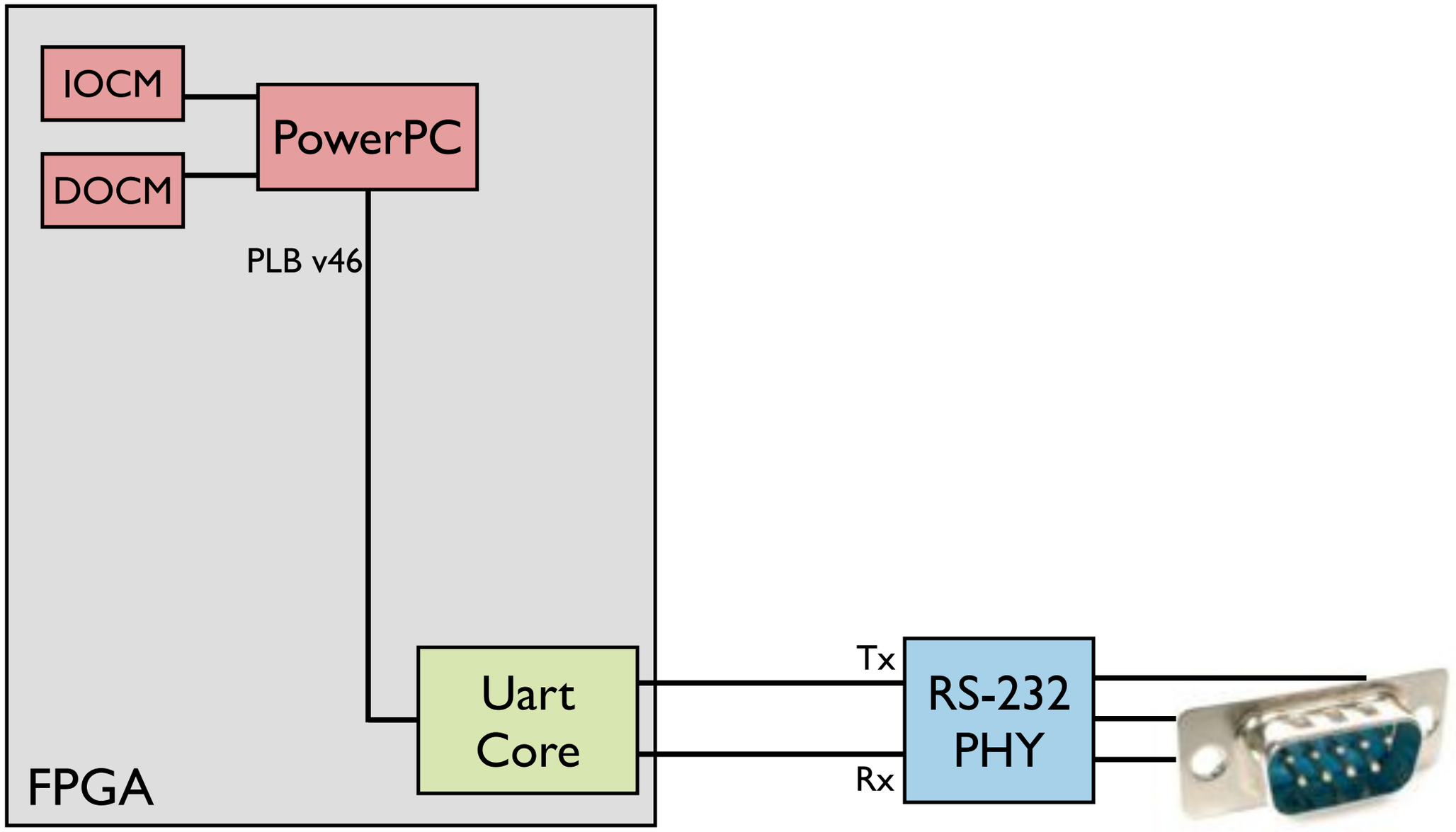
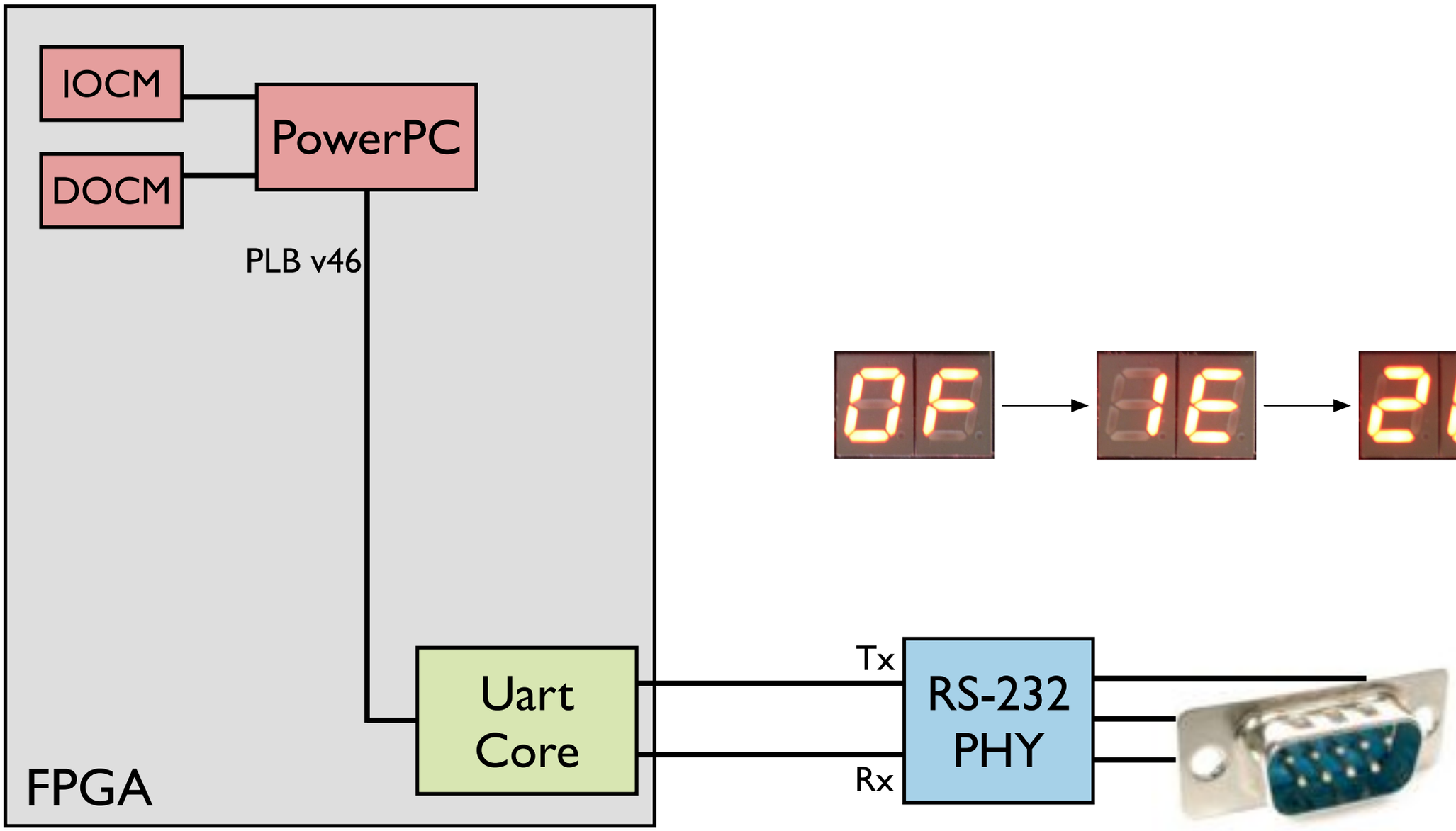
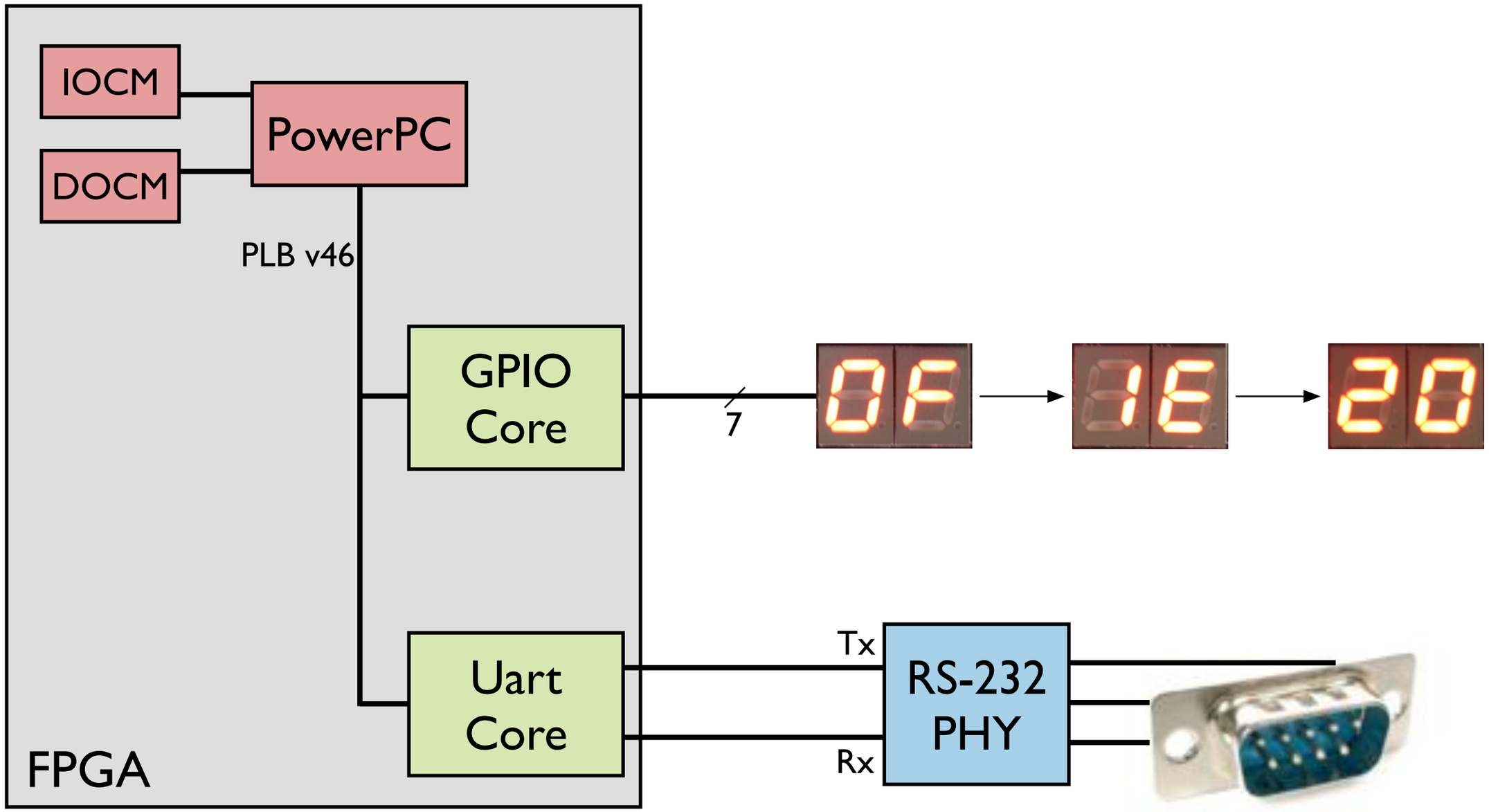


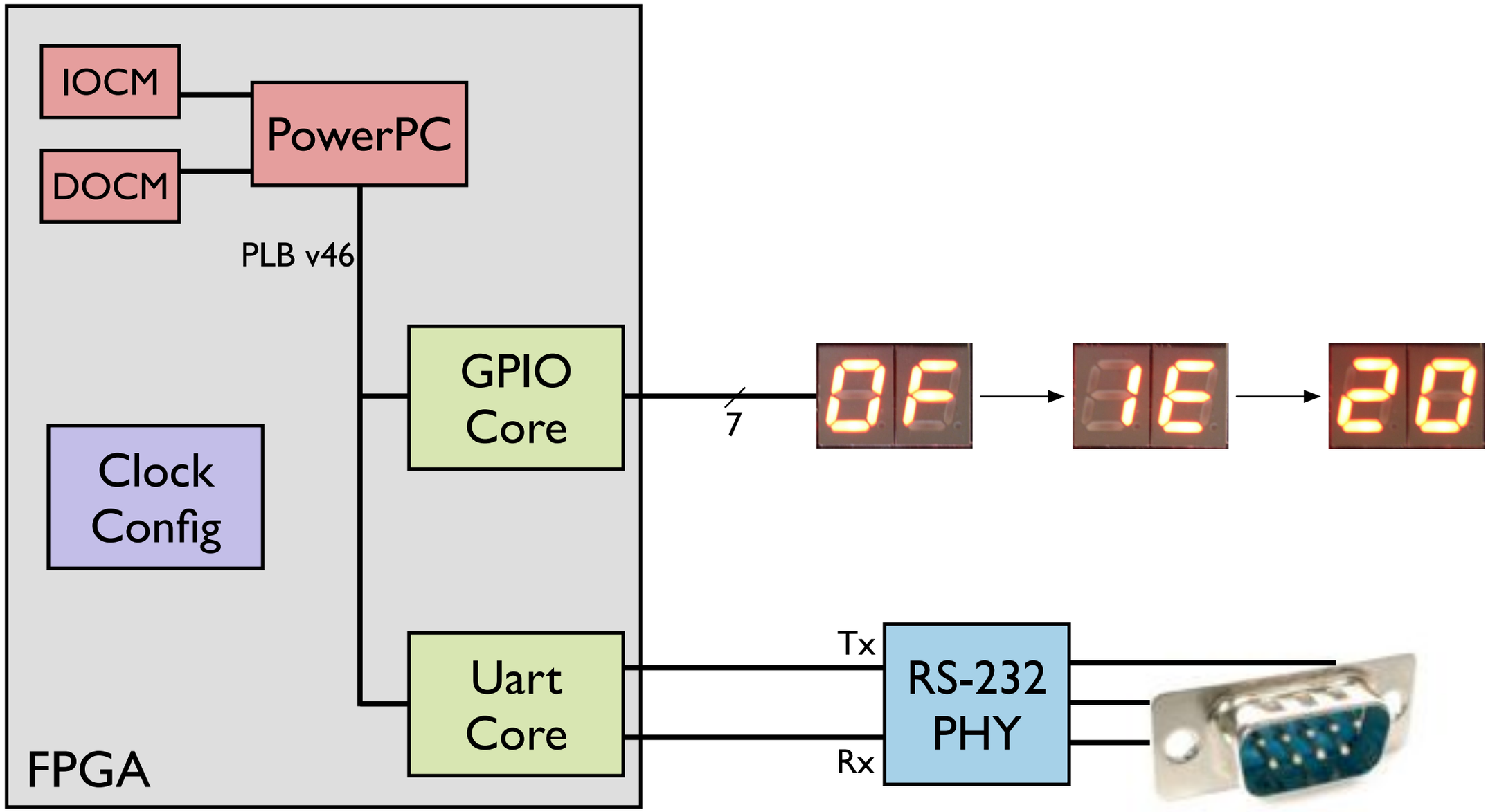
Hello World


IOCM
DOCM
PowerPC
PLB v46
Uart
Core
FPGA
Tx
Rx
RS-232
PHY
0F
1E
20

Hello World


IOCM
DOCM
PowerPC
PLB v46
GPIO
Core
Uart
Core
FPGA
7
Tx
Rx
RS-232
PHY

Hello World


IOCM
DOCM
PowerPC
PLB v46
GPIO Core
Clock Config
Uart Core
FPGA
7
0F
1E
20
Tx
Rx
RS-232 PHY

Lab 2: XPS Introduction

- Introduction to Xilinx Platform Studio
- Building a simple hardware platform
- Interacting with the WARP hardware