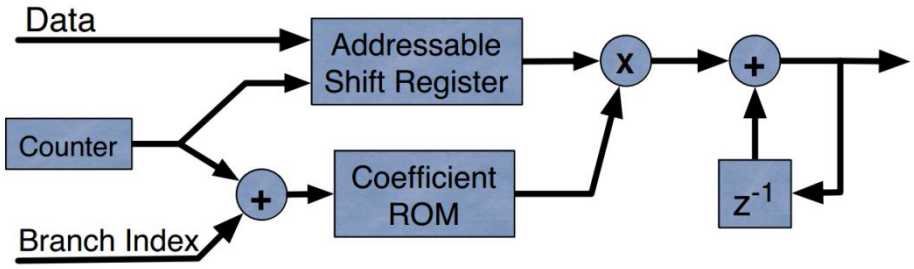
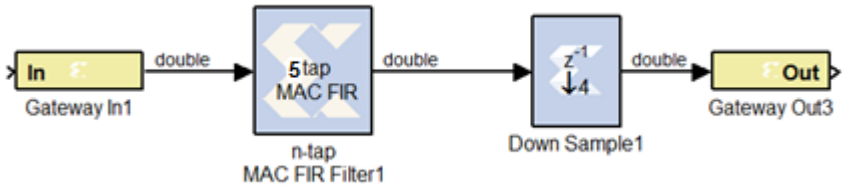
Elec 433 – Spring 2013 – Lab 4

In all the exercises below, use an input data type of Fix_12_10 and constrain every data signal, including coefficients, to no more than 16 bits. Use whatever impulse responses you like. I suggest using MATLAB's filter construction tool `fdatool` or commands like `fir1`, `fir2`, `firpm` or `rcosfir`. Verify your designs by plotting their outputs against the outputs of the Xilinx filter blocks; see Frequency Response Demo.

1) Implement the serial interpolating polyphase filter shown below. For each input sample, the filter should produce M=8 output samples. Each output sample should be computed by a sub-filter of length N/M=128/8=16. The same resources should be used to implement every sub-filter (i.e. no block should ever be idle). Assume data input sample period is 8 for this block and the output sample period is 1.



2) In part 2 of this lab, we will build a polyphase decimator (the spec is on the next page). In the example below, suppose we want to build a 4th order filter followed by downsample by 4.

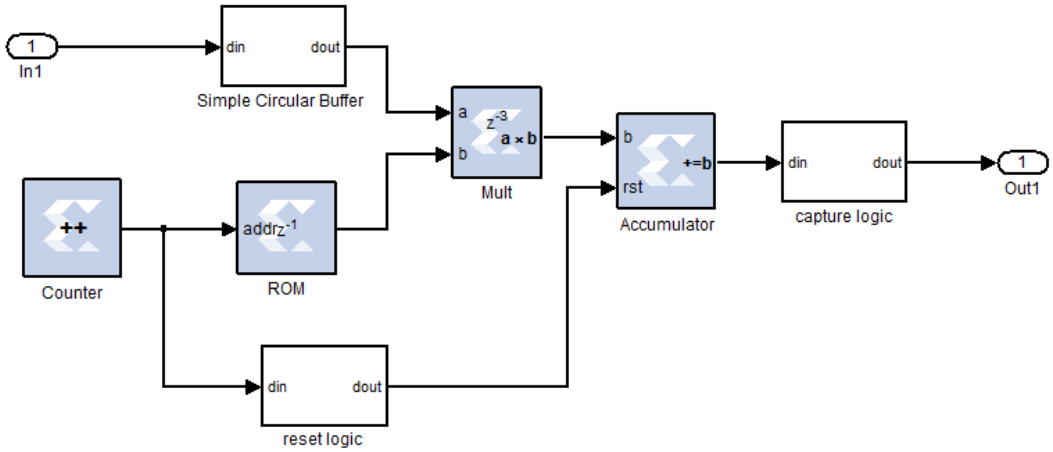


Let the input sequence be x = [0 1 2 3 4 5 6 7 8] and the filter coefficients be h = [1 2 3 4 5]. We can write the result of the convolution as:

h[0]**x**	0	1	2	3	4	5	6	7	8
h[1]$\mathbf{x^{-1}}$		0	2	4	6	8	10	12	14
h[2]$\mathbf{x^{-2}}$			0	3	6	9	12	15	18
h[3]$\mathbf{x^{-3}}$				0	4	8	12	16	20
h[4]$\mathbf{x^{-4}}$					0	5	10	15	20
Sum	0	1	4	10	20	35	50	65	80

We then decimate by 4 to get the final output: y = [0,20,80, …]. Before you build your design, I suggest you go over the questions below.

a) Why is a straightforward design (filter followed by decimation, example above) bad? Hint: how many multiplies do we really need in this design?
b) Describe how you can avoid multiplies that does not contribute to the final output.
c) Below is a diagram of a serial polyphase filter. Suppose the input rate is 1. What is the rate of the multiplier? What's the input rate and the output rate of the input sample buffer? Describe how the sample buffer should work.



Deliverable: Implement a polyphase decimator. The input period of this block is 1 and the output period rate is 8. Analogous to part 1, the length of the filter is 128 and the down sample rate is 8. Hint: for the sample buffer, you can use the sample buffer provided on the website. Please briefly describe this block in your report. Alternatively, you can implement your own sample buffer.