```c
//Extra definitions to access a specific shared memory address
#define SG_SMR0demo_SMR0_dpram1 (SG_SMR0demo_SMR0_dpram+0x04)
#define SG_SMR0demo_SMR0_dpram2 (SG_SMR0demo_SMR0_dpram+0x08)
#define SG_SMR0demo_SMR0_dpram3 (SG_SMR0demo_SMR0_dpram+0x0C)
#define SG_SMR0demo_SMR0_dpram4 (SG_SMR0demo_SMR0_dpram+0x10)

int main()
{
   while(1)
   {
      *((volatile unsigned int*) SG_SMR0demo_Gateway_In1) = 5;
      usleep(100);
      xil_printf("\n\rGWout: %d",  *((volatile unsigned int*) SG_SMR0demo_Gateway_Out1));

      xil_printf("\n\rValue0: %d ", *((volatile unsigned int*) SG_SMR0demo_SMR0_dpram));
      xil_printf("\n\rValue1: %d ", *((volatile unsigned int*) SG_SMR0demo_SMR0_dpram1));
      xil_printf("\n\rValue2: %d ", *((volatile unsigned int*) SG_SMR0demo_SMR0_dpram2));
      xil_printf("\n\rValue3: %d ", *((volatile unsigned int*) SG_SMR0demo_SMR0_dpram3));
      xil_printf("\n\rValue4: %d ", *((volatile unsigned int*) SG_SMR0demo_SMR0_dpram4));
      XUartLite_RecvByte(STDIN_BASEADDRESS);
   }
   return 0;
}
```