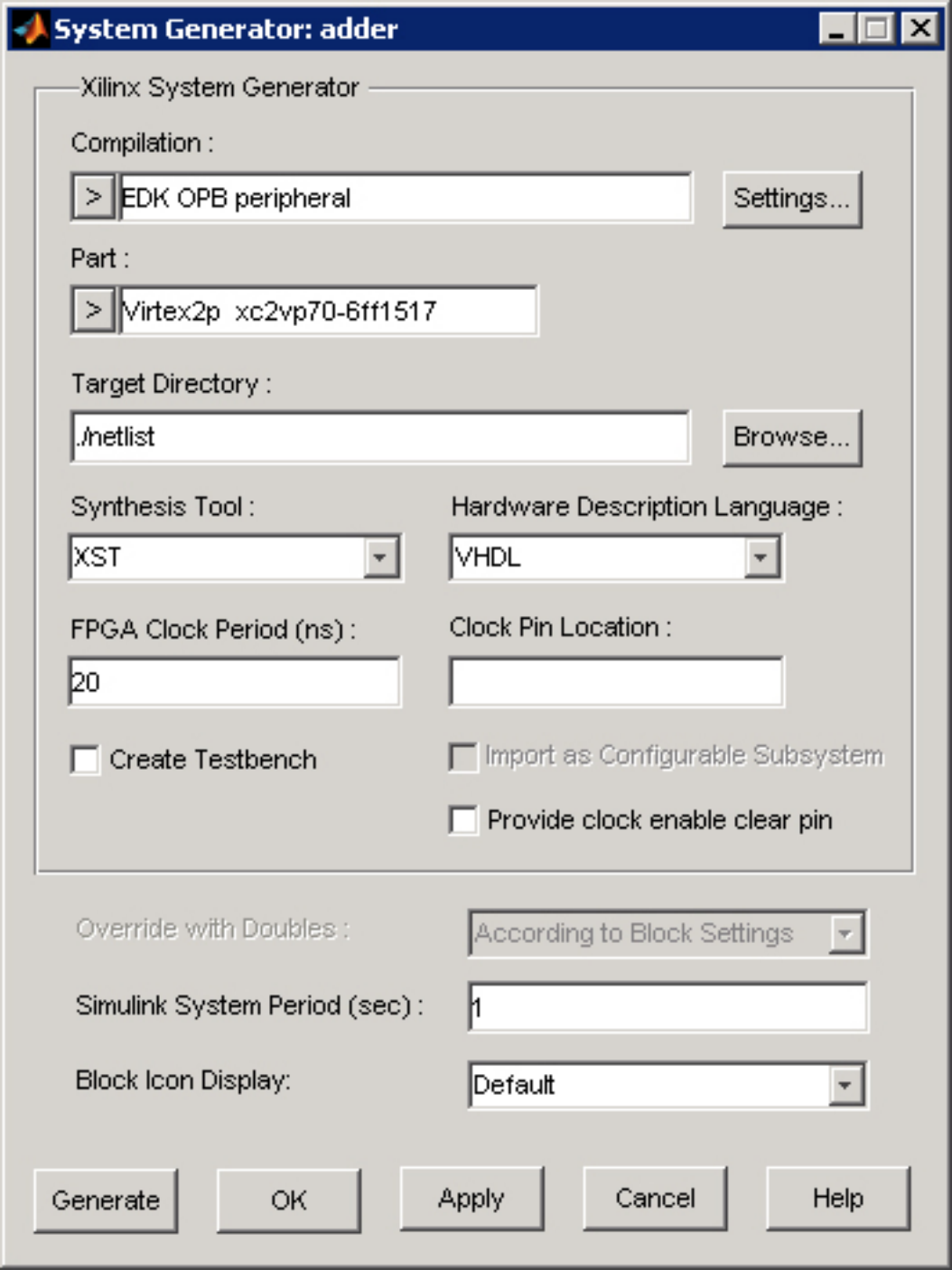
System Generator: adder
Xilinx System Generator
Compilation :
>
EDK OPB peripheral
Settings...
Part :
>
Virtex2p xc2vp70-6ff1517
Target Directory :
./netlist
Browse...
Synthesis Tool :
XST
Hardware Description Language :
VHDL
FPGA Clock Period (ns) :
20
Clock Pin Location :
Create Testbench
Import as Configurable Subsystem
Provide clock enable clear pin
Override with Doubles :
According to Block Settings
Simulink System Period (sec) :
1
Block Icon Display:
Default
Generate
OK
Apply
Cancel
Help