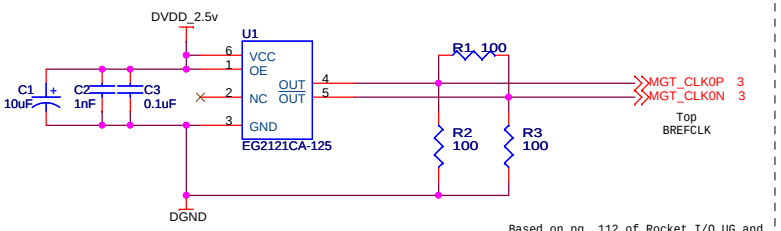
TAP FPGA Board
Rev x1

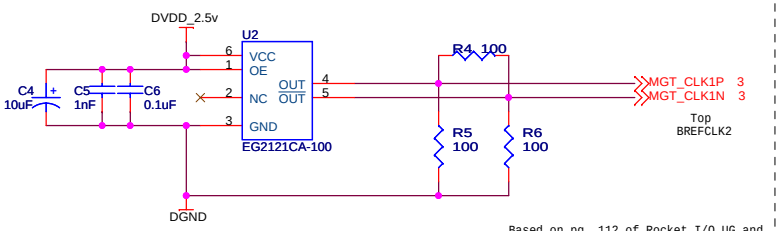
Schematic Pages:

Rice University	
Title: TAP FPGA Board	
Description: Table of Contents	Rev: x1
Date: Sunday, September 26, 2004	Sheet 1 of 14



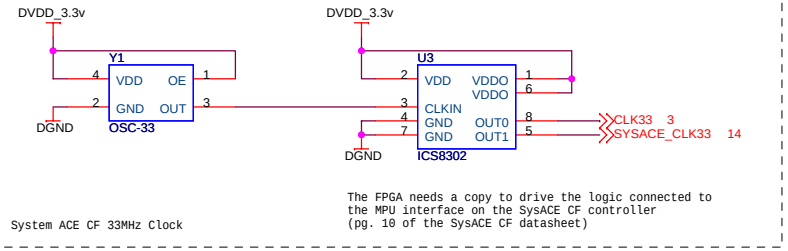
125MHz MGT Reference Clock

Based on pg. 112 of Rocket I/O UG and Avnet V2Pro dev board schematics



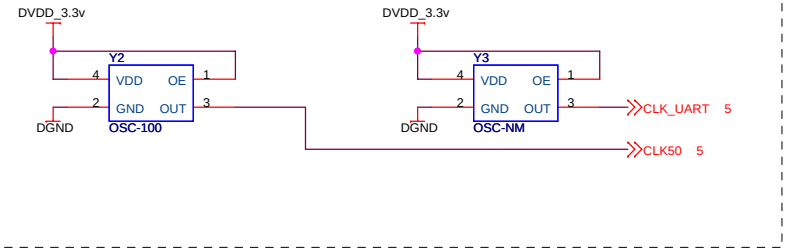
100MHz MGT Reference Clock

Based on pg. 112 of Rocket I/O UG and Avnet V2Pro dev board schematics

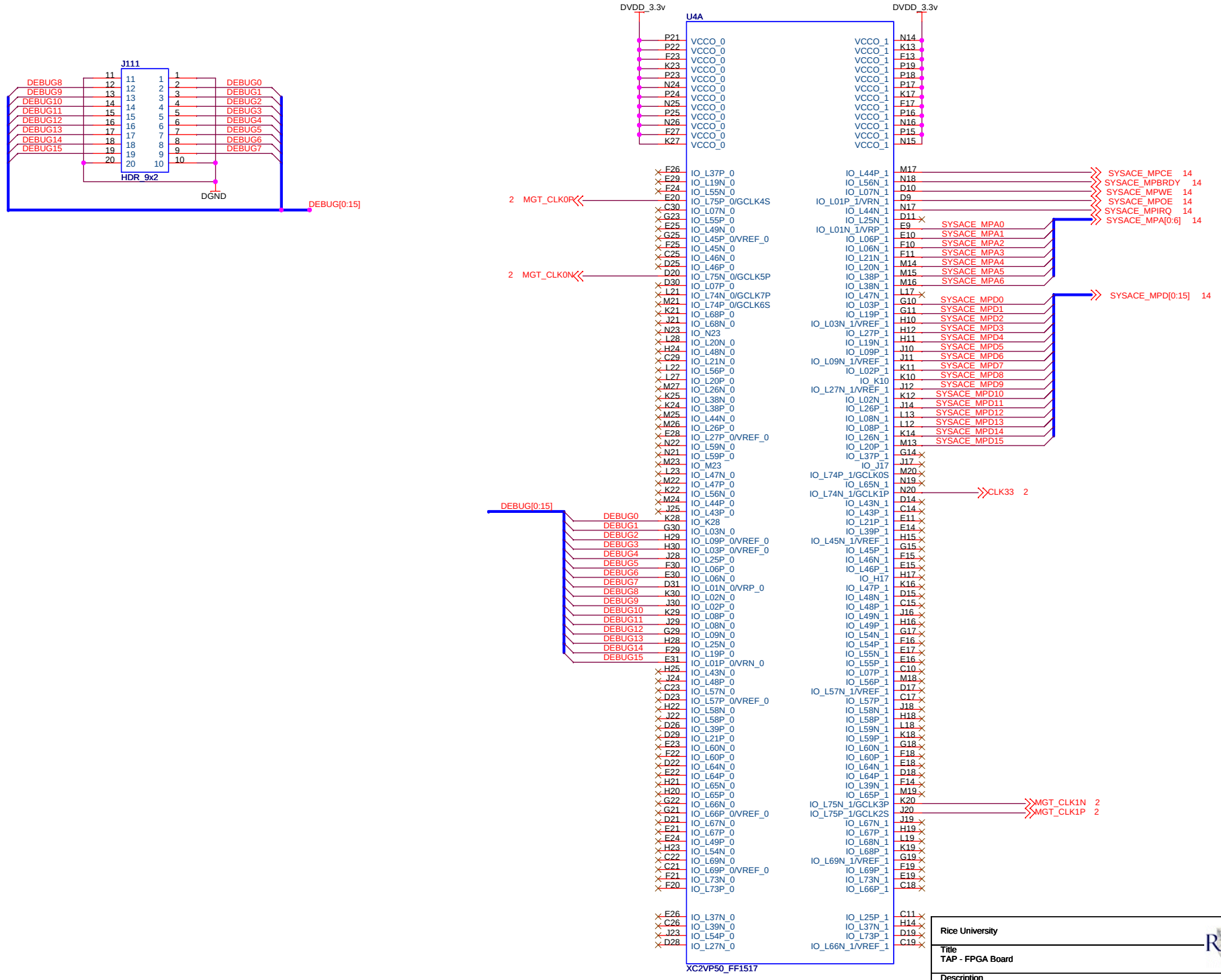


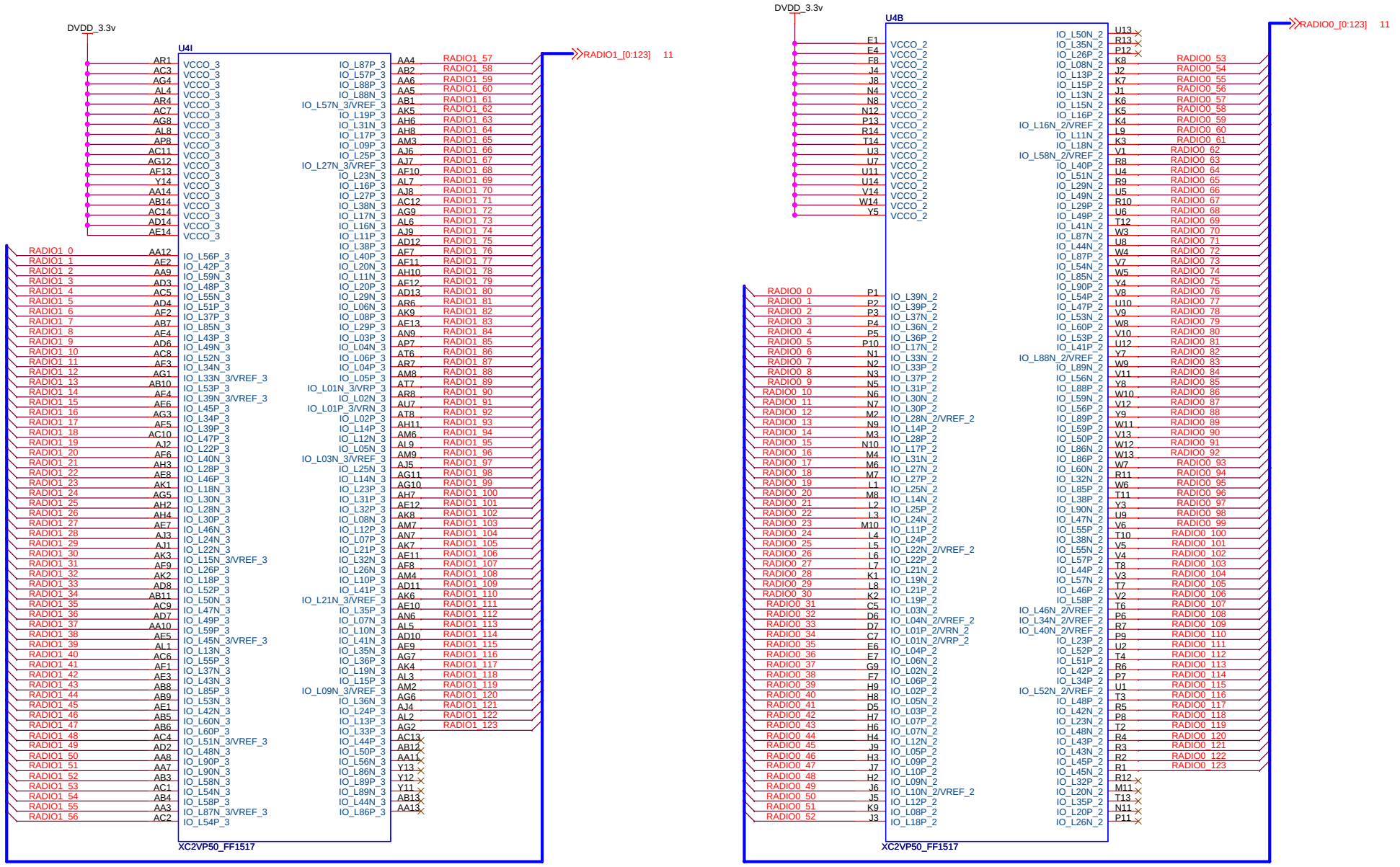
System ACE CF 33MHz Clock

The FPGA needs a copy to drive the logic connected to the MPU interface on the SysACE CF controller (pg. 10 of the SysACE CF datasheet)

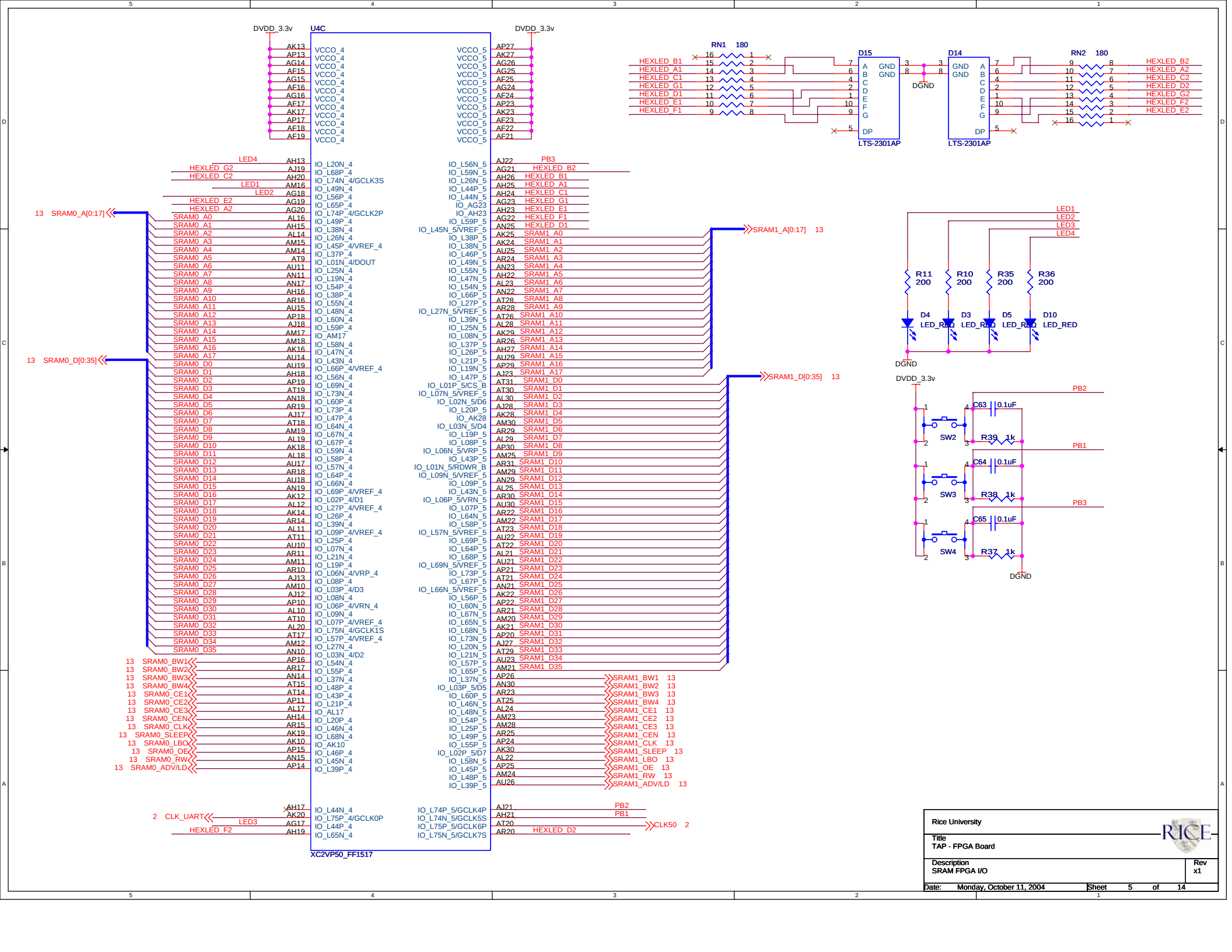


Rice University			
Title: TAP - FPGA Board			
Description: Clocks			Rev: x1
Date: Monday, October 11, 2004	Sheet 2 of 14		

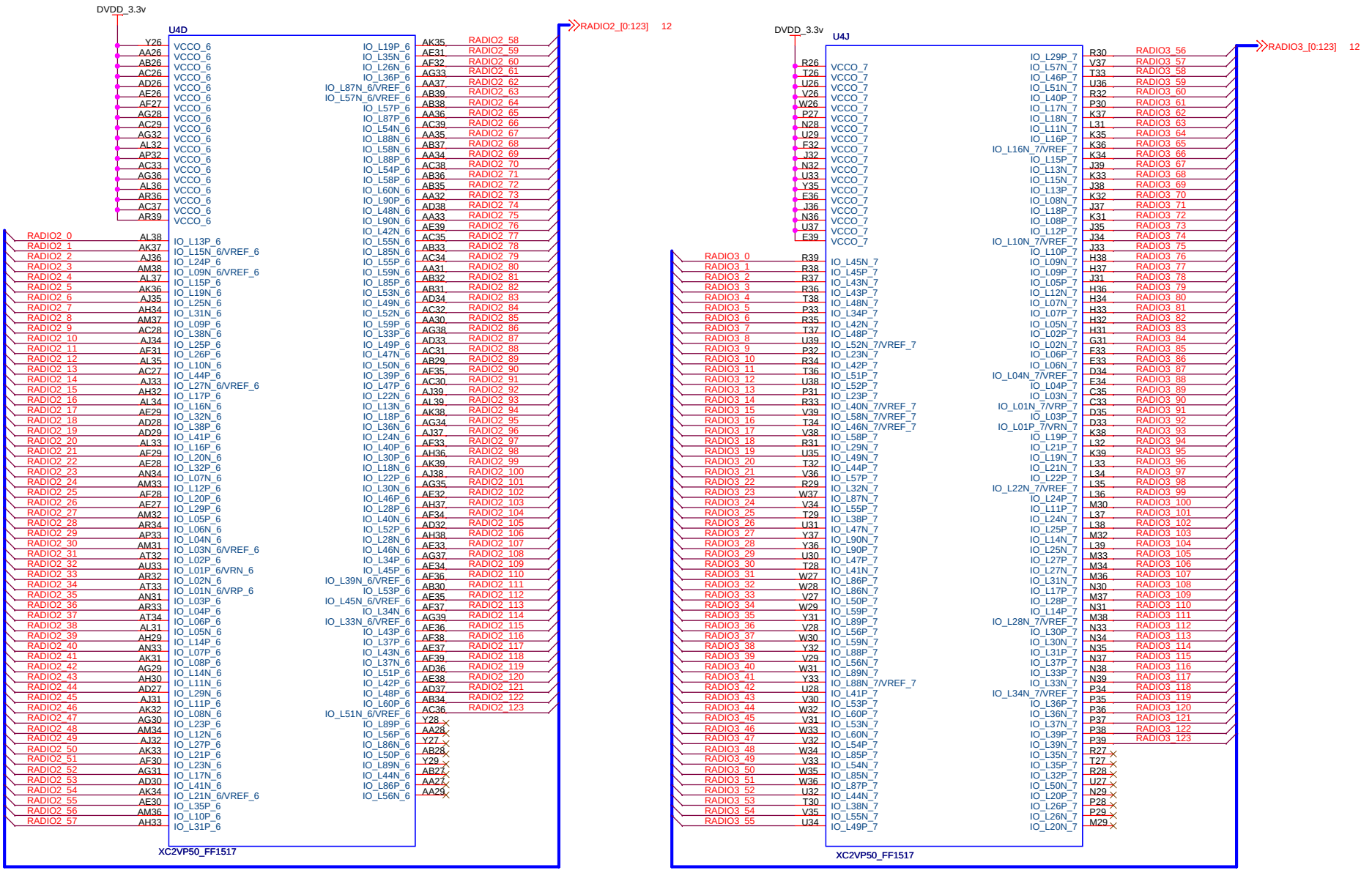

J111
HDR_9x2
DGND
DEBUG[0:15]
U4A
DVDD_3.3v
XC2VP50_FF1517
MGT_CLK0P
MGT_CLK0N
SYSACE_MPCE 14
SYSACE_MPBRDY 14
SYSACE_MPWE 14
SYSACE_MPOE 14
SYSACE_MPIRQ 14
SYSACE_MPA[0:6] 14
SYSACE_MPD[0:15] 14
CLK33 2
MGT_CLK1N 2
MGT_CLK1P 2
Rice University
Title
TAP - FPGA Board
Description
Misc FPGA I/O
Rev
x1
Date: Monday, October 11, 2004
Sheet 3 of 14



Rice University	
Title: TAP - FPGA Board	
Description: Radios 0-1 FPGA I/O	Rev: x1
Date: Monday, October 11, 2004	Sheet 4 of 14



Rice University	
Title: TAP - FPGA Board	
Description: SRAM FPGA I/O	Rev: x1
Date: Monday, October 11, 2004	Sheet 5 of 14



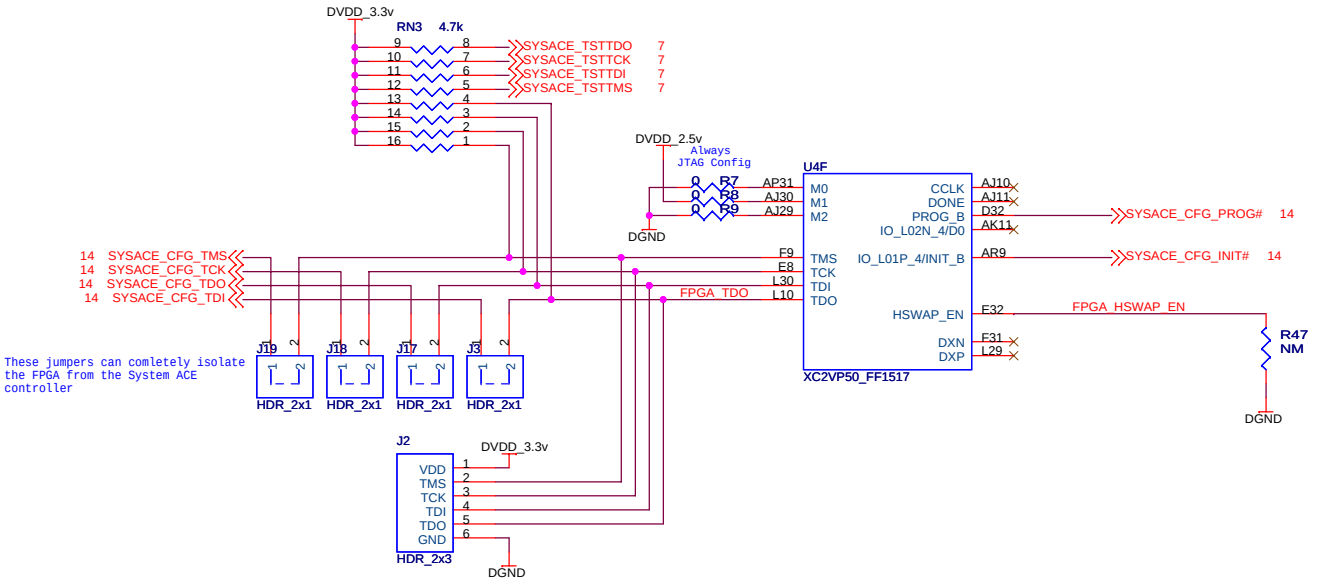
Rice University

Title
TAP - FPGA Board

Description
Radios 2-3 FPGA I/O

Rev
x1

Date: Monday, October 11, 2004 Sheet 6 of 14



Rice University	
Title: TAP - FPGA Board	
Description: FPGA JTAG, Configuration & Temperature Control	Rev: x1
Date: Monday, October 11, 2004	Sheet 7 of 14

Notes:
MGTB_AGND: Analog ground for bottom edge MGTs
MGTT_AGND: Analog ground for top edge MGTs
MGT_2.5v: Dedicated MGT power supply
MGT_VTR_x: MGT Rx termination voltage
(tied to MGT_2.5v for DC coupling, 1.8v for AC)

DVDD_2.5v

Unused MGTs must still be powered
See pg. 14 of the V2Pro Datasheet for details

U4E

Bottom Edge MGTs

Top Edge MGTs

XC2VP50_FF1517

MGT_2.5v

MGT_VTR_1 MGT_VTR_2 MGT_VTR_3 MGT_VTR_4 MGT_VTR_5 MGT_VTR_6 MGT_VTR_7 MGT_VTR_8

MGTT_AGND

MGTB_AGND

HSSDC2 Jack

Four MGTs always set for DC-coupled links
Four MGTs configurable for AC or DC-coupled links

Analog/Digital Ground Filtering

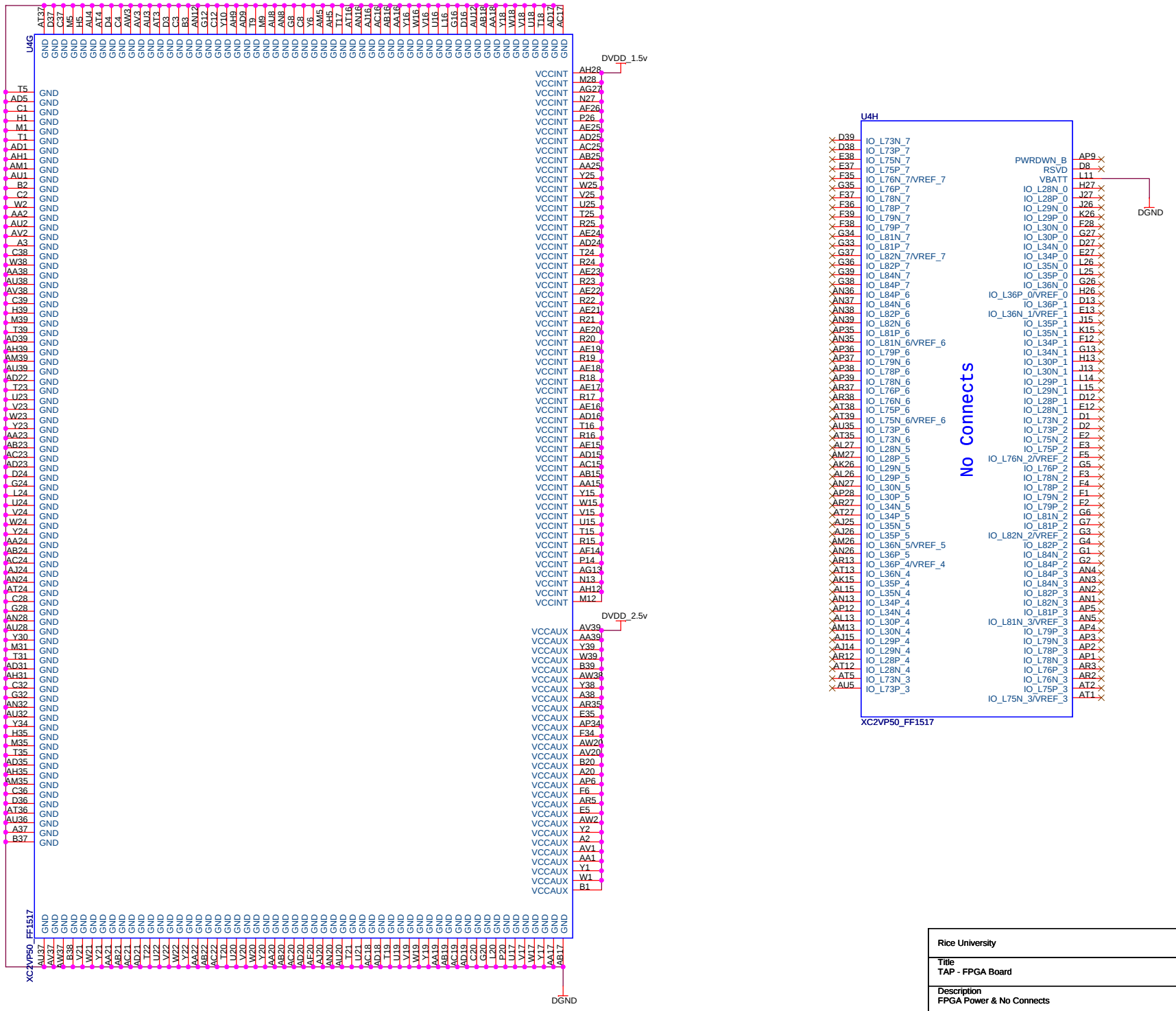
Top MGTs are used, so copule their AGND through inductors

L39 PLM18AG102SN1
L38 PLM18AG102SN1
L37 PLM18AG102SN1
L36 PLM18AG102SN1
L34 PLM18AG102SN1

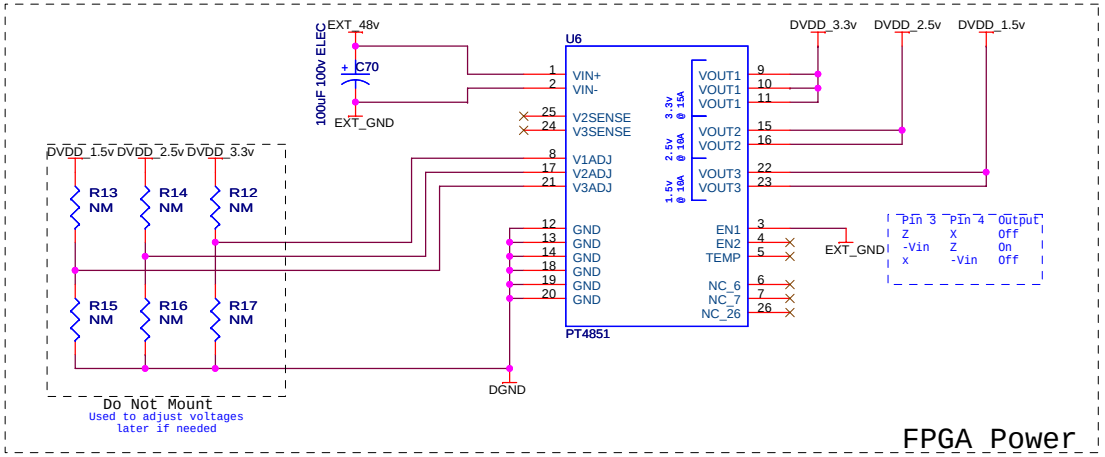
Bottom MGTs are unused, so their AGND is just DGND

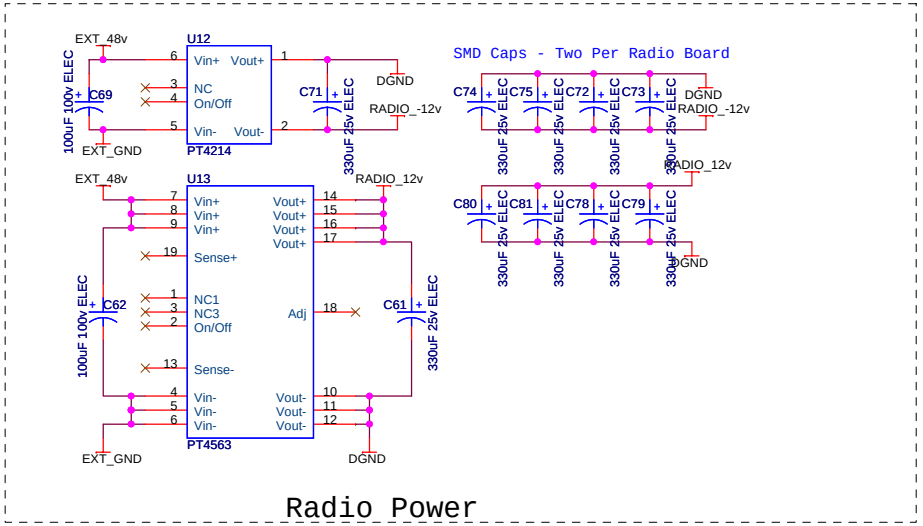
MGTB_AGND DGND MGTT_AGND DGND

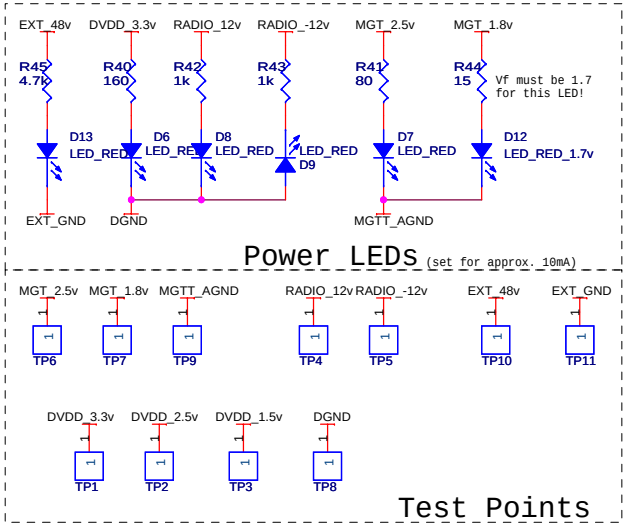
Rice University	
Title: TAP - FPGA Board	
Description: Multi-gigabit Transceivers	Rev: x1
Date: Monday, October 11, 2004	Sheet 8 of 14

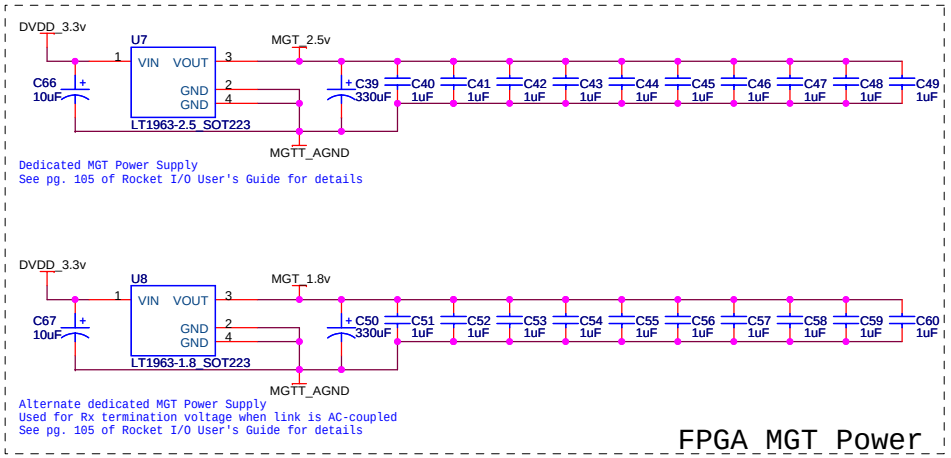


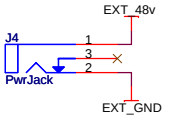
Rice University	
Title: TAP - FPGA Board	
Description: FPGA Power & No Connects	Rev: x1
Date: Monday, October 11, 2004	Sheet 9 of 14

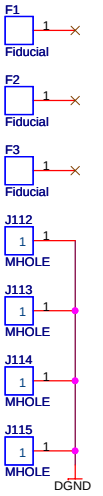




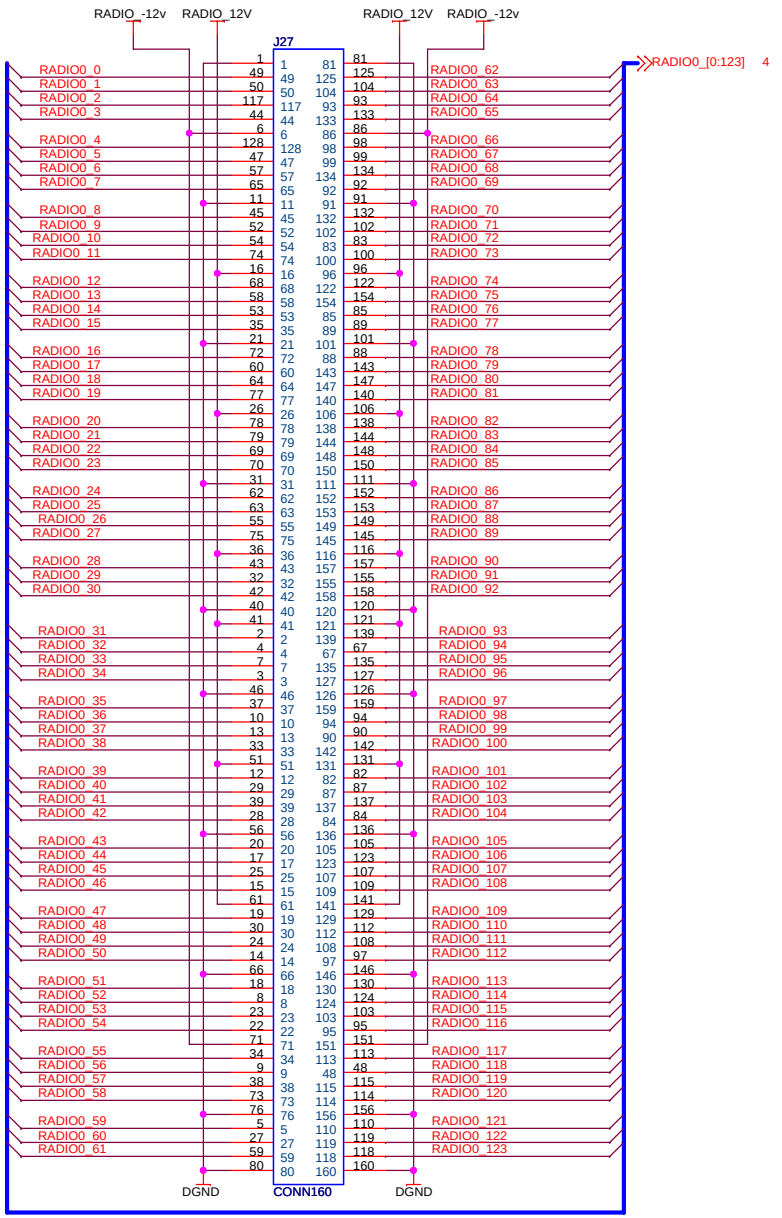


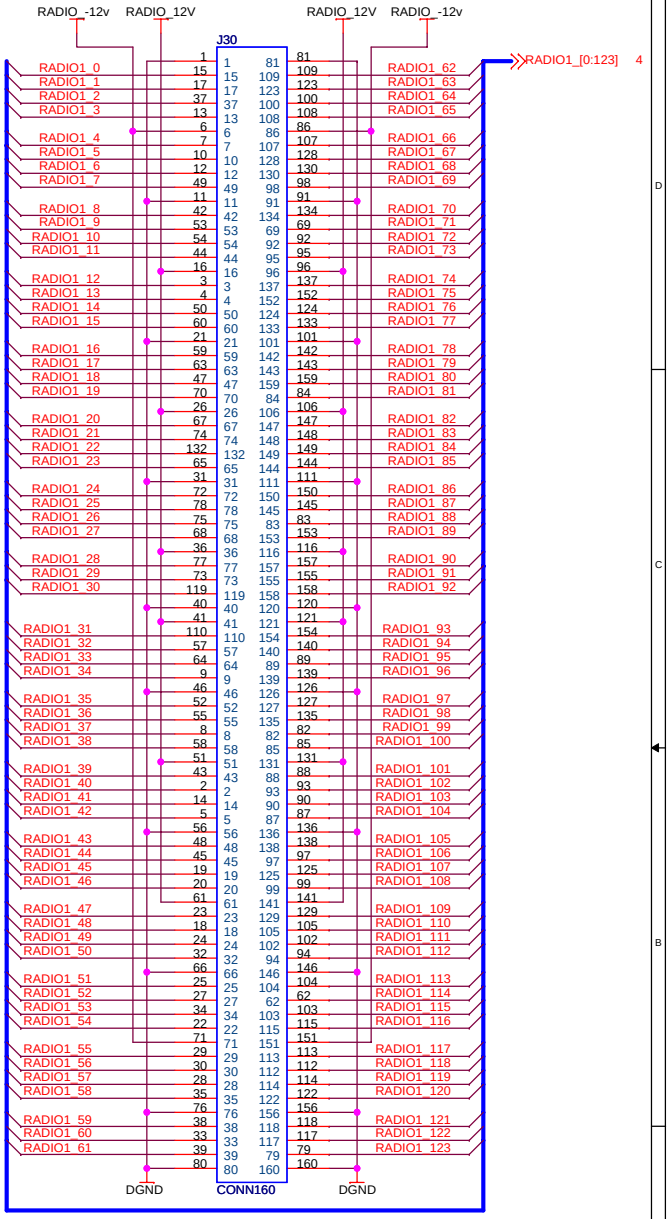




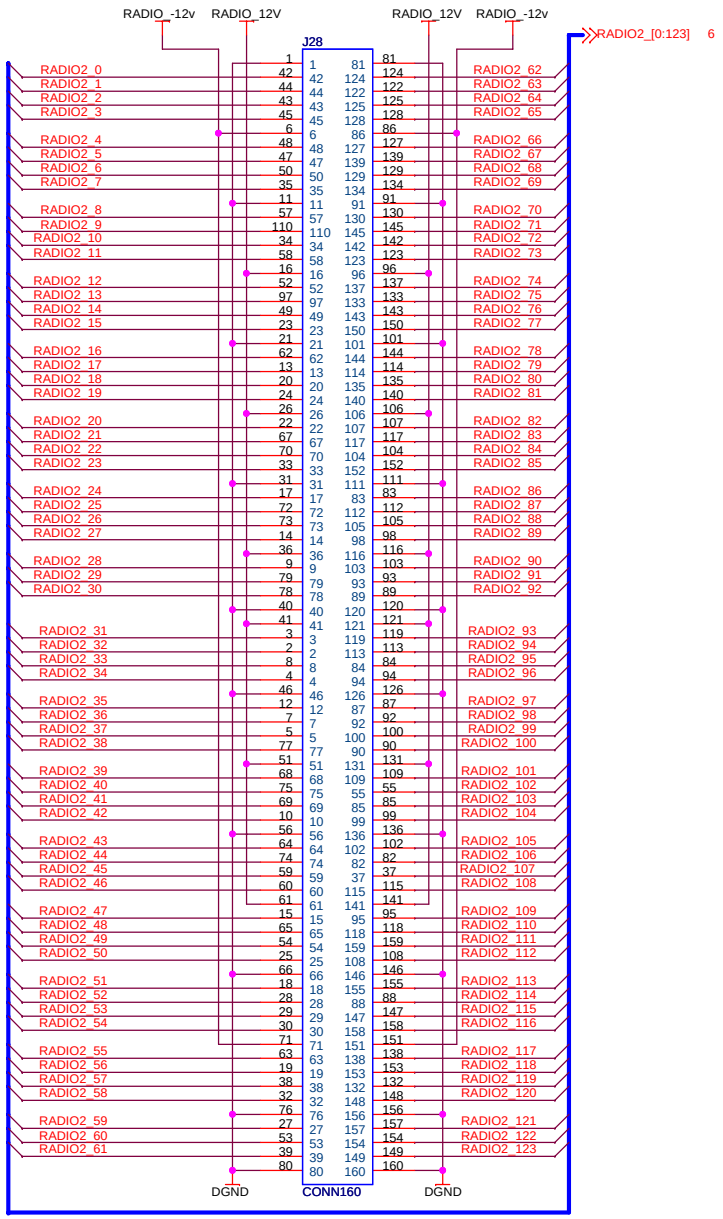


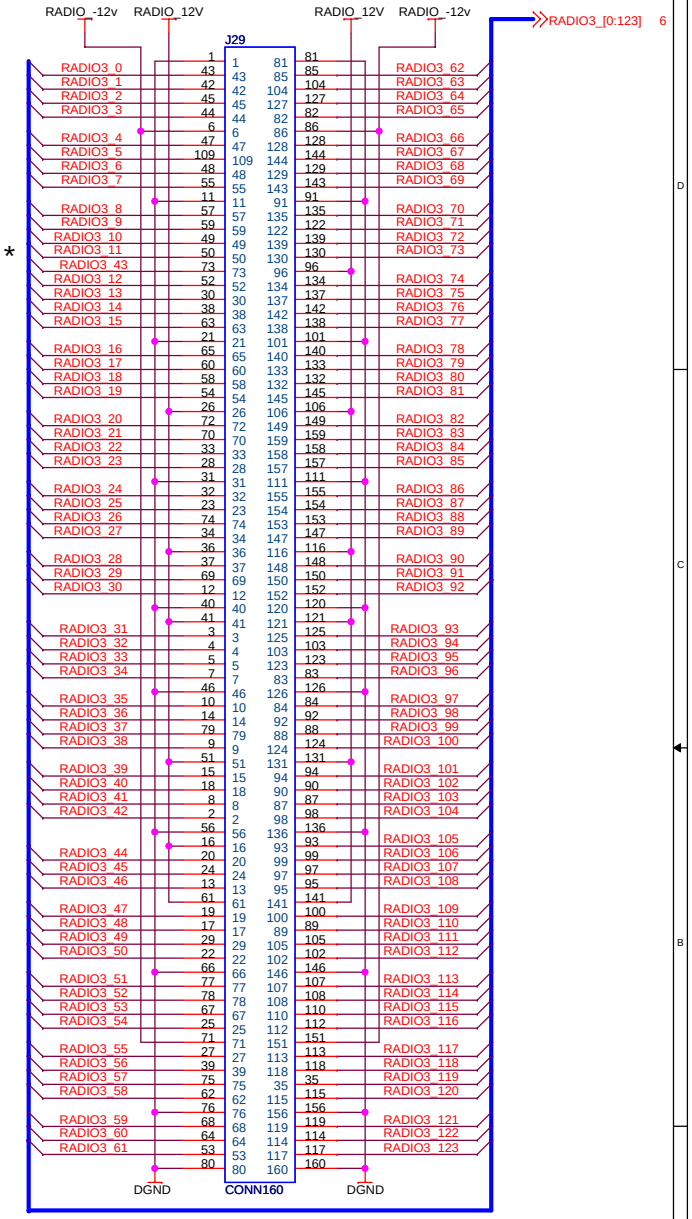
Rice University	
Title: TAP - FPGA Board	
Description: Power Regulators	Rev: x1
Date: Monday, October 11, 2004	Sheet 10 of 14



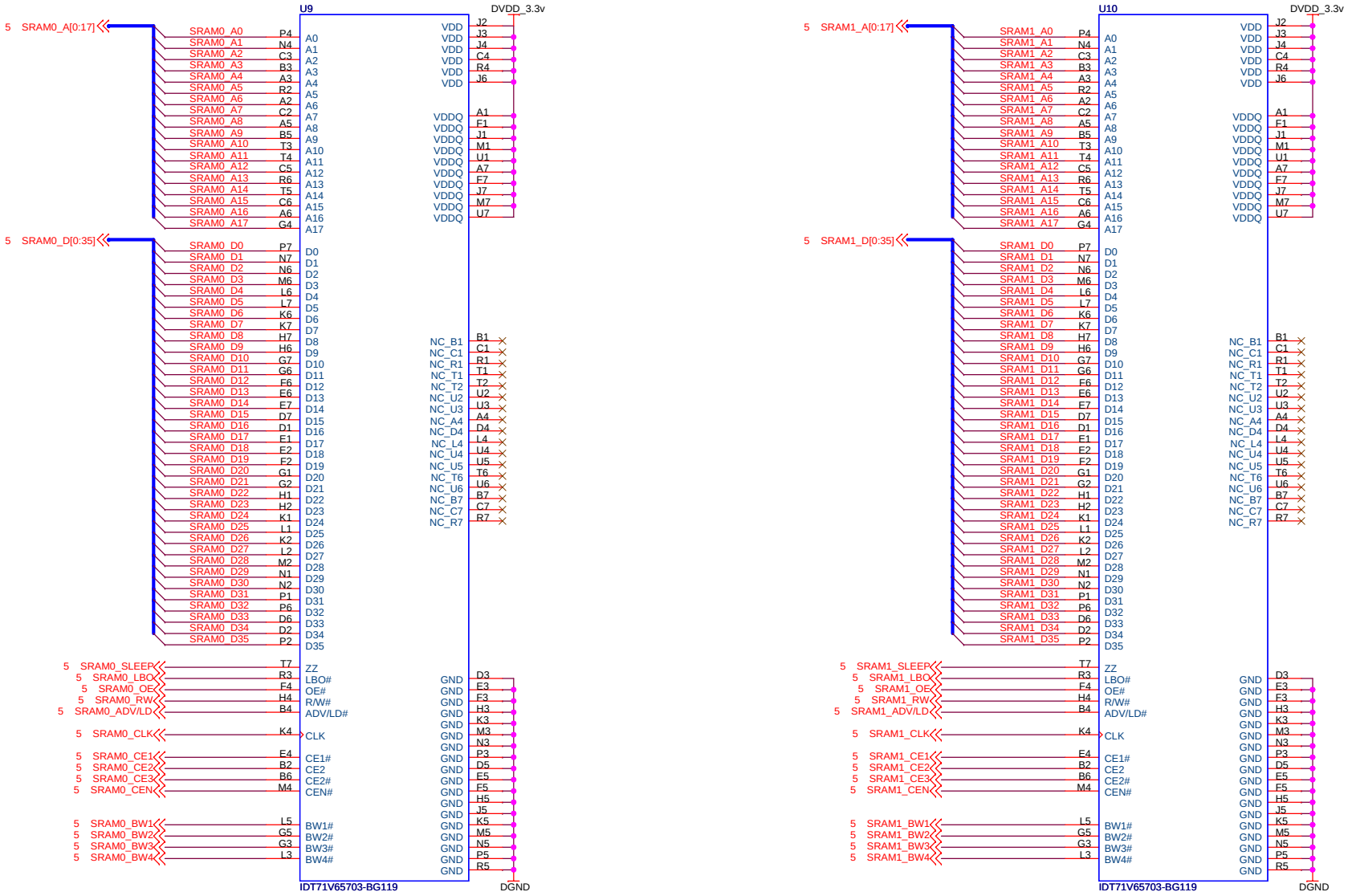


Rice University	
Title TAP - FPGA Board	
Description Radio Board Headers	Rev x1
Date: Monday, October 11, 2004	Sheet 11 of 14

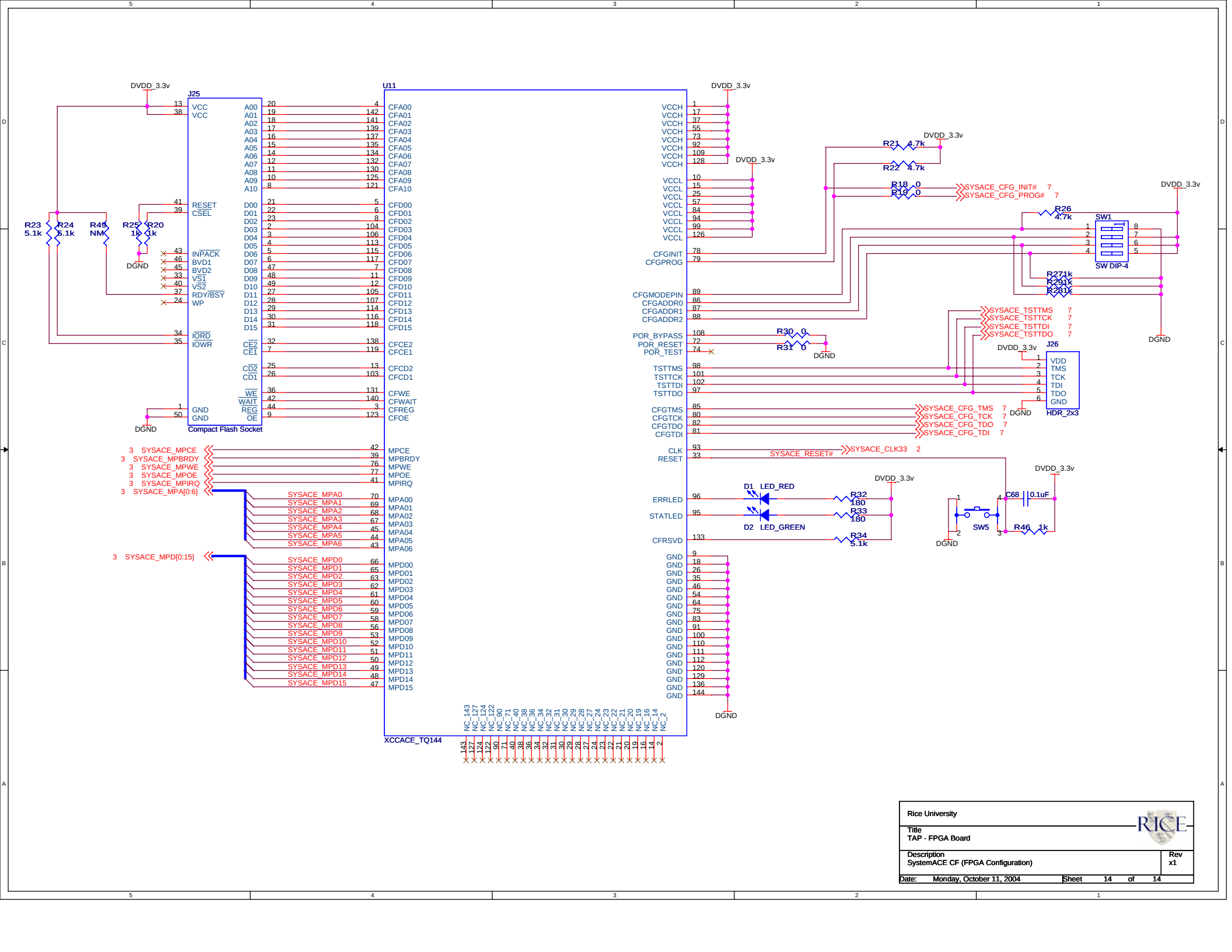




Rice University	
Title TAP - FPGA Board	
Description Radio Board Headers	Rev x1
Date: Monday, October 11, 2004	Sheet 12 of 14



Rice University	
Title: TAP - FPGA Board	
Description: SRAMs	Rev: x1
Date: Monday, October 11, 2004	Sheet 13 of 14


DVDD_3.3v
J25
U11
Compact Flash Socket
XCCACE_TQ144
DGND
R23 5.1k
R24 5.1k
R49 NM
R25 1k
R20 1k
R21 4.7k
R22 4.7k
R18 0
R19 0
R26 4.7k
R271k
R291k
R281k
SW1
SW DIP-4
SYSACE_CFG_INIT# 7
SYSACE_CFG_PROG# 7
R30 0
R31 0
J26
HDR_2x3
SYSACE_TSTTMS 7
SYSACE_TSTTCK 7
SYSACE_TSTTDI 7
SYSACE_TSTTDO 7
SYSACE_CFG_TMS 7
SYSACE_CFG_TCK 7
SYSACE_CFG_TDO 7
SYSACE_CFG_TDI 7
SYSACE_RESET#
SYSACE_CLK33 2
D1 LED_RED
D2 LED_GREEN
R32 180
R33 180
R34 5.1k
SW5
C68 0.1uF
R46 1k
SYSACE_MPCE 3
SYSACE_MPBRDY 3
SYSACE_MPWE 3
SYSACE_MPOE 3
SYSACE_MPIRQ 3
SYSACE_MPA[0:6] 3
SYSACE_MPD[0:15] 3
Rice University
Title
TAP - FPGA Board
Description
SystemACE CF (FPGA Configuration)
Rev
x1
Date: Monday, October 11, 2004
Sheet 14 of 14


FPGA VCC_INT Bypass (56 power pins)
DVDD_1.5v
DGND
C131 C132 C134 C133 C138 C135 C137 C136 0.047uF
C146 C139 C141 C140 C145 C142 C144 C143 0.047uF
C157 C150 C152 C151 C156 C153 C155 C154 0.047uF
C161 C158 C160 C159 C165 C162 C164 C163 0.047uF
C166 C167 C168 C169 0.47uF
C173 C170 C171 C172 0.47uF
C177 C174 C175 C176 0.47uF
C181 C178 C179 C180 0.47uF
C113 C115 C117 C119 C118 C120 2.2uF
C121 470uF
FPGA VCC_AUX Bypass (28 power pins)
DVDD_2.5v
DGND
C200 C184 C192 C193 C194 0.047uF
C199 C195 C196 C197 C198 0.047uF
C205 C201 C202 C203 C204 0.047uF
C187 C186 C185 C183 0.47uF
C190 C189 C188 C191 0.47uF
C149 470uF
C122 C123 C147 C148 2.2uF
Radio Boards Bypass
RADIO_12v
RADIO_-12v
DVDD_3.3v
DVDD_2.5v
DGND
C383 C380 C397 C396 C405 C404 C382 C381 0.047uF
C387 C384 C399 C398 C407 C406 C386 C385 0.047uF
C395 C388 C403 C400 C408 C409 C389 C390 0.47uF
C394 C391 C402 C401 C410 C411 C392 C393 0.47uF
C372 C356 C358 C357 C362 C359 C361 C360 0.047uF
C370 C363 C365 C364 C369 C366 C368 C367 0.047uF
C351 C344 C346 C345 C350 C347 C349 C348 0.047uF
C330 C326 C329 C328 C355 C352 C354 C353 0.047uF
C114 C116 C125 C127 C126 C128 C129 C130 2.2uF
C371 C325 C327 C331 0.47uF
C335 C332 C333 C334 0.47uF
C339 C336 C337 C338 0.47uF
C343 C340 C341 C342 0.47uF
C374 220uF
C379 C378 C377 C376 220uF
C438 C439 2.2uF
These caps shouldn't be needed, but just in case...
C445 C442 0.47uF
C449 C446 C448 C447 0.047uF
C440 C441 2.2uF
C450 C443 0.47uF
C456 C451 C453 C452 0.047uF
FPGA VCCO_x Bypass
C236 C221 C223 C222 C227 C224 C226 C225 0.047uF
C235 C228 C230 C229 C234 C231 C233 C232 0.047uF
C216 C209 C211 C210 C215 C212 C214 C213 0.047uF
C208 C182 C207 C206 C220 C217 C219 C218 0.047uF
C292 C277 C279 C278 C283 C280 C282 C281 0.047uF
C291 C284 C286 C285 C290 C287 C289 C288 0.047uF
C248 C241 C243 C242 C247 C244 C246 C245 0.047uF
C240 C237 C239 C238 C276 C249 C275 C274 0.047uF
C308 C293 C294 C295 C324 C309 C310 C311 0.47uF
C299 C296 C297 C298 C315 C312 C313 C314 0.47uF
C303 C300 C301 C302 C319 C316 C317 C318 0.47uF
C307 C304 C305 C306 C323 C320 C321 C322 0.47uF
C250 C252 C254 C256 C258 C262 C264 C266 C268 C260 2.2uF
C251 C253 C255 C257 C259 C263 C265 C267 C269 C261 2.2uF
C271 470uF
C419 C416 C454 C455 0.47uF
These caps shouldn't be needed, but just in case...
C423 C420 C422 C421 0.047uF
Rice University
Title
TAP - FPGA Board
Description
Decoupling Capacitors
Rev
x1
Date: Wednesday, September 22, 2004
Sheet 15 of 14