

# WARP FPGA Board User I/O Reference Design

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## 1 Connecting and Powering the WARP FGPA Board

## **1.1 Hardware Requirements**

- Power Supply for the WARP FPGA Board (12V-DC)
- Parallel Cable w/ JTAG (Requires 5V-DC supply for Xilinx Parallel Cable IV)
- 9-pin serial cable

### **1.2 Connecting the Board**

### 1.2.1 Connect and Power the Parallel Cable

- 1. Attach the parallel cable to the 25-pin port on your computer.
- 2. Attach the parallel cable to the board using the JTAG connector. (The connection to the board is underneath the board on the middle-left side)
- 3. Connect the parallel cable to a 5V-DC power supply. (The status light on the parallel cable should be yellow before the board is powered)

#### 1.2.2 Connect the Serial Cable

- 1. Attach the 9-pin serial cable to one of the COM ports of your computer
- 2. Attach the serial cable to the board. (The connection to the board is in the lower right hand corner on the right side of the board)

#### 1.2.3 Connect and Power the WARP FPGA Board

- 1. Connect a 12V-DC power supply to the FPGA board. (The connection to the board is in the bottom right corner on the bottom side)
- 2. Turn the power switch on. The switch is located to the left of the power connection. (Turning on the board should cause a number of LEDs to light. If there is no flash card in the flash port, then the LED near the flash port will blink until one is inserted. This is not needed now.)

## 2 Setting up the Project in XPS

## 2.1 Create New Project

- 1. Start XPS via Program Files  $\rightarrow$  Xilinx Platform Studio 8.1i  $\rightarrow$  Xilinx Platform Studio
- 2. At the Create new or open existing project window, select Base System Builder wizard (recommended) and click OK

🔶 Xilinx	Platform Studio		×
-Create	new or open existing project		
BSB	<u>Base System Builder wizard (recommended)</u>		
Ē	C Blank ≚PS project		
	C Open a recent project		
Brow	se for More Projects		•
Browse i	nstalled EDK examples (projects) <u>here</u>	<u>D</u> K	<u>C</u> ancel

Figure 1: Step 2 – Opening Dialog Box

- 3. For Project file, Either:
  - (a) Enter: C:/WARP/BoardTests/IOTest/system.xmp. Click OK and click Yes when asked if you would like to create the directory; OR
  - (b) Browse to the directory in which you would like to store your project. Create a new folder within this directory and open it. The file name should be system.xmp. Click Save. XPS will save all the various project files and folders in this project folder. Click OK to move to the next window.
  - (c) This readme assumes method one when giving locations. You must adjust your addresses accordingly if choosing to save the system elsewhere.



Create New XPS Project using BSB Wizard	
Project file C:/WARP/BoardTests/I0Test/system.xmp	Browse
Advanced options (optional)	
Use Repository paths	
	Bro <u>w</u> se
ОК	Cancel

Figure 2: Step 3 – Choose a directory for system.xmp



Figure 3: Step 3 – Click Yes to create the directory.



4. The Base System Builder - Welcome window should appear. Select I would like to create a new design, and click Next

Embedded Development-Kit Platform Studio         Welcome to the Base System Builder!         This tool will lead you through the steps necessary to create an embedded system.         Please begin by selecting one of the following options:         • I would like to create a new glesign         • I would like to load an existing .bsb settings file (saved from a previous session)	Base System Builder - Welcome		?
Welcome to the Base System Builder! This tool will lead you through the steps necessary to create an embedded system. Please begin by selecting one of the following options: I would like to create a new gesign I would like to load an existing .bsb settings file (saved from a previous session) Browse	Embedded Develor Platform Studio	oment. Kit	
<ul> <li>This tool will lead you through the steps necessary to create an embedded system.</li> <li>Please begin by selecting one of the following options:</li> <li>I would like to create a new design</li> <li>I would like to load an existing .bsb settings file (saved from a previous session)</li> </ul>	Welcome to the Base Sys	tem Builder!	
Please begin by selecting one of the following options:  I would like to create a new design I would like to load an existing .bsb settings file (saved from a previous session)  Browse	This tool will lead you through the steps nec	essary to create an embedded sy	ystem.
I would like to create a new design     I would like to load an existing .bsb settings file (saved from a previous session)	-Please begin by selecting one of the follow	ina options:	
C I would like to load an existing .bsb settings file (saved from a previous session)	<ul> <li>I would like to create a new design</li> </ul>		
Browse	C I would like to load an existing .bsb set	tings file (saved from a previous	session)
DIOWOO			Browse
			Contract

Figure 4: Step 4 – Welcome Screen



- 5. At the Select Board window, make the following selections and click Next:
  - Board vendor: Rice University CMC WARP Project
  - Board name: WARP FPGA and Radio Boards
  - Board revision: 1.0b

Base System Builder - Select Board	? ×
Select a target development board:	
Select board	
I would like to create a system for the following development board	
Board vendor: Rice University CMC - WARP Project	<b>.</b>
Board name: WARP FPGA and Radio Boards	-
Board revision: 1.0b	<b>.</b>
Note: Visit the vendor website for additional board support materials.	
Vendor's Website Contact Info	
Download Third Party Board Definition Files	
C I would like to create a system for a custom board	
Board description	
This board utilizes a Xilinx Virtex-II Pro FPGA XC2VP70-FF1517-6C. This XBD enables: 4 LEDs, 2 Hex Displays, 1 Reset Button, 4 Push-Buttons, SystemACE CompactFlash MCU interface, UART, 2 256kx32b ZBT SRAMs, Ethernet & OneWire EEPROM. It also includes support for the 4-slot radio controller and radio bridge peripherals.	
More Info < Back Next > Canc	el

Figure 5: Step 5 – Select Board window



6. Make sure PowerPC is your selected processor. Click Next

	. ·	5			
Architecture:	Device:	Pac <u>k</u> aj	je:	Speed grade:	
virtex2p	XC2VP70	) FF151	7 💌	-6	<b>v</b>
elect the process	or you would like to	) use in this design:			
Processors					
C MicroBlaze	DIPe	Port			
PowerPC			ЛАС	<b>E</b>	
·					
	Arbiter	PIR A	ater 405		
			RAM		
	OPB 10/100L Net	MEMO	32K B BRAN		
	Ethernet				
		SRAM			
Processor descri	iption				
The PowerPC	405 core is a 32-bit	implementation of a F	RISC PowerPC e	mbedded-envira	nment
architecture. I	t is integrated into the	he Virtex-II Pro and Vi	rtex-4 FX device	using the IP-Im	nersion
peripherals and	d utilities.	Connectibus initiasut	icture and extern	SIVE IF CUIES IOI	

Figure 6: Step 6 – Processor Selection window



- 7. The **Configure PowerPC** window should appear, make the following designations and click **Next**:
  - Processor clock frequency: 100.00 MHz
  - Bus clock frequency: 50.00 MHz
  - Processor configuration: FPGA JTAG
  - On-chip memory (OCM)
    - Data: 64 KB
    - Instruction: 128 KB
  - Cache setup should be *unchecked*

Base System Builder -	Configure PowerPC ?>
PowerPC	
System wide settings	
Reference clock	Processor clock Bus clock frequency:
100.00 MH-	
100.00 MHz	
Reset polarity: Activ	e HIGH 💌
-Processor configuration-	
Debug I/F	
FPGA JTAG	
C CPU debug <u>u</u> ser pin	sonly
C CPU debug and trac	e pins
C No debug	
	-On-chip memory (DCM)-
	(Use BRAM)
PowerP	
	Instruction:
	128 KB 🔻
Cache setup	
j <u>E</u> nable	
Mara Infa	/ Back Sancel

Figure 7: Step 7 – Configure PowerPC



- 8. The next windows are **Configure IO Interfaces**. Depending on the size of your window, a varying number of IO devices will be available on each screen. Make sure the following are checked (if an attribute is not enumerated, assume default configuration):
  - LED\_7SEGMENT
  - LED\_7SEGMENT\_1
  - LEDs\_4Bit
  - Push\_Buttons\_4bit
    - Check Use interrupt for the Push\_buttons\_4bit IO device.
       IMPORTANT: If you fail to do so now, consult the Help Documentation to learn how to add them once the project is created.
  - RS232
    - Peripheral: OPB UARTLITE
    - Baudrate: 57600
  - DIPSWs\_4bit
  - UNCHECK: SysACECompactFlash, Ethernet\_MAC, onewire\_0, radio\_controller\_0, radio\_bridge\_slot\_2, SRAM0\_ZBT\_512Kx32, and SRAM1\_ZBT\_512Kx32



🗇 Base System Builder - Configure IO Interfaces	? ×
The following external memory and IO devices were found on your board:	
Rice University CMC - WARP Project WARP FPGA and Radio Boards Revisi	ion 1.0b
Please select the IO devices which you would like to use:	
-IO devices	
LED_7SEGMENT	Data Chara
Peripheral: OPB GPI0	
Use interrupt	
LED_7SEGMENT_1	
Peripheral: OPB GPI0	Data Sheet
🔽 Use interrupt	
LEDs_4Bit	
Peripheral: OPB GPI0	
T Use interrupt	
- 🔽 Push Buttons 4bit	
Peripheral: OPP CPI0	Data Sheet
🔽 Use interrupt	
More Info	<u>C</u> ancel

Figure 8: Step 8 – Choosing Peripherals



🗇 Base System Builder - Configure Additional IO Interfaces	? ×
The following external memory and IO devices were found on your board: Rice University CMC - WARP Project WARP FPGA and Radio Boards Re Please select the IO devices which you would like to use: IO devices	vision 1.0b
Peripheral: OPB GPI0	Data Sheet
✓ Use interrupt     ✓ RS232     Peripheral:     OPB UARTLITE	Data Sheet
Baudrate (bits per seconds): 57600 Data bits: 8 Parity: NONE Use interrupt SysACE_CompactFlash	<u>D</u> ata Sheet
More Info	xt > Cancel

Figure 9: Step 8 – Choosing Peripherals cont.



🗇 Base System Builder - Configure Additional IO 🛙	interfaces ? 🗙
The following external memory and IO devices were found Rice University CMC - WARP Project WARP FPGA and F Please select the IO devices which you would like to use IO devices	d on your board: Radio Boards Revision 1.0b
onewire_0	<u>D</u> ata Sheet
Ethernet_MAC	<u>D</u> ata Sheet No <u>t</u> e
radio_controller_0	Data Sheet Note
<u>M</u> ore Info	ck <u>Next &gt;</u> <u>C</u> ancel

Figure 10: Step 8 – Choosing Peripherals cont.



🗇 Base System Builder - Configure Additional IO Interfaces	? ×			
The following external memory and IO devices were found on your board	:			
Rice University CMC - WARP Project WARP FPGA and Radio Boards Revision 1.0b				
Please select the IO devices which you would like to use:				
└IO devices				
- 🦵 radio_bridge_slot_2	Dele Chart			
	<u>D</u> ata Sheet			
	Note			
SRAM0_ZBT_512Kx32	Data Shoot			
	Data Sheet			
SRAM1_ZBT_512Kx32	Data Sheet			
	Eara auras			
More Info	ext > <u>C</u> ancel			

Figure 11: Step 8 – Choosing Peripherals cont.



 At Add Internal Peripherals, click Remove to the right of the plb\_bram\_if\_cntlr\_1 box. Click Next

📀 Base System Builder - Add Internal Pe	ripherals		? ×
Add other peripherals that do not interact with o "Add Peripheral" button to select from the list of If you do not wish to add any non-IO peripherals	off-chip component: available peripher s, click the "Next"	s. Use the als. button.	
			Add Peripheral
Peripherals			
plb_bram_if_cntlr_1		<b>(</b>	Remove
Peripheral: PLB BRAM IF CNTLR			Data Sheet
More Info	< Back	Next>	Cancel
		2 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	

Figure 12: Step 9 – Before Removing



🗇 Base System Builder - Add Internal Peripherals	? ×
Add other peripherals that do not interact with off-chip components. Use the "Add Peripheral" button to select from the list of available peripherals.	
If you do not wish to add any non-IO peripherals, click the "Next" button.	
	Add Peripheral
- Peripherals	
More Info	<u>C</u> ancel

Figure 13: Step 9 – After Removing



10. At Software Setup, UNCHECK Memory test and Peripheral selftest. RS232 should be chosen for STDIN and STDOUT. Click Next.

📀 Base System Builder - Software Setup 🛛 💡 🗙
Devices to use as standard input and standard output
STDIN: RS232
STDOUT: RS232
Sample application selection
Select the sample C application that you would like to have generated. Each application will include a linker script.
Memory test
Illustrate system aliveness and perform a basic read/write test to each memory in your system
Peripheral selftest
Perform a simple self-test for each peripheral in your system.
More Info

Figure 14: Step 10 – Software Setup



 If you chose to keep the "Memory test" or "Peripheral selftest" simply click NEXT through configuration menu(s). Click Generate at the System Created window. Click Finish to exit the builder. Click OK to beging using XPS.

Processor: PPC 40 Processor clock fr Bus clock frequen Debug interface: F On Chip Memory :	05 equency: 100.000000 MH cy: 50.000000 MHz PGA JTAG 192 KB	z		
he address maps t diting features of X	below have been automati KPS.	cally assigned. You	can modify them using l	the
Processor OCM: Core Name	instance Name	Race Addr	High Addr	
isbram_if_cntlr	iocm_cntlr	0xFFFE0000	0xFFFFFFFF	
Processor OCM	:			_
Core Name	Instance Name	Base Addr	High Addr	
dsbram_if_cntlr	docm_cntlr	0x20800000	0x2080FFFF	
PLB Bus : PLB_	V34 Inst. name: plb	Attached Compo	onents:	
Core Name	Instance Name	Base Addr	High Addr	
plb2opb_bridge	plb2opb_C_RNG0_B	A: 0x40000000	0x7FFFFFFF	
OPB Bus : OPB	_V20 Inst. name: opb	Attached Comp	oonents:	
Core Name	Instance Name	Base Addr	High Addr	
opb_gpio	LED_7SEGMENT	0x40000000	0x4000FFFF	
opb_gpio	LED_7SEGMENT_1	0x40020000	0x4002FFFF	
opb_gpio	LEDs_4Bit	0x40040000	0x4004FFFF	
	10 I D 0 10 10 10 10 10 10 10 10 10 10 10 10 1	Lo #0000000	Lo KOOCEEEE	_

Figure 15: Step 11 – Generate File



📀 Base System Builder - Finish	? ×
	The Base System Builder has successfully generated your embedded system! Click the Finish button to return to XPS to compile your hardware system and software application.
C:\WARP\BoardTests\IOTest\sy C:\WARP\BoardTests\IOTest\da C:\WARP\BoardTests\IOTest\et C:\WARP\BoardTests\IOTest\et C:\WARP\BoardTests\IOTest\sy C:\WARP\BoardTests\IOTest\sy	stem.mhs uta\system.ucf c\fast_runtime.opt c\download.cmd stem.mss stem.xmp
✓ Save settings file:	
C:\WARP\BoardTests\IOTest	\system.bsb
The settings file contains all the loaded in a future wizard session	e user's selections and inputs in the wizard session. It can be on.
More Info	< Back Cancel

Figure 16: Step 11 – Finish





Figure 17: Step 11 - Start Working



Figure 18: XPS Workspace after Base System Builder

## 2.2 Setting up the UserIO Test in XPS

 Click on the Applications tab in the left hand box. Right-click on Add Software Application Project... and choose Add Software Application Project... Type in UserIOTest, and click OK. You should see you project in the list of "Software Projects".

🗇 Xilinx Platform Studio - C:/WARP/BoardTests	/IOTest/system.xmp - [S
🕩 File Edit View Project Hardware Software De	evice Configuration Debug S
ji 🗶 🗠 🗠 🛛 📷 📬 🛛 🚑 🔚 🍕 🗋 🛛	à 🛱 🗛 🛛 🖻 🗗 🖏 🕻
×	0 00
Project Applications IP Catalog	
Software Projects	
- Add Software Application Project	╢ <b>▶</b> ▶♥♥
	▶₽₽₽
🔛 Default: ppc4U5_1_bootloop	

Figure 19: Step 1 – Adding a Software Project

📀 Add Software Ap	oplication Project  🗙		
Project Name Userl	OTest		
Note: Project Name of	cannot have spaces.		
Processor ppc405_0			
OK	Cancel		
-			

Figure 20: Step 1 - Name the project: UserIOTest

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WARP



 Right-click on Sources and choose Add Existing Files... Browse to c:/WARP/BoardTests/Files. You will want to add the following \*.c files:

- warplib.c
- UserIOTest.c



Figure 21: Step 2 – Adding Source Files



Figure 22: Step 2 - Select: UserIOTest.c and warplib.c



3. Next, right-click on **Headers** and choose **Add Existing Files...** You should already be in the correct folder.

If you do not see *warplib.h*, browse to **c:/WARP/BoardTests/Files**. You will want to add the following \*.h file:

• warplib.h





Select Source/H	leader File to Ad	d to Project			? ×
Look <u>i</u> n	Files		• +	🗈 💣 🎟 •	
	🖬 warplib.h				
My Recent					
Desktop					
My Documents					
My Computer					
<b>S</b>					
My Network	File <u>n</u> ame:	warplib.h		-	<u>O</u> pen
Places	Files of type:	C Headers (*.h)		•	Cancel

Figure 24: Step 3 - Select: warplib.h



4. Right-click on **Default: ppc405\_0\_bootloop** in the right hand menu. Uncheck **Mark to Intial**ize **BRAMs**. Afterward, there should be a red 'x' over the green arrow next to the name.

	- ×
Project Applications IP Catalog	
Software Projects	
🛅 Add Software Application Project	
	nitialize BRAMs
	ce
🖻 🐏 Project: UserIOTest 🛛 🗕 🚽 👘	
⊕- Processor: ppc405_0	
Executable: C:\WARP\BoardTests\IOTest\	User
Ė- Sources	
	st.c
-Headers	
C.7 WAIN 70 Odial estart lies/Waiplib.n	

Figure 25: Step 4 - Uninitializing BRAMs for the Default

 Right-click on Project: UserIOTest and check Mark to Initialize BRAMs. This step tells XPS to update the bitstream with your project. Afterward, there should no longer be a red 'x' over the green arrow next to the name.



Figure 26: Step 5 – Initializing BRAMs for UserIOTest



 Right-click on Project: UserIOTest and select Generate Linker Script. Make sure that each article under the Memory drop down menus is either set to iocm\_cntlr or docm\_cntlr. Click Generate



Figure 27: Step 6 – Generate Linker Script

Section	Size (bytes)	Memory	Section	Size (bytes)	Memory
vectors.	0x00000000	iocm_cntlr 💌	Heap	0x400	docm_cntlr
.text	0x00000000	iocm_cntlr 🔄	Stack	0x400	docm_cntlr
.rodata	0x00000000	docm_cntlr 💌			
.sdata2	0x00000000	docm_cntir 💌			
.sbss2	0x00000000	docm_cntlr 🔄			
.data	0x00000000	docm_cntlr 💌	Memories View:		
.fixup	0x00000000	docm_cntlr 🔽	Memory	Start Address	Length
.sdata	0x00000000	docm_cntlr 🔽	iocm_cntlr	0xFFFE0000	128K
.sbss	0x00000000	docm_cntlr 💌	docm_cntlr	0x20800000	64K
.bss	0x00000000	docm_cntlr 💌			
.boot0	0x00000000	iocm_cntlr 💌			
	Add Sec	tion Delete Section	ELF file used to	copulate section inform dTests\IOTest\UserIO	ation: Test\executable.elf
Soot and Vector	Sections:				
Section	Address	Memory	Output Linker So	ript: UserlOTest_linke	er_script.ld
boot	OVEFFFFFF	ioem entir			

Figure 28: Step 6 - Set memory to iocm\_cntlr or docm\_cntlr



 Choose Update Bitstream by either accessing it through Device Configuration on the top menu, or by clicking on the toolbar button (it says "Bram Init" on it). This process will take 10-15 minutes depending on your computing speed. Longer may indicate an improper setup (esp. steps 4,5,6 of this section).



Figure 29: Step 7 – Update Bitstream

8. The file is now ready to download to the board.

For help, please refer to the Help/FAQ page.



## 3 Running the Program

## 3.1 Ready Tera Term Pro

- 1. Open Tera Term Pro (Browse to "\Program Files\TTERMPRO\ttermpro.exe")
- 2. Choose **Serial** and select the appropriate COM port (the one to which the board is connected) from the **Port**: drop down menu.

Tera Term - [dis	connected] ¥T		_
File Edit Setup G	ontrol Window He	p	-
	Tera Term: New c	nnnection	Ē
	C TCP/IP	Host: myhost.mydomain	
		Telnet TCP port#: 23	
	• Serial	Port: COM1 _	
		OK Cancel Help	
			-

Figure 30: Step 2 – Tera Term Opening Dialog

3. Go to Setup → Serial Port... and change the Baud rate to 57600 (or whatever you specified in your project) from the drop down menu. Click OK

🛄 Tera 1	erm - COM1 ¥T
<u>F</u> ile <u>E</u> dit	Setup Control Window Help
	Setup       Control       Window       Help         Terminal       Window       Font         Font       Keyboard       Serial port         Serial port       General         Save setup       Restore setup         Load key map

Figure 31: Step 3 – Change Serial Port Settings

4. Tera Term is now ready to receive data.

NOTE: (If you are unsure about what rate you choose, this can be found by double-clicking **RS232** in the **System Assembly** view. It is the number given for **UART Lite Baud Rate**).

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era Term: Serial port s	etup	×
Port:	СОМ1 -	ОК
<u>B</u> aud rate:	57600 💌	
<u>D</u> ata:	8 bit 💌	Cancel
P <u>a</u> rity:	none 💌	
<u>S</u> top:	1 bit 💌	<u>H</u> elp
Elow control:	none 💌	
Transmit dela	у c <u>/c</u> har <mark>0 п</mark>	nsec/line

Figure 32: Step 3 – Serial Port Settings

## 3.2 Download Peripheral Test to the Board

(Assumes that the board has been connected and powered and that the bitstream has been generated successfully)

### 3.2.1 Method 1: Directly from XPS

 Download the bitstream to the board via Device Configuration → Download Bitstream or by clicking on the toolbar icon. (NOTE: XPS will recompile/regenerate everything that is not current before downloading the bitstream)



Figure 33: Step 1 – Download Bitstream

#### 3.2.2 Method 2: Using iMPACT

- 1. Open iMPACT via Program Files  $\rightarrow$  Xilinx ISE 8.1i  $\rightarrow$  Accessories  $\rightarrow$  iMPACT
- 2. When the **iMPACT Project** dialogue box pops up, click **Cancel** You should see the workspace.
- 3. Right-click on the workspace and choose Initialize Chain. Click OK at the Boundary-Scan Chain Contents Summary window.
- 4. You will see the **Assign New Configuration File** window. Click **Bypass** for the **xccace** (first) block.



- For the xc2vp70 block, browse to the location of your generated bitstream (e.g. "\ProjectFolder\implement Select this file and click Open. Click OK at the Add Virtex-II Pro/Virtex-4 Object Files window to return to the workspace.
- 6. Right click on the xc2vp70 block, and choose Program. Click OK to download to the board.

### 3.2.3 Method 3: Using ChipScope

- 1. Open ChipScope via Program Files  $\rightarrow$  ChipScope Pro 8.1i  $\rightarrow$  ChipScope Pro Analyzer
- 2. Click on the Open Cable/Search JTAG Chain button located in the upperleft corner.
- 3. Click **OK** at the window that pops up.
- 4. Right click on **xc2vp70** in the box in the upper-lefthand corner. Choose **Configure**.
- 5. Choose Select New File and browse to the location of your generated bitstream (e.g. "\ProjectFolder\impl
- 6. Click OK to download to the board.

## 4 FAQ

## 4.1 QUESTIONS

- 1. I forgot to enable interrupts for the push buttons when using Base System Builder. What do I do now?
- 2. What do I do if I didn't select one of the devices while using Base System Builder?
- 3. I get an error: "\*\*\* No rule to make target 'File name', needed by 'UserIOTest/executable.elf'. Stop"
- 4. Where can I get Tera Term Pro?
- 5. When I download my project (download.bit) to the board, nothing happens.
- 6. My project takes a longtime to generate the bitstream. Then it doesn't work. What's wrong?
- 7. Everything looks right, but when I try downloading to the board with iMPACT, nothing happens.
- 8. I get an error: "built in linker script:[line#] cannot move location counter backwards (from [address1] to [address2])"
- 9. When all else fails...

### 4.2 ANSWERS

- 1. I forgot to enable interrupts for the push buttons when using Base System Builder. What do I do now?
  - Copy the following lines of code into the MHS file:

```
BEGIN opb_intc
PARAMETER INSTANCE = opb_intc_0
PARAMETER HW_VER = 1.00.c
PARAMETER C_BASEADDR = 0x41200000
PARAMETER C_HIGHADDR = 0x4120ffff
BUS_INTERFACE SOPB = opb_newline
PORT Intr = Push_Buttons_4bit_IP2INTC_Irpt
PORT Irq = EICC405EXTINPUTIRQ
END
```

 Add these lines to the Push\_Buttons\_4bit instance in the MHS file (the first parameter in each device in the instance name):

PARAMETER C\_INTERRUPT\_PRESENT = 1
PORT IP2INTC\_Irpt = Push\_Buttons\_4bit\_IP2INTC\_Irpt

• Add this line to the ppc405\_0 instance in the MHS file:

PORT EICC405EXTINPUTIRQ = EICC405EXTINPUTIRQ

• Add these lines to the MSS file:

```
BEGIN DRIVER
PARAMETER DRIVER_NAME = intc
PARAMETER DRIVER_VER = 1.00.c
PARAMETER HW_INSTANCE = opb_intc_0
END
```

If this does not work, you will need to recreate the project using Base System Builder

#### 2. What do I do if I didn't select one of the devices while using Base System Builder?

- For the size of this project, it will be easier to simply recreate the project using Base System Builder. You can clear out the contents of the directory containing all the current files, or simply create a new folder in which to store the new project.
- 3. I get an error: "\*\*\* No rule to make target 'File name', needed by 'UserIOTest/executable.elf'. Stop"
  - Check to see that there are no spaces anywhere in the names of your source and header paths. XPS will give the above error if there are.

#### 4. Where can I get Tera Term Pro?

- http://www.vector.co.jp/authors/VA002416/teraterm.html
- 5. When I download my project (download.bit) to the board, nothing happens.
  - Did the lowest LED light up up downloading?
    - Yes? This indicates that the program has reached the board but that there may be something wrong with the serial connection. Check these and try again.
    - No? This indicates that the program never got to your board. Check the JTAG connection and try again. Then move to the following questions.
  - Do the baud rates match between your project and Tera Term?
    - See Step 3 and "NOTE" on the **Running the Program** page
  - Review Steps 2-6 of Setting up the UserIO Test in XPS
- 6. My project takes a longtime to generate the bitstream. Then it doesn't work. What's wrong?
  - Refer to steps 4-6 of Setting up the UserIO Test in XPS
- 7. Everything looks right, but when I try downloading to the board with iMPACT, nothing happens.
  - Try restarting TeraTerm and iMPACT. If this doesn't work, try the other methods listed in the **Download Peripheral Test to the Board** section
- 8. I get an error: "built in linker script:[line#] cannot move location counter backwards (from [address1] to [address2])"
  - You need to regenerate the linker script because of changes to your code. Repeat step 6 of **Setting up the UserIO Test in XPS**: here. Click OK at the request to overwrite the previous script.
- 9. When all else fails...
  - Consult the help documentation provided by Xilinx accessible through the help menu (Help  $\rightarrow$  EDK Online Documentation  $\rightarrow$  Click DOCUMENTS tab). You may find the following most helpful:
    - Platform Specification Format
    - OS and Libraries Reference Guide
    - Processor IP Catalog