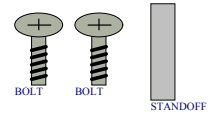
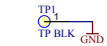
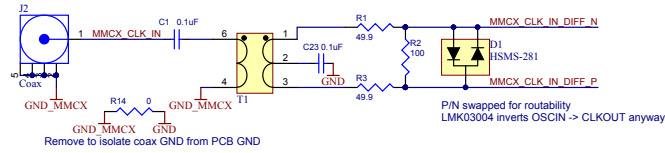


# Mango Communications CM-PLL - Clock Module for WARP v3 Rev 1.1

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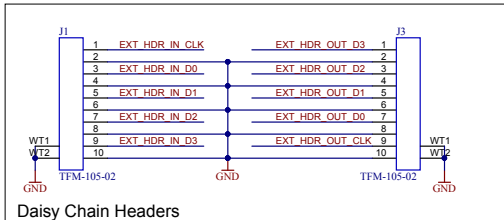
Ribbon cable connectors:  
Samtec TFM-105-02-x-d-WT-x  
Terminals (male pins)  
Dual-row 5 position (10 pins total) w/ weld tabs  
Pins numbered according to Samtec TFM-1XX-XX-XXX-D-XXX drawing  
Shroud notch/key at PCB edge on both connectors  
Even pins tied to ground

HDR\_IN connections:  
1: CLK\_IN  
3,5,7,9: Direct 2.5v FPGA I/O  
2,4,6,8,10: GND

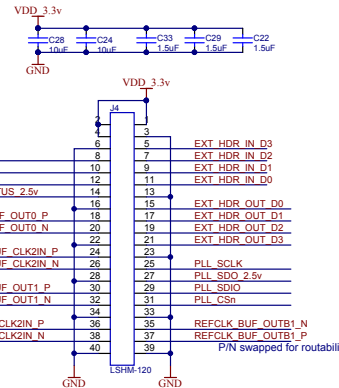
HDR\_OUT connections:  
1,3,5,7: Direct 2.5v FPGA I/O  
9: CLK\_OUT  
2,4,6,8,10: GND

Cables must connect pins:  
Evens: Evens (all GND)  
1:9  
3:7  
5:5  
7:3  
9:1

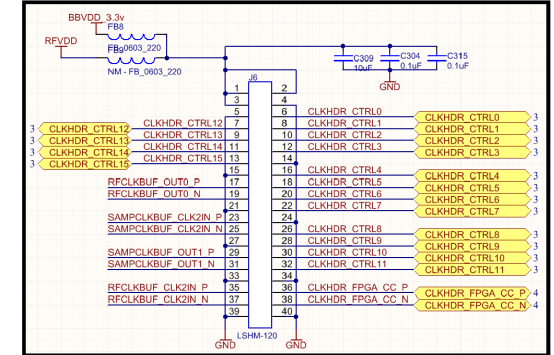
Suitable cables:  
Samtec FHSC-105-LL-LL-SBR-SBL-3 (LL.LL = Length in decimal inches)  
Samtec SFSD-05-28-F-LL-LL-DR-NUS



Daisy Chain Headers



## WARP v3 Main Board Circuit



REFCLKBUF\_OUT0: Output from main board RF reference clock buffer (AD9512 port OUT0; requires far-end LVPECL termination on clock module)

SAMPCLKBUF\_CLK2IN: Input to main board sampling clock buffer (AD9512 port CLK2; AC-coupled on main board)

SAMPCLKBUF\_OUT1: Output from main board sampling clock buffer (AD9512 port OUT1; requires far-end LVPECL termination on clock module)

REFCLKBUF\_CLK2IN: Input to main board RF reference clock buffer (AD9512 port CLK2; AC-coupled on main board)

CLKHDR\_FPGA\_CC: Connected to column 2 SRCC LVDS I/O on FPGA

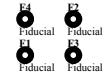
CLKHDR\_CTRL[15:0]: Connected to general 2.5v I/O on FPGA

Clock module interface uses same connector on main board and clock module. When mated main board pin N connects to clock module pin (N+1) for odd N.

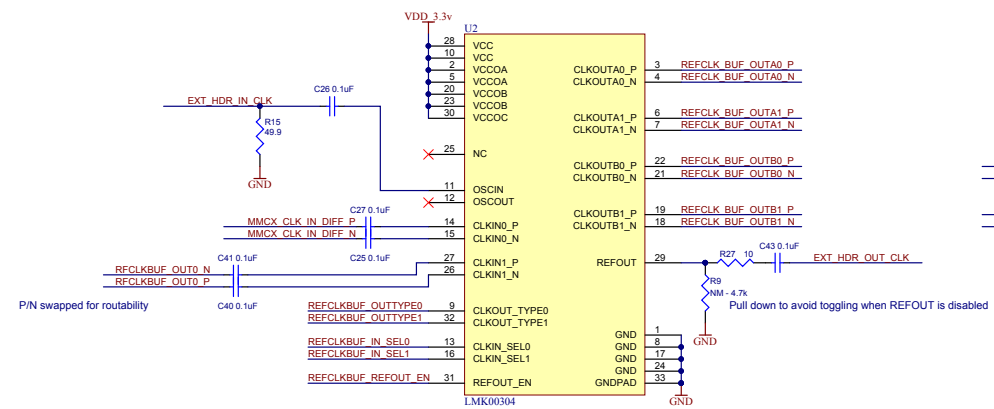
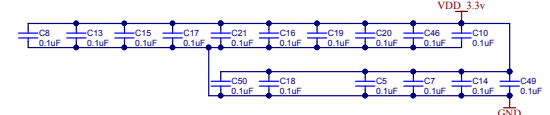
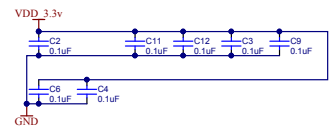
The clock module uses the same footprint as the WARP v3 main board. As a result, the connector symbols in the two schematics are mirror images.

Pin mapping:

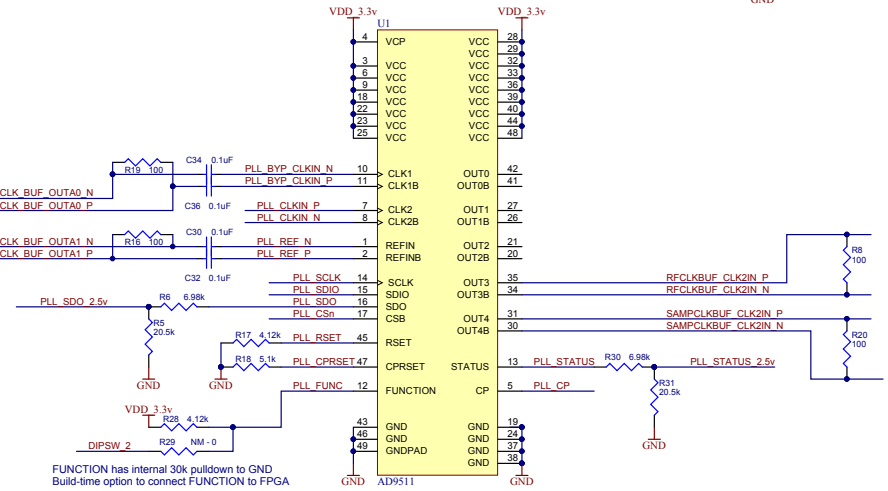
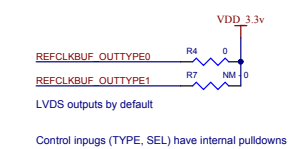
MB	CM
1	2
2	1
3	4
4	3
...	...
39	40
40	39



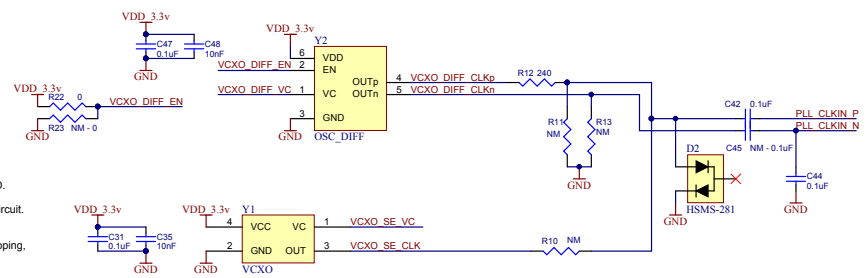
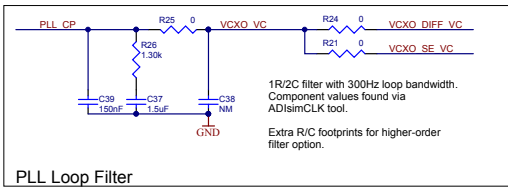
Design:	CM-PLL Clock Module	
Revision:	1.1	
Description:	Description	
Date:	9/11/2015	Sheet 1 of 2
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All clk inputs internally biased



FUNCTION has internal 30k pulldown to GND  
Build-time option to connect FUNCTION to FPGA



Footprints for large single-ended VCXO and smaller differential VCXO. Only one is mounted / connected to loop filter circuit. Many clock signal configurations supported (LVPECL term, diode clipping, voltage divider)