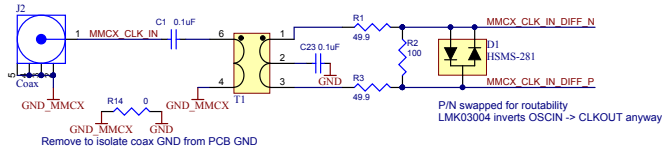
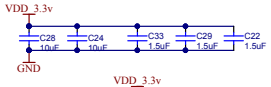
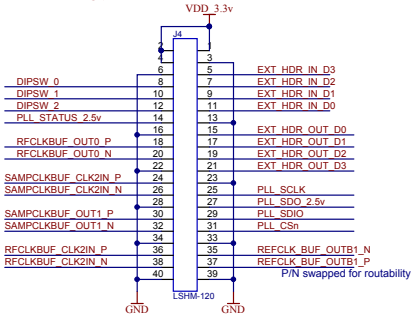
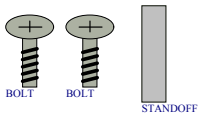
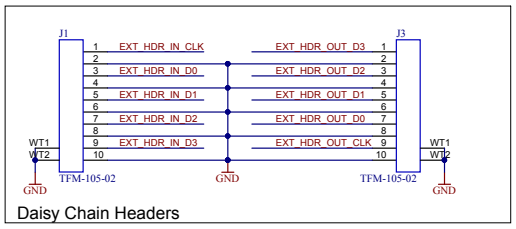
Mango Communications
CM-PLL - Clock Module for WARP v3
Rev 1.1











Ribbon cable connectors:
Samtec TFM-105-02-x-D-WT-x
Terminals (male pins)
Dual-row 5 position (10 pins total) w/ weld tabs
Pins numbered according to Samtec TFM-1XX-XX-XXX-D-XXX drawing
Shroud notch/key at PCB edge on both connectors
Even pins tied to ground

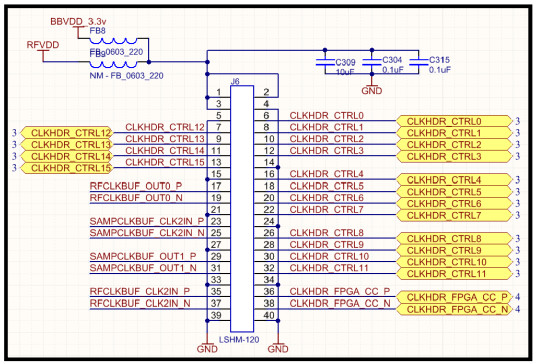
HDR_IN connections:
 1: CLK_IN
 3,5,7,9: Direct 2.5v FPGA I/O
 2,4,6,8,10: GND

HDR_OUT connections:
 1,3,5,7: Direct 2.5v FPGA I/O
 9: CLK_OUT
 2,4,6,8,10: GND

Cables must connect pins:
Evens:Evens (all GND)
1:9
3:7
5:5
7:3
9:1

Suitable cables:
Samtec FHSC-105-LL.LL-SBR-SBL-3 (LL.LL = length in decimal inches)
Samtec SFSD-05-28-F-LL.LL-DR-NUS

WARP v3 Main Board Circuit



RFCLKBUF_OUT0: Output from main board RF reference clock buffer
  (AD9512 port OUT0; requires far-end LVPECL termination on clock module)

SAMPCLKBUF_CLK2IN: Input to main board sampling clock buffer
  (AD9512 port CLK2; AC-coupled on main board)

SAMPCLKBUF_OUT1: Output from main board sampling clock buffer
  (AD9512 port OUT1; requires far-end LVPECL termination on clock module)

RFCLKBUF_CLK2IN: Input to main board RF reference clock buffer
  (AD9512 port CLK2; AC-coupled on main board)

CLKHDR_FPGA_CC: Connected to column 2 SRCC LVDS I/O on FPGA

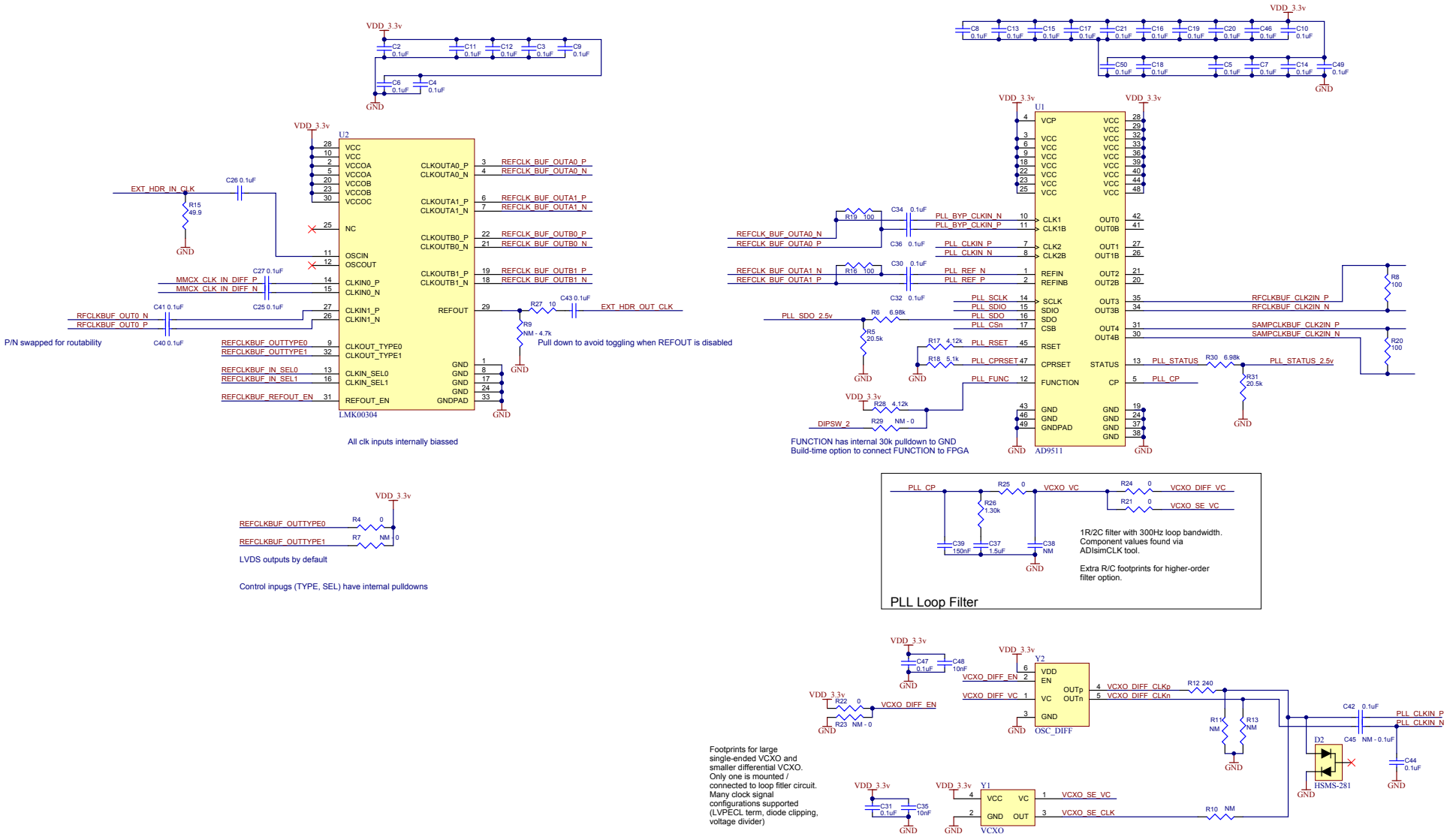
CLKHDR_CTRL[15:0]: Connected to general 2.5v I/O on FPGA

Clock module interface uses same connector
on main board and clock module. When mated
main board pin N connects to clock module
pin (N+1) for odd N.

The clock module uses the same footprint as
the WARP v3 main board. As a result, the
connector symbols in the two schematics are
mirror images.

Pin mapping:
MB | CM
1 | 2
2 | 1
3 | 4
4 | 3
...
39 | 40
40 | 39

Design:	CM-PLL Clock Module
Revision:	1.1
Description:	Description
Date:	9/11/2015
Sheet	1 of 2



Design:	CM-PLL Clock Module
Revision:	1.1
Description:	Description
Date:	9/11/2015
Sheet	2 of 2