

WARP, a Modular Testbed for Configurable Wireless Network Research at Rice

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Abstract—Wireless Open-Access Research Platform (WARP), developed at CMC lab, Rice University, provides a scalable and configurable platform for wireless network research. Its programmability and flexibility makes it easy to prototype and implement various physical and network layer protocols and standards. In order to share algorithms and implementations developed at different research centers, an online open-access repository is used so that wireless network researchers can collaborate to initiate multi-disciplinary system designs.

I. WARP PLATFORM ARCHITECTURE

Rice University's WARP [1,2] is a scalable, extensible and programmable wireless platform, built from the ground up, to prototype wireless networks. The platform architecture consists of four key components: custom hardware, platform support packages, open-access repository and research applications; all together providing a reconfigurable wireless testbed for students and faculty. Figure 1 shows the WARP boards in CMC lab.



Fig. 1. WARP boards in the CMC lab.

Custom Baseband Hardware: The WARP board is built up around Xilinx Virtex-II Pro FPGA as the primary communication processor, which along with the PowerPC processors embedded in the FPGA, provide a complete embedded programming environment for physical, medium access control (MAC) and network layer design. The dedicated multi-gigabit transceivers (MGTs) provide high speed board-to-board connections which make the WARP platform scalable and extendable. Moreover, four daughtercard slots on the WARP board can be used to connect the FPGA to the radio boards designed fully by Rice University students so that up to a 4×4 multiple-input multiple-output (MIMO) system can be built. Using these radio boards, the testbed may be used for wideband wireless communications in the 2.4 GHz/5 GHz ISM/UNII bands. The radio link, designed for MIMO applications, guarantees the phase coherency of carriers by sharing a reference clock.

Development Tools: The Xilinx "Platform Studio" tool is an integrated programming environment that is used to control both the physical layer and MAC layer implementations. For physical layer design, Xilinx "System Generator", integrated in MATLAB Simulink, provides abstractions for building and debugging high-performance DSP systems in MATLAB/Simulink using the Xilinx

Blockset. Moreover, the WARP board supports Simulink "hardware co-simulation" that expedites the simulation and debugging steps. For MAC and network layer design, the WARP platform supports "C" based applications on the PowerPC while interfacing the physical layer implementations in the FPGA fabric.

Online Open-Access Repository: The open-access repository [3], accessible from the Internet, is the central archive for all source codes, models, platform support packages, application building blocks, research applications, design documents and hardware design files associated with WARP. The contents of the repository are verified by the project administrator at Rice University.

II. WIRELESS NETWORK RESEARCH IMPACT

WARP provides a unique platform to develop, implement and test advanced wireless algorithms. All the design files are shared and documented through the online open-access repository [3]. A major benefit of custom physical and MAC layer designs is that they facilitate multi-layer system design by providing a flexible framework for researchers with expertise in a specific layer and little background in other layers to implement advanced protocols while abstracting away other layers.

The embedded PowerPC core in the Xilinx FPGA has been programmed using the C language to implement a flexible medium access development framework. This framework is in fact a set of software routines that can be used by network researchers to develop various advanced MAC and networking protocols while abstracting away the physical layer. Using this framework, various wireless networks, e.g. ad-hoc and multi-hop networks, as well as cooperative communication systems, e.g. relay networks, can be implemented on multiple WARP boards.

Furthermore, a 2×2 MIMO OFDM physical layer transceiver, i.e. two daughtercard radio boards for each WARP node, has been designed and implemented on the WARP hardware. The data streams are spatially multiplexed on both the antennas. In order to up-convert the baseband signals to the RF band, two daughtercard radio boards are used in each WARP node. Error correcting codes, e.g. LDPC, have also been developed to fit in the WARP framework, and further enhance the wireless link performance.

III. ACKNOWLEDGEMENT

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