Questions From Lab 1?
WARP Hardware

- WARP Hardware Components
  - FPGA Board
  - Radio Board
  - Clock Board
- FPGA Architecture
- Xilinx Platform Studio
- Processing & Storage
- External I/O
- User I/O
- Configuration
- Power
Xilinx XC2VP70 FPGA

- Extensive I/O & Logic Resources
- Embedded CPUs
- Extremely Flexible
- Powerful and Easy-to-Use Development Tools
• Augments FPGA’s Internal RAM Resources
• Usable as Instruction and/or Data Memory
• Two ICs, Each 512K x 32

4 MByte Onboard SRAM
Serial Port
Multi-Gigabit Transceivers
Ethernet Port
Serial Port
Daughtercard Connectors

- Provide Expanded Functionality via Custom Daughtercards
- Connect to FPGA Through General Purpose Digital I/Os
- Protocol Defined By Logic and Software Residing in FPGA
- Supports Radios, Video Cards, A/D & D/A Cards, Others
Generic 20-Pin Header

Switches, Buttons, LEDs
Compact Flash Slot
JTAG Header
USB Connector
12V DC Voltage Input
Questions?
Antenna Ports
Antenna Switch
Dual-Band Power Amp
RF Transceiver (MAX2829)

Digital Control Signals
Baseband Analog Signals
RF Signals

RF Rx
RF Tx

Analog I/Q
Analog RSSI

D/A Converters (AD9777)
A/D Converters (AD9248)
A/D Converter (AD9200)

Digital I/Q
Digital RSSI
Digital Control

Daughtercard Connectors
RF Transceiver (MAX2829)

D/A Converters (AD9777)

A/D Converters (AD9248)

A/D Converter (AD9200)

Digital I/Q

Analog I/Q

Analog RSSI

Antenna Ports

Antenna Switch

Dual-Band Power Amp

RF Rx

RF TX

Baseband Analog Signals

RF Signals

Digital Control Signals

Analog I/Q

Digital I/Q

Digital RSSI

Digital Control

Daughtercard Connectors

D/A Converters

AD9777

Analog I/Q

Analog RSSI

RF Tx

RF Rx

Baseband Analog Signals

RF Signals

Digital Control Signals

Baseband Analog Signals

RF Signals

Digital Control

Daughtercard Connectors
RF Transceiver (MAX2829)

D/A Converters
- AD9777

A/D Converters
- AD9248
- AD9200

Digital I/Q

Analog I/Q

Analog RSSI

Digital Control

Antenna Ports

Antenna Switch

Dual-Band Power Amp

RF Rx

RF Tx

Daughtercard Connectors

A/D Converters
- AD9248

A/D Converter
- AD9200

Analog I/Q

Digital I/Q

Digital RSSI

Digital Control Signals
Baseband Analog Signals
RF Signals

Analog I/Q

Digital Control

A/D Converters AD9248
- Dual-Band Operation: 2.4 GHz and 5 GHz
- Direct Conversion Between RF and Baseband
- 40 MHz Bandwidth Independent of Carrier Frequency
Clock Inputs

- Reference Frequency Input for Radio’s Up/Down Conversion
- May Be Supplied Externally via MMCX Connector
- May Be Supplied Locally via Onboard Oscillator
- Low-Frequency Signal is Up-Converted by Radio IC
Clock Inputs

- Reference Clock for A/D, D/A Converters
- Off-board via header or from FPGA
Questions?
Radio Reference Clock

- 20 MHz Output
- High-Precision Oscillator
Four MMCX Daughtercard Outputs

External Input

Forwarding Output
Radio Clock

20MHz TCXO

MMCX Jack

Clock Buffer (AD9510)

MMCX Jack
MMCX Jack
MMCX Jack
MMCX Jack
MMCX Jack
FPGA Logic Clock

- 40MHz Output
- Clocks FPGA and Radio Data
Four Twisted-Pair Daughtercard Outputs

Forwarding Output

External Input
Questions?
http://warp.rice.edu/trac

Hardware Platform
WARP Hardware

- WARP Hardware Components
  - FPGA Board
  - Radio Board
  - Clock Board

- FPGA Architecture
- Xilinx Platform Studio
XC2VP70 Resources
XC2VP70 Resources

- Embedded PowerPC processors
- 18-Bit by 18-Bit multipliers
- 18 Kbit block RAMs
- General purpose I/Os
- Multi-gigabit transceivers (MGTs)
- Reconfigurable user logic (Fabric)
18 Kbit Block RAMs

- Dual-ported for simultaneous reads and writes
- Simplifies construction of dual-port FIFOs
- Addressable via different aspect ratio on each port
- Coupled one-to-one with multipliers for extremely high throughput
- Operate independently and in parallel
- May be combined for increased capacity
XC2VP70 Resources

- 2 PowerPC processors
- 328 multipliers
- 328 block RAMs
- 964 general purpose I/Os
- 16 MGTs (8 on WARP FPGA board)
- 66176 4-input LUTs
- 66176 flip-flops (plus I/O registers)
Questions?
WARP Hardware

- WARP Hardware Components
  - FPGA Board
  - Radio Board
  - Clock Board
- FPGA Architecture
- Xilinx Platform Studio
Development Tools

Physical Layer

Network Protocols

MATLAB
Algorithm Development & Simulation

Platform Studio
C/C++ Protocol Implementation

System Generator
Piecewise Transition to Hardware Model

Low-Level HDL
& ASIP Development

Hardware Visibility

Automatic Implementation

PPC
Cores

FPGA

Radio

Logic

Radio

Radio

WARP Hardware

Radio
Hello World
Hello World

RS-232 PHY

Tx
Rx
Hello World

- FPGA
- Uart Core
- RS-232 PHY

Tx
Rx
Hello World
Hello World
Hello World

- FPGA
- IOCM
- DOCM
- PowerPC
- Uart Core
- PLB v46
- RS-232 PHY
- Tx
- Rx
Hello World

FPGA

IOCM

DOCM

PowerPC

PLB v46

Uart Core

RS-232 PHY

Tx

Rx

OF → IE → 20

Digital Display
Hello World

FPGA

IOCM

DOCM

PowerPC

PLB v46

GPIO Core

Uart Core

RS-232 PHY

Tx

Rx

OF → 1E → 20
Hello World
Lab 2: XPS Introduction

• Introduction to Xilinx Platform Studio
• Building a simple hardware platform
• Interacting with the WARP hardware