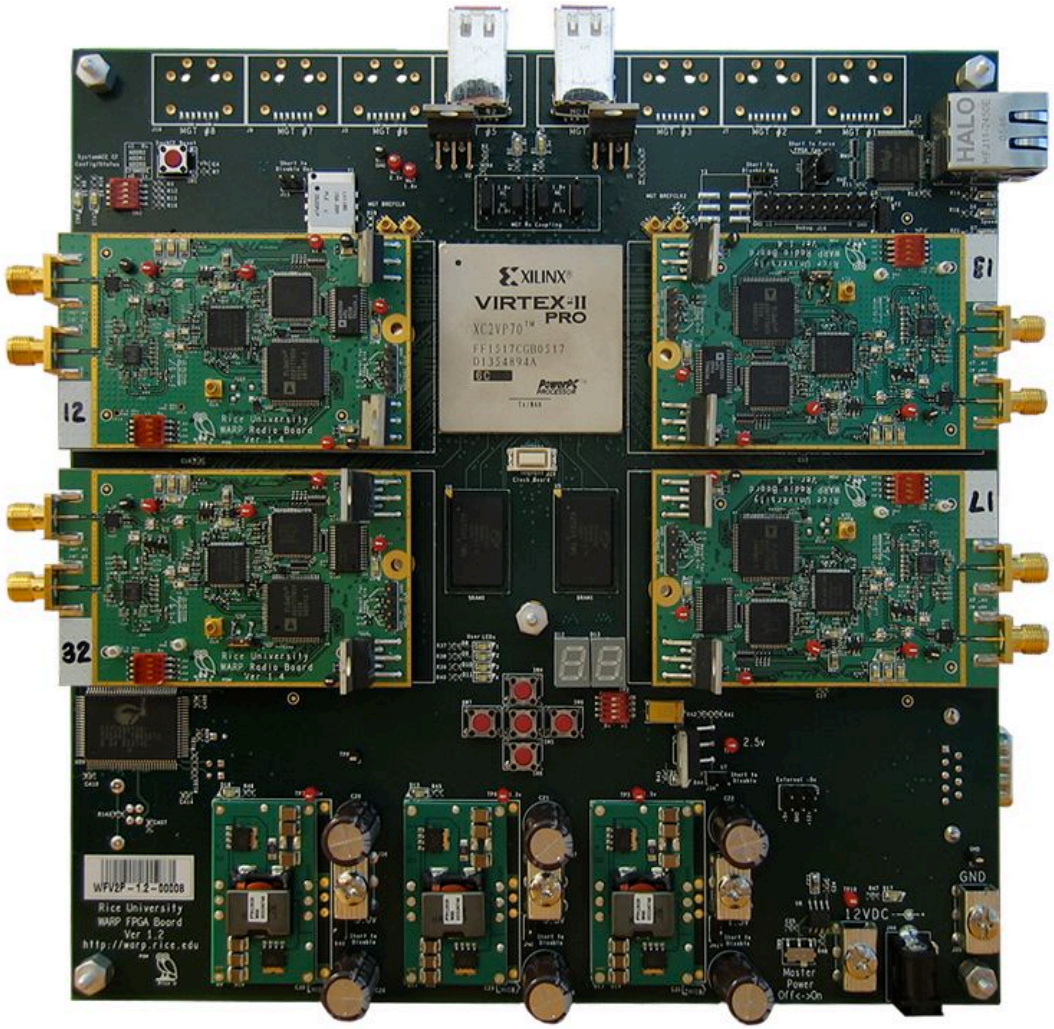
WARP: Hardware

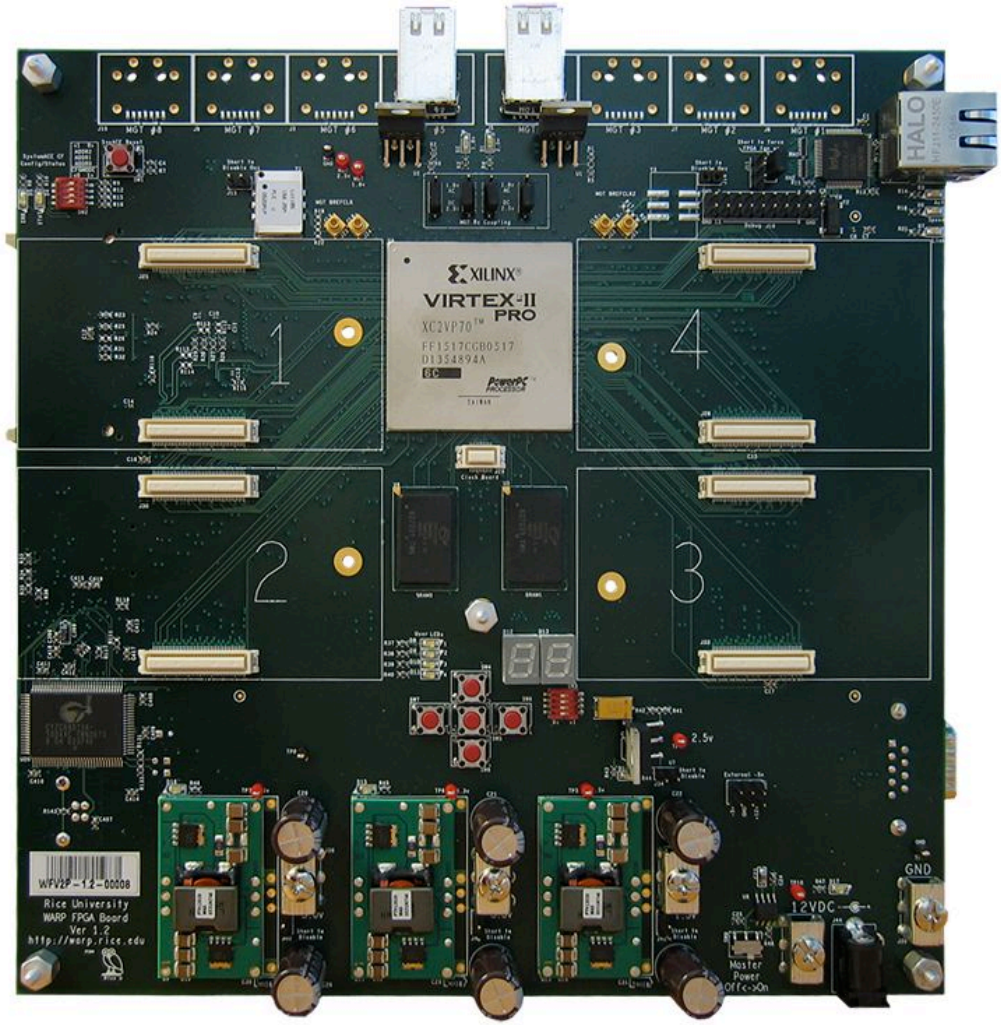
Charles Camp

WARP Workshop
Rice University
October 19, 2006

WARP Hardware

- WARP Hardware Components
  - FPGA Board
  - Radio Board
- FPGA Architecture
- Targeting WARP Hardware


XILINX
VIRTEX-II PRO
XC2VP70
Rice University
WARP Radio Board
Ver 1.4
WFV2F-1.2-00008
Rice University
WARP FPGA Board
Ver 1.2
http://warp.rice.edu
2.5v
12VDC
GND
Master
Power
Off<->On
HALO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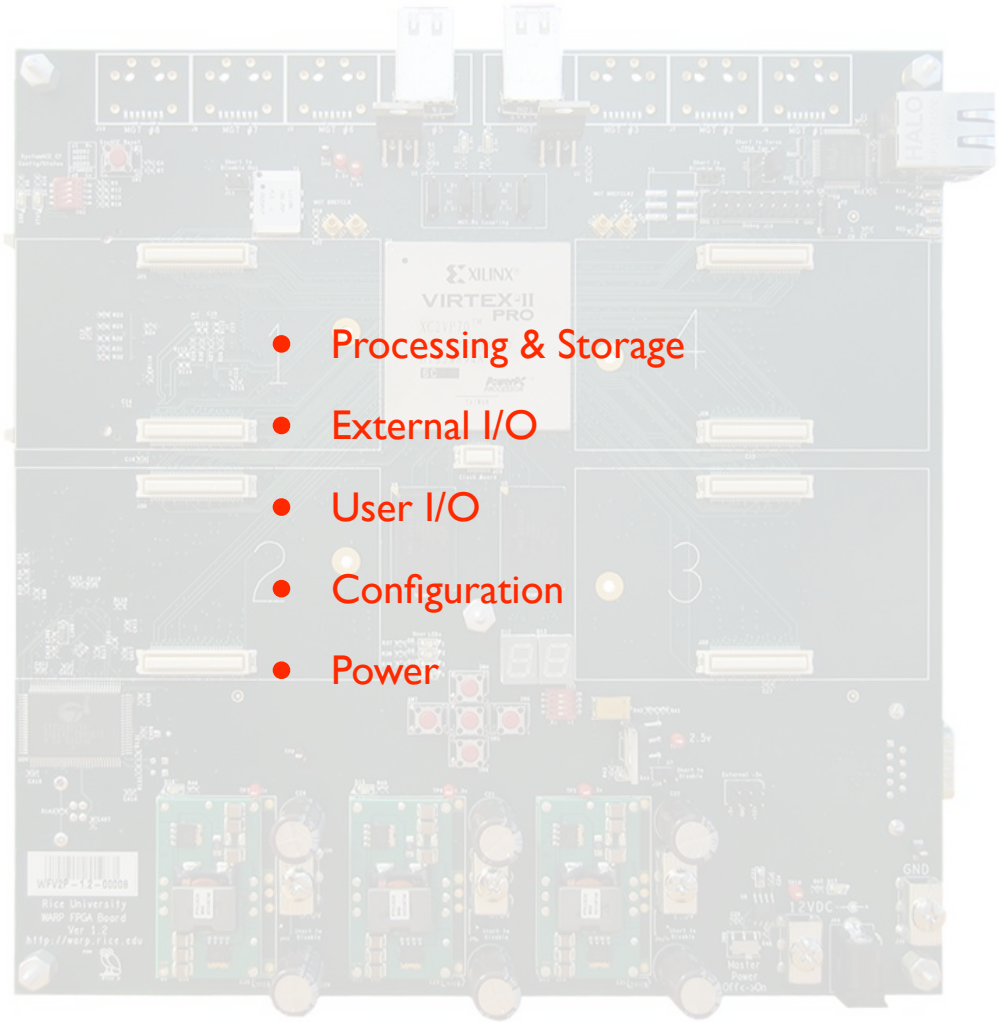


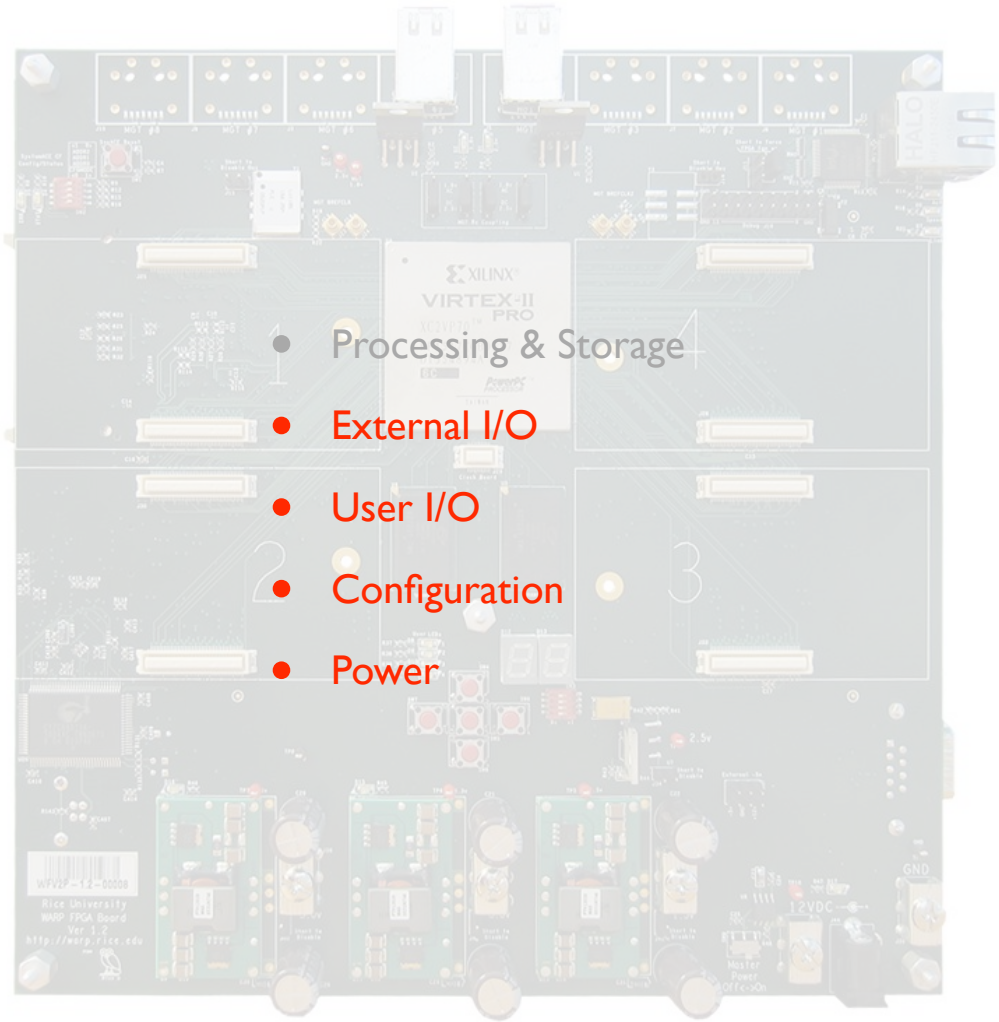
- Processing & Storage
- External I/O
- User I/O
- Configuration
- Power

Processing & Storage : XC2VP70 FPGA

- Extensive I/O & Logic Resources
- Embedded CPUs
- Extremely Flexible
- Powerful and Easy-to-Use Development Tools

Processing & Storage : 4 MByte Onboard SRAM

- Augments FPGA's Internal RAM Resources
- Usable as Instruction and/or Data Memory
- Two ICs, Each 512K x 32



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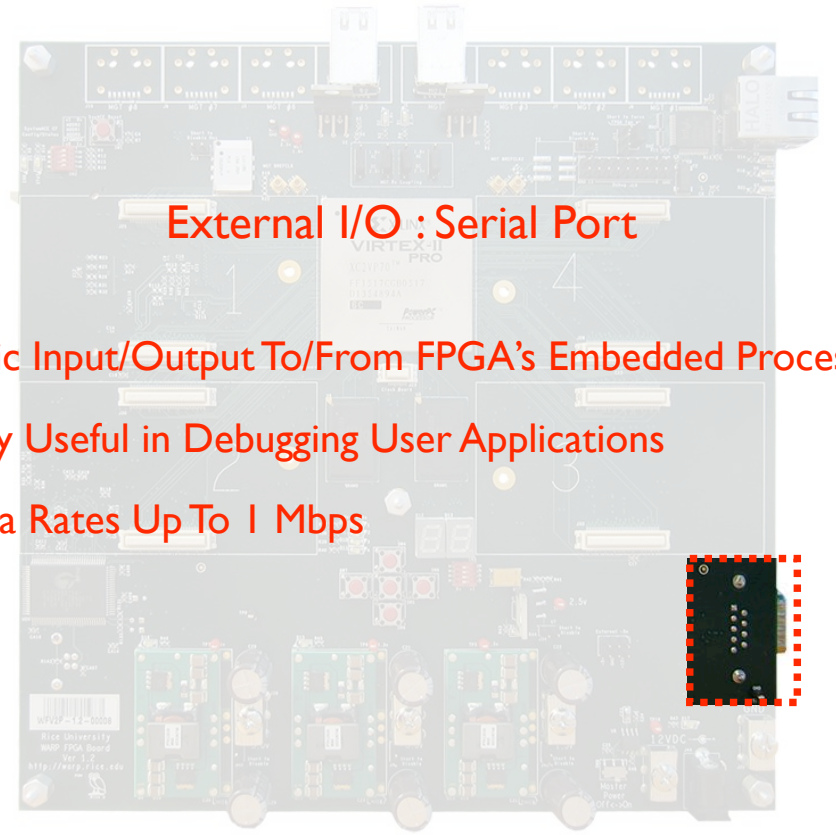
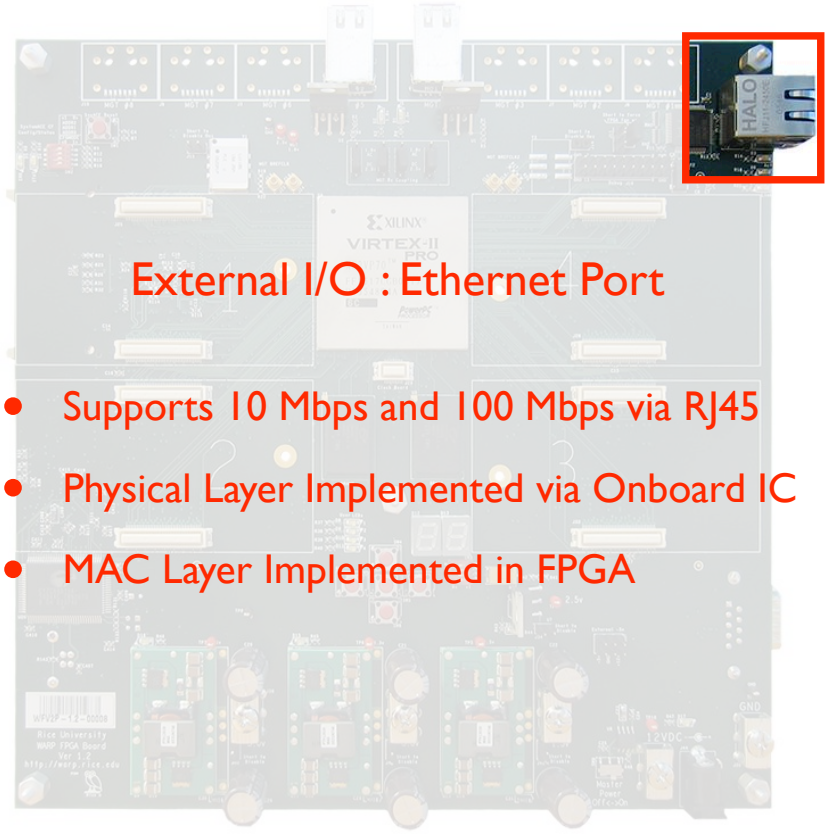
External I/O : Serial Port

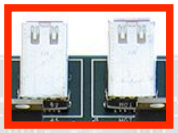
- Basic Input/Output To/From FPGA's Embedded Processors
- Very Useful in Debugging User Applications
- Data Rates Up To 1 Mbps





External I/O : Ethernet Port

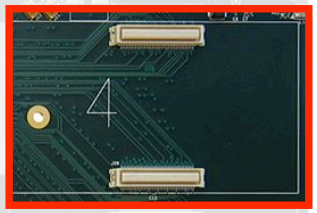
- Supports 10 Mbps and 100 Mbps via RJ45
- Physical Layer Implemented via Onboard IC
- MAC Layer Implemented in FPGA



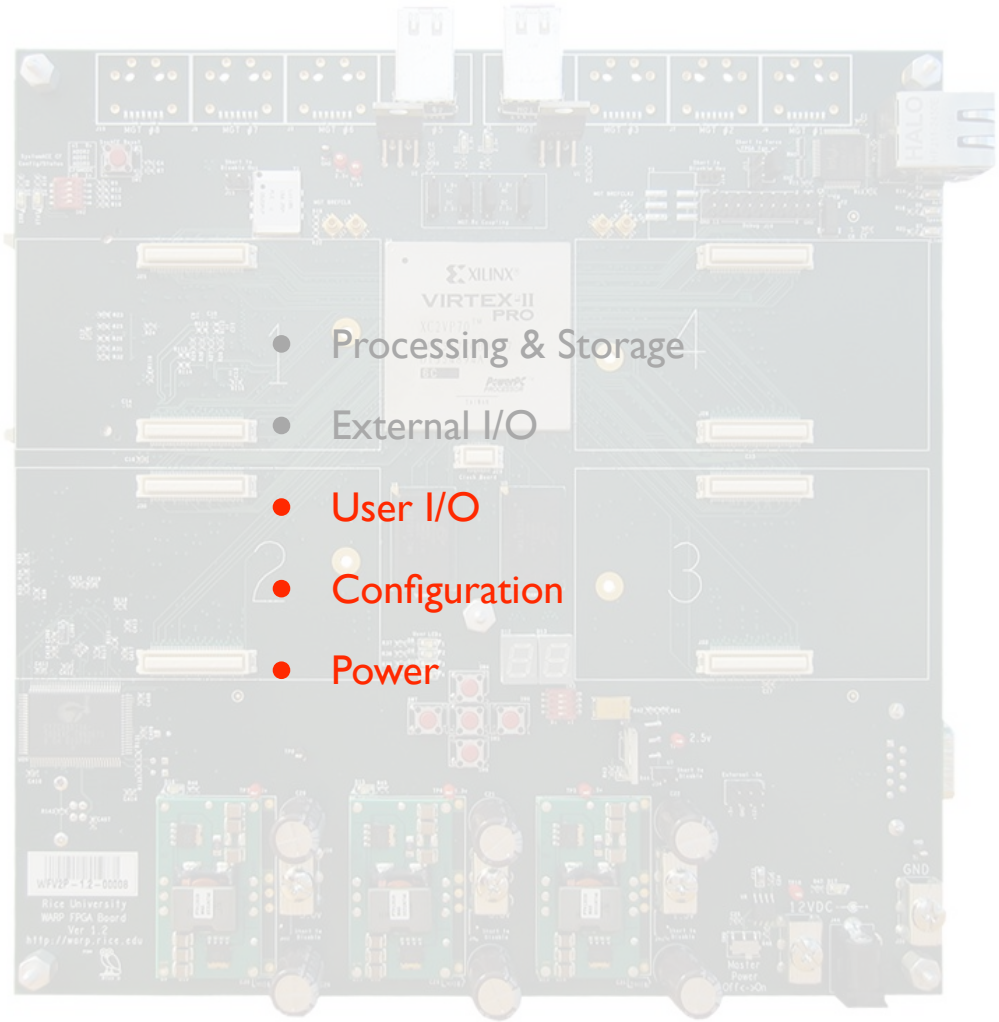
External I/O : Muli-gigabit Transceivers

- High Performance Serial Links (3.125 Gbps Full Duplex)
- Inter-Board Communication for Multi-FPGA Processing

External I/O : Daughtercard Connectors



- Provide Expanded Functionality via Custom Daughtercards
- Connect to FPGA Through General Purpose Digital I/Os
- Protocol Defined By Logic and Software Residing in FPGA
- Supports Radios, Video Cards, A/D & D/A Cards, Others



- Processing & Storage
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- User I/O
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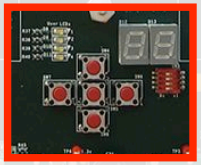
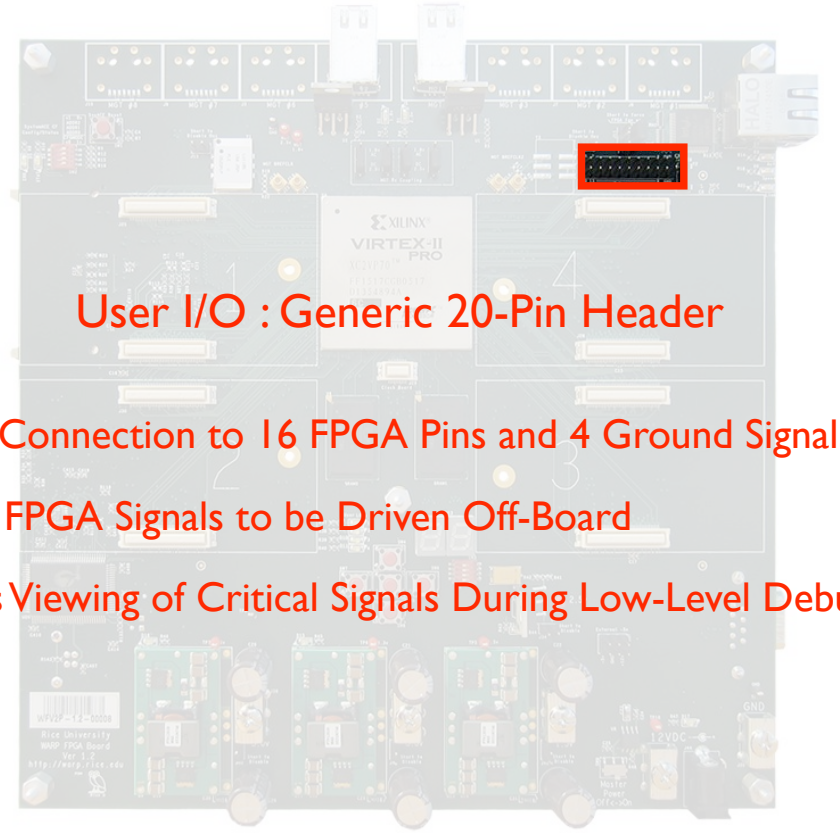
User I/O : Switches, Buttons, LEDs

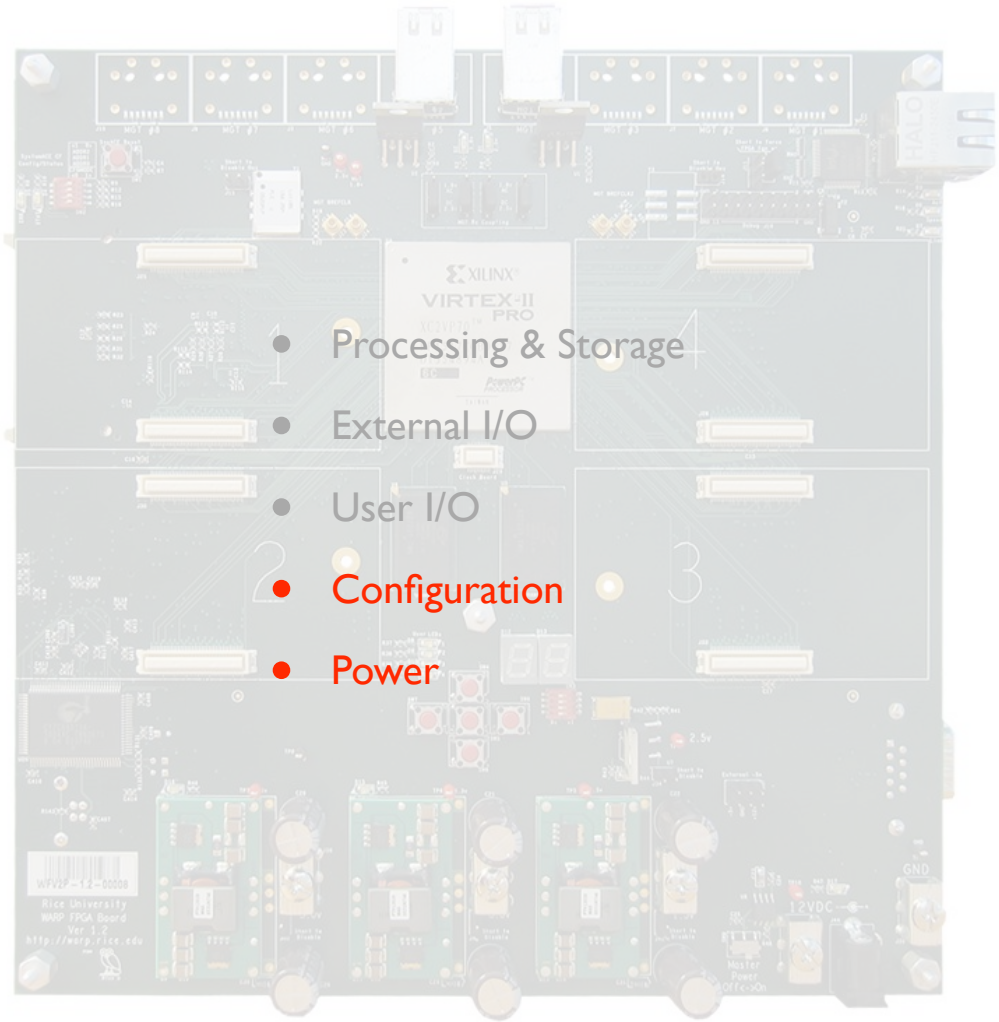
- Discrete and 7-Segment LEDs Provide Visible Status
- Buttons and Switches Provide Mechanism for User Input





User I/O : Generic 20-Pin Header

- Direct Connection to 16 FPGA Pins and 4 Ground Signals
- Allows FPGA Signals to be Driven Off-Board
- Enables Viewing of Critical Signals During Low-Level Debugging



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Configuration : Compact Flash Slot

- Configures FPGA From File(s) Stored on CF Card
- Multiple Programs Selectable via Switches on PCB
- Accessible by FPGA for Non-Volatile Storage

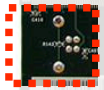
Configuration : JTAG Header

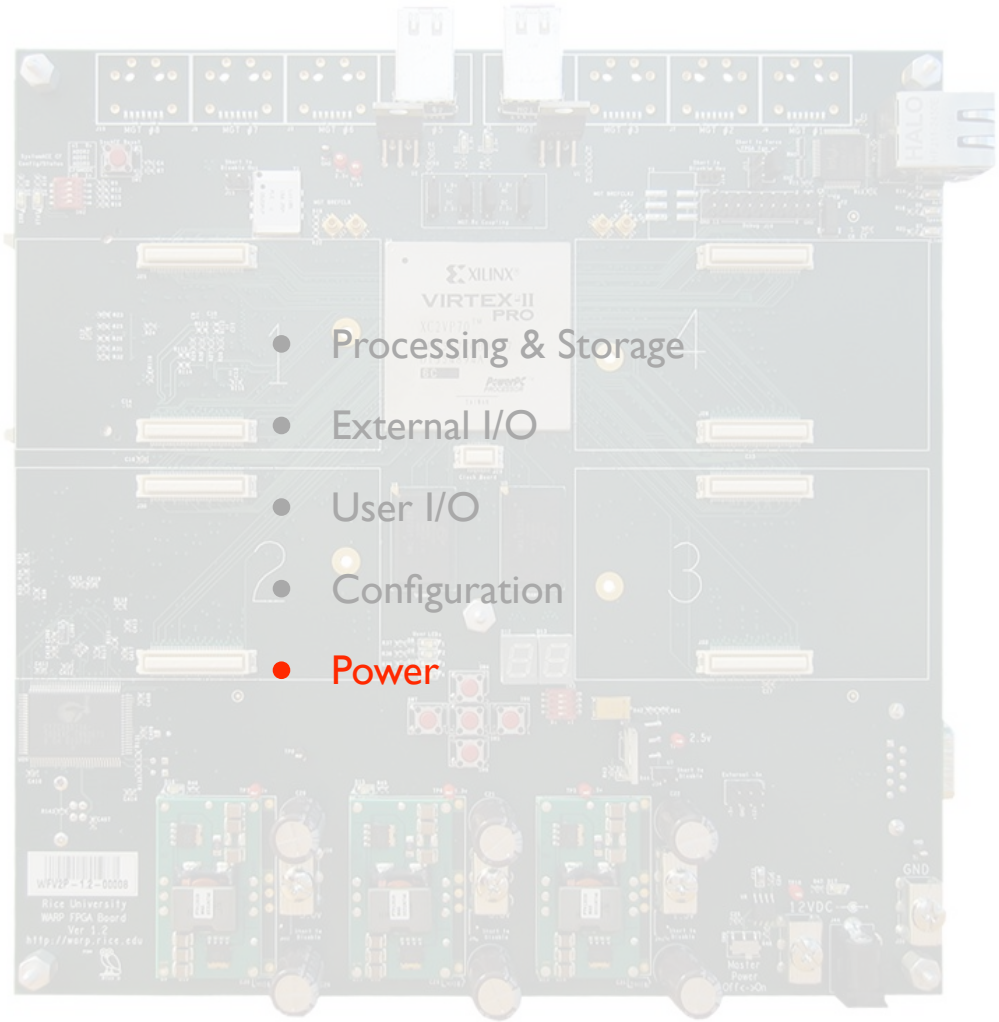
- Connects to Xilinx Parallel IV or Platform USB Configuration Cables
- Used to Configure FPGA From PC During Development

- Provides Interface for Debugging Tools (e.g. ChipScope)
- Supports Industry-Standard Boundary Scan Testing

Configuration : USB Connector

- Allows Direct Connection to PC via Standard USB Cable
- Emulates Functionality of Xilinx Platform USB Cable
- Eliminates the Need for Dedicated Configuration Cables





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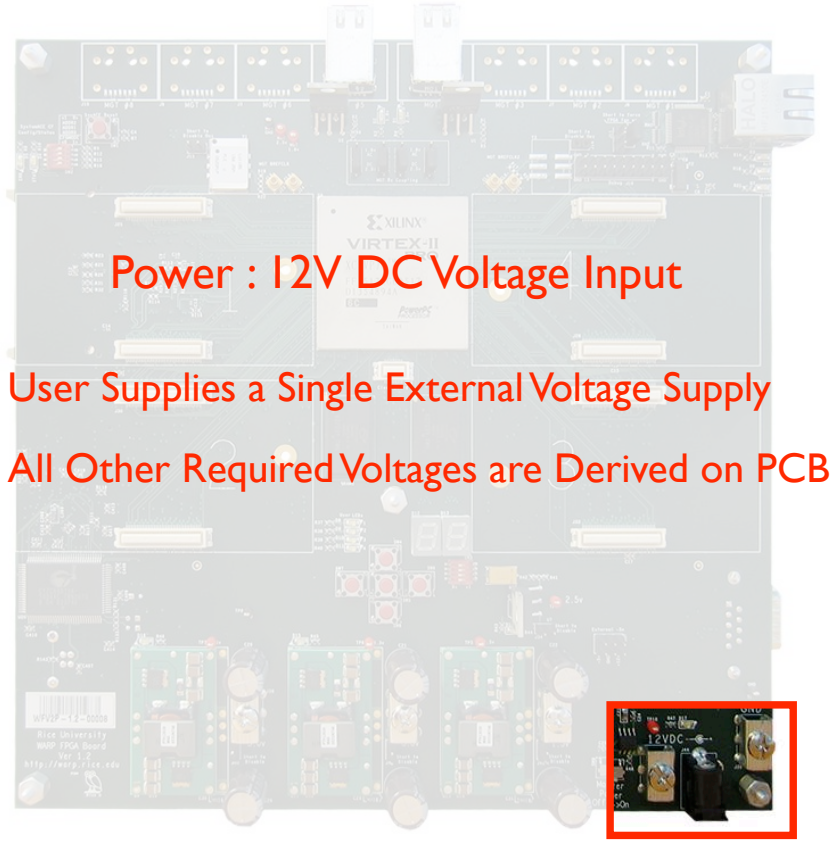
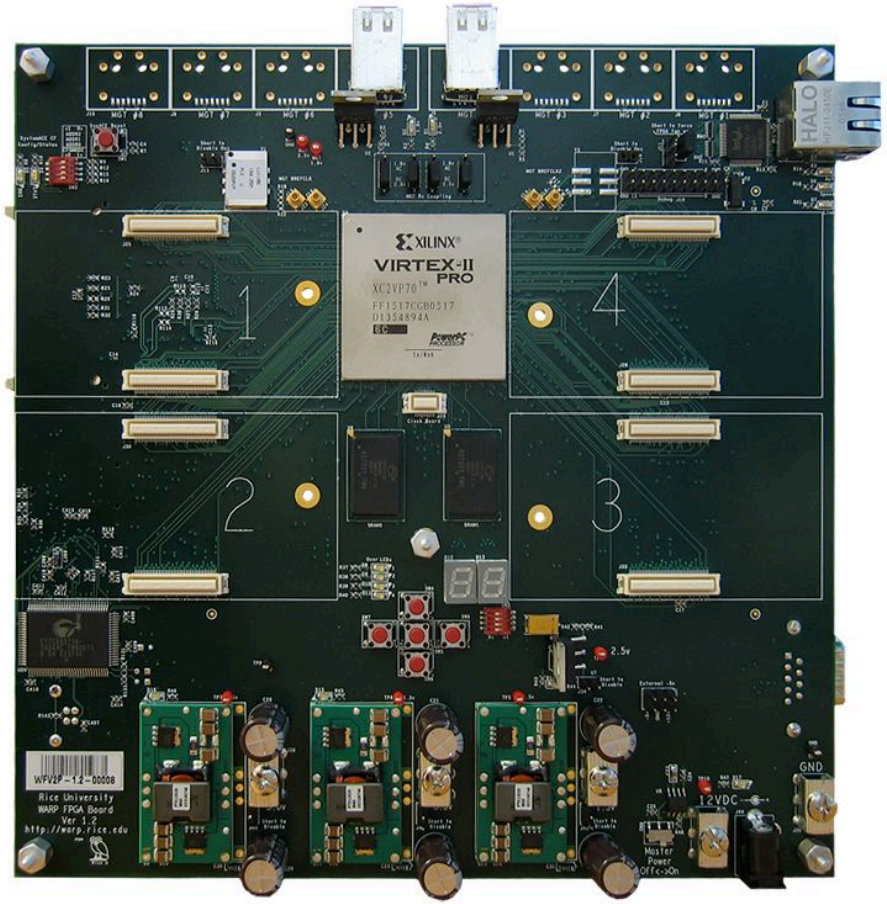


Power : 12V DC Voltage Input

- User Supplies a Single External Voltage Supply
- All Other Required Voltages are Derived on PCB

Questions?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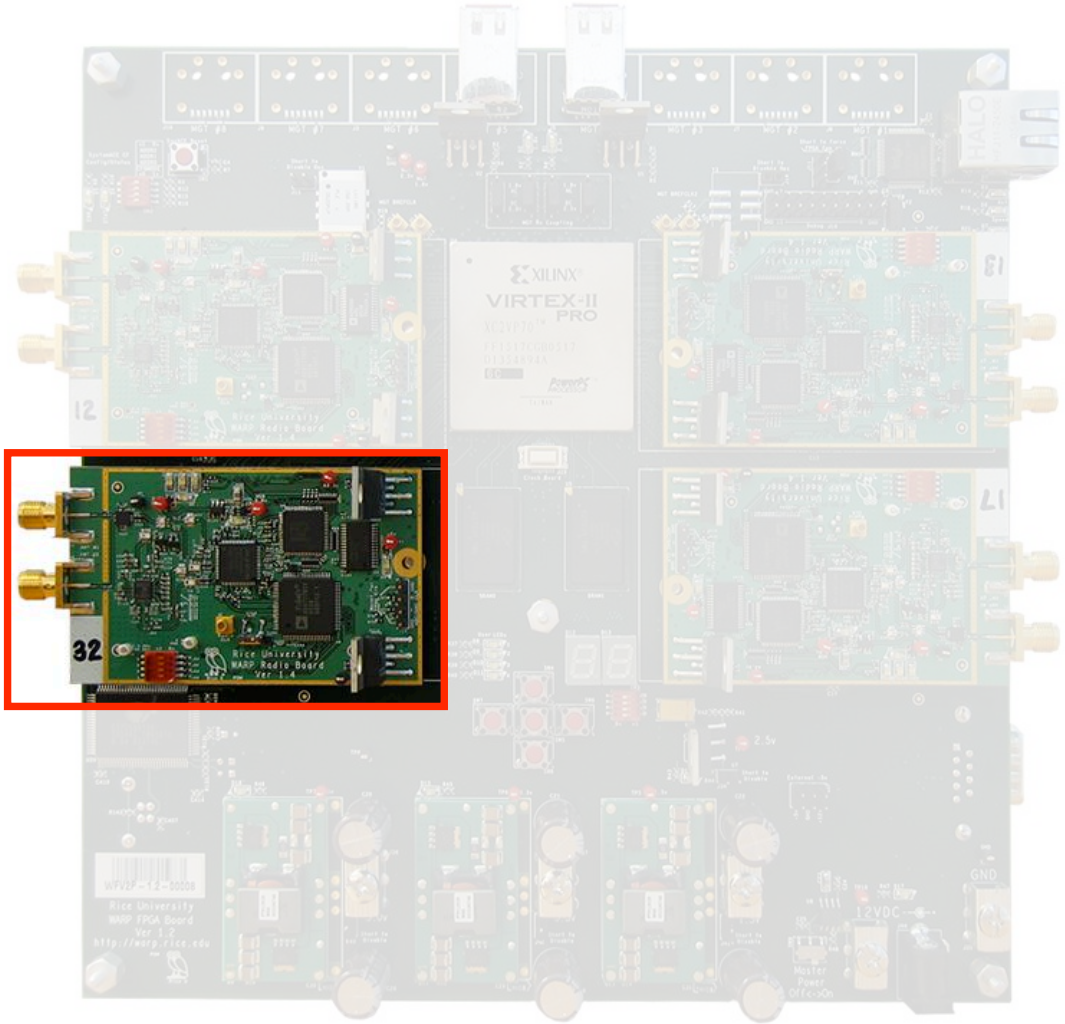
XILINX
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12
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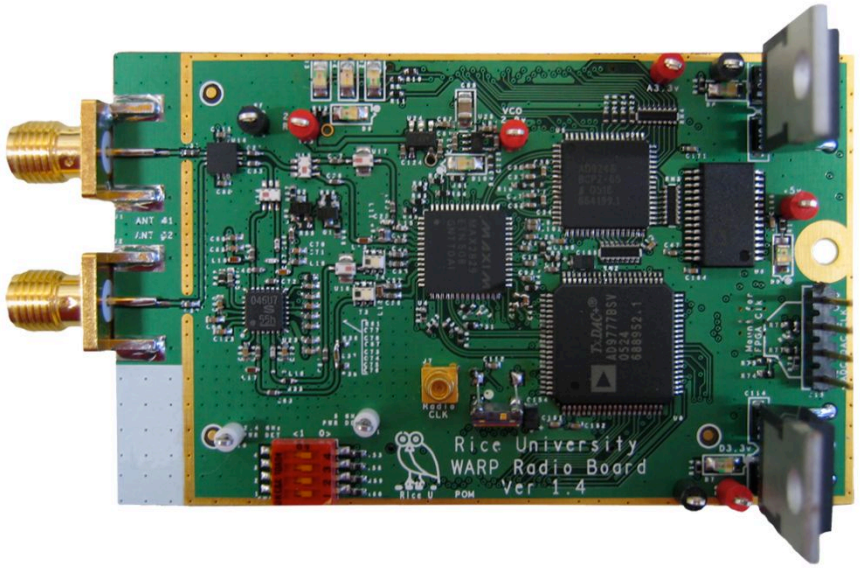
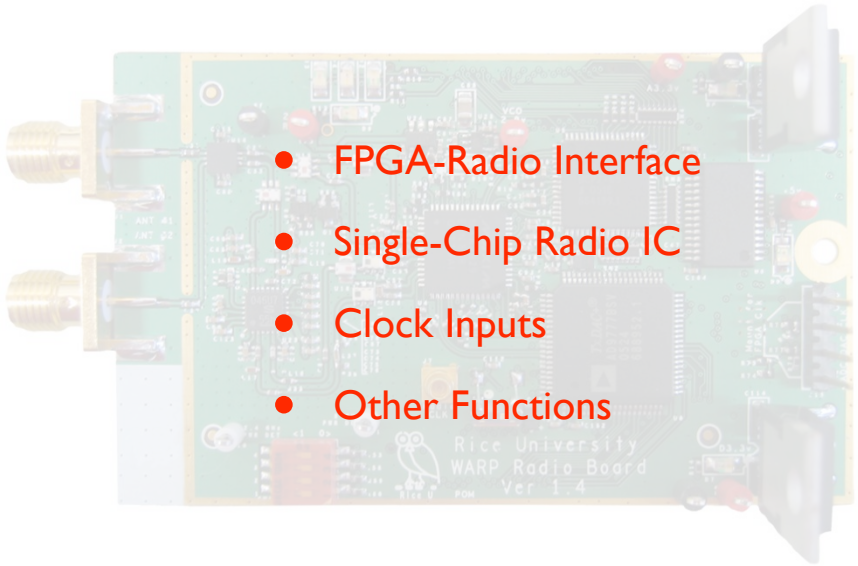
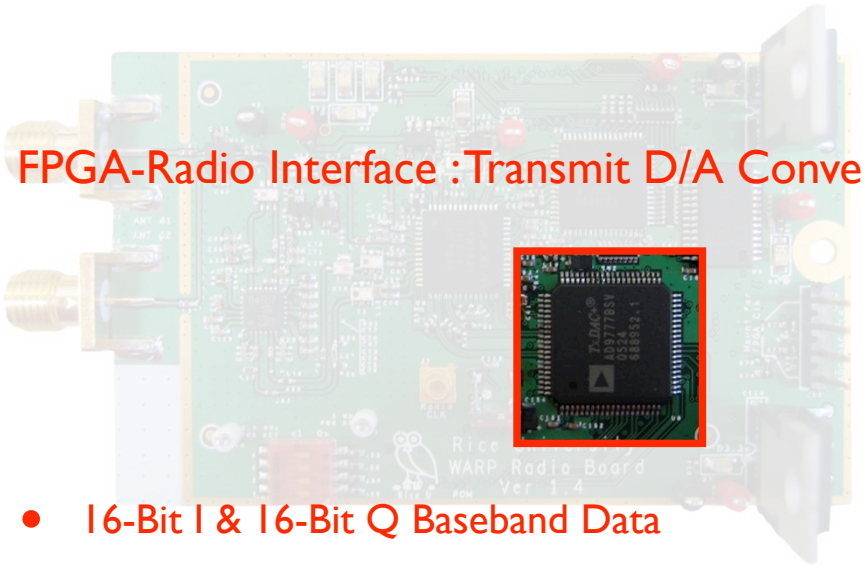

Rice University
WARP Radio Board
Ver 1.4



- FPGA-Radio Interface
- Single-Chip Radio IC
- Clock Inputs
- Other Functions

FPGA-Radio Interface : Transmit D/A Converters



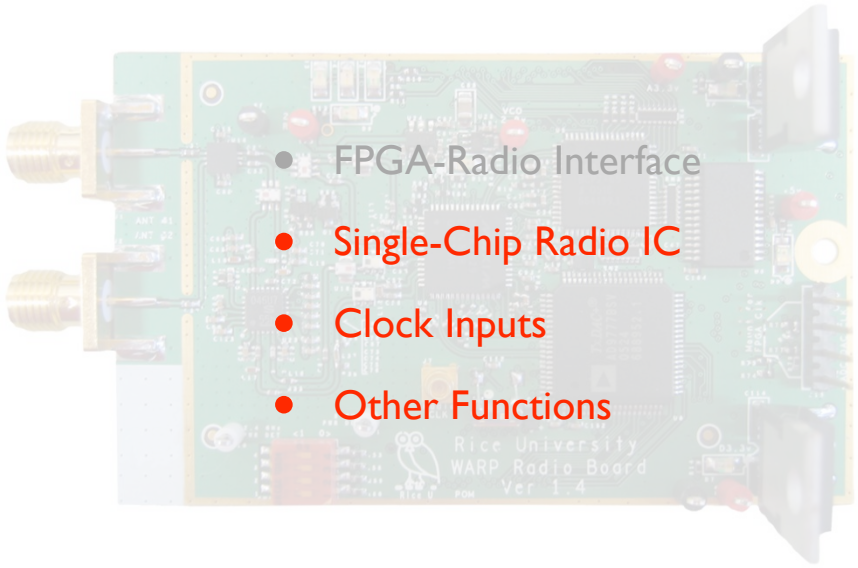
- 16-Bit I & 16-Bit Q Baseband Data
- Dual Converters for Optimum Parametric Matching

FPGA-Radio Interface : Receive A/D Converters

- 14-Bit I & 14-Bit Q Baseband Data
- Dual Converters for Optimum Parametric Matching

FPGA-Radio Interface : RSSI A/D Converter

- 10-Bit Representation of Radio Chip's Rx Signal Strength
- Values Used for Packet Detection in Physical Layer



- FPGA-Radio Interface
- Single-Chip Radio IC
- Clock Inputs
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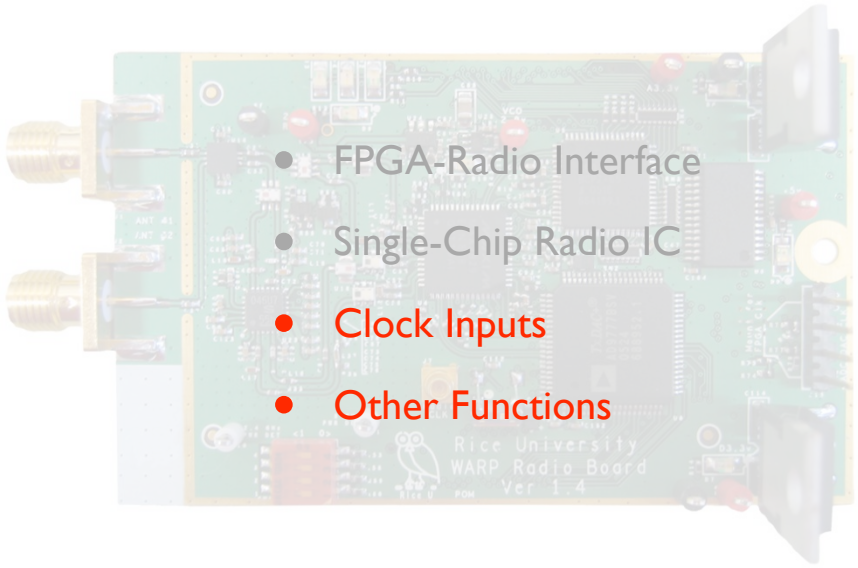
Single-Chip Radio IC : MAX2829

- Dual-Band Operation : 2.4 GHz and 5 GHz
- Direct Conversion Between RF and Baseband
- 40 MHz Bandwidth Independent of Carrier Frequency



- FPGA-Radio Interface
- Single-Chip Radio IC
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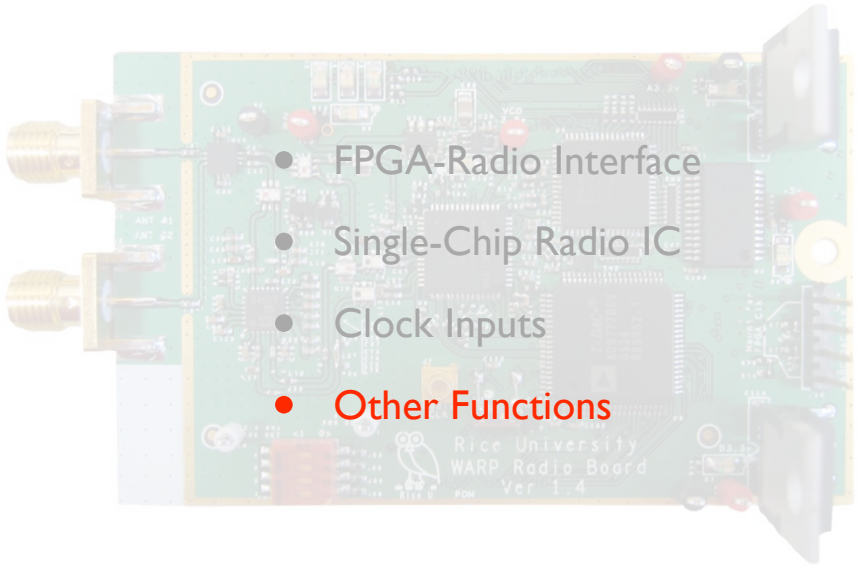
- Other Functions

Clock Inputs

- Reference Frequency Input for Radio's Up/Down Conversion
- May Be Supplied Externally via MMCX Connector

- May Be Supplied Locally via Onboard Oscillator
- Low-Frequency Signal is Up-Converted by Radio IC



- FPGA-Radio Interface
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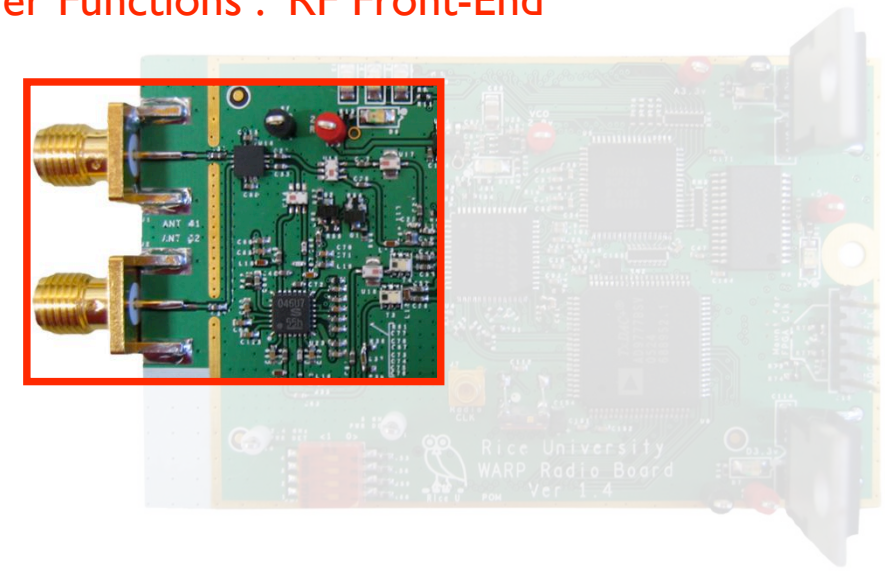
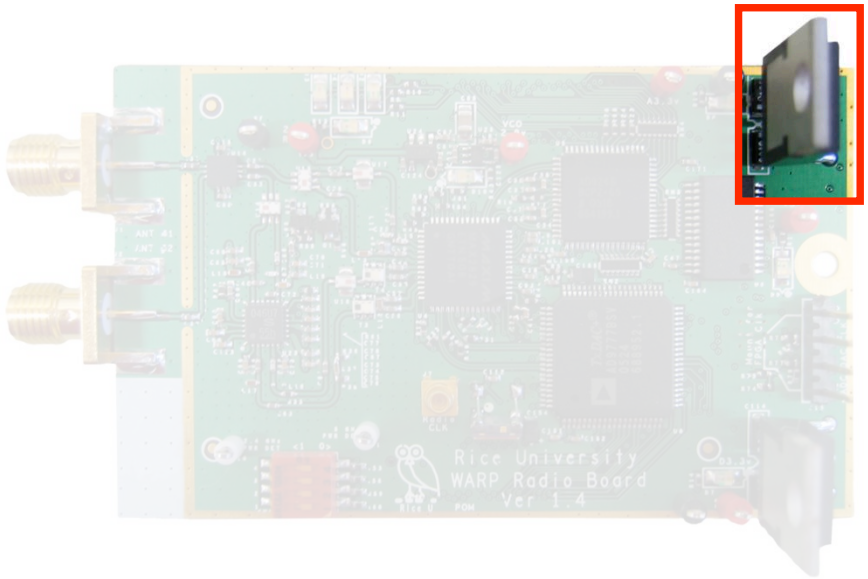
- Clock Inputs
- Other Functions

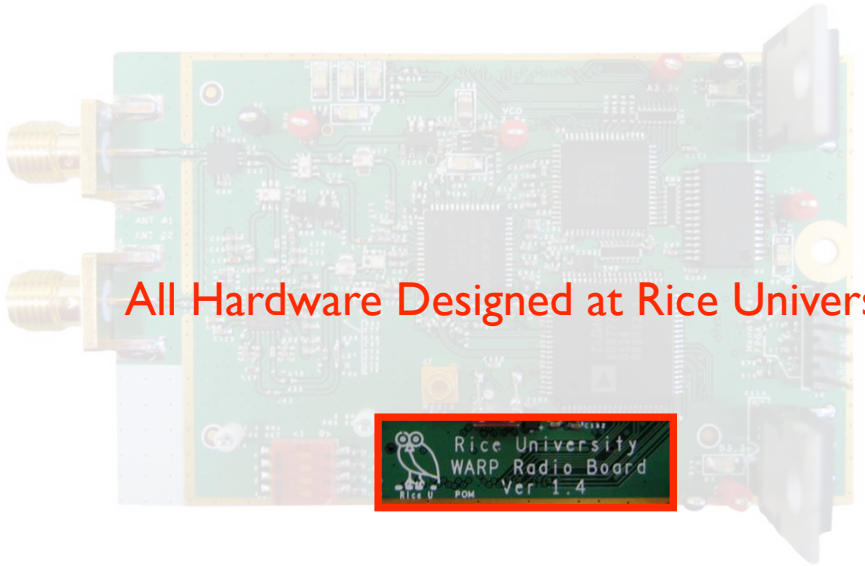
Other Functions : RF Front-End



Other Functions : Power Regulators



All Hardware Designed at Rice University



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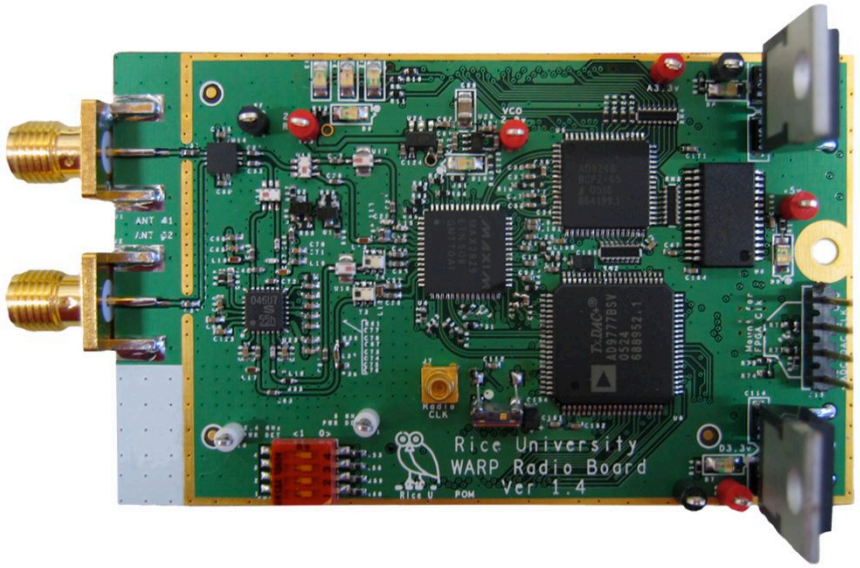
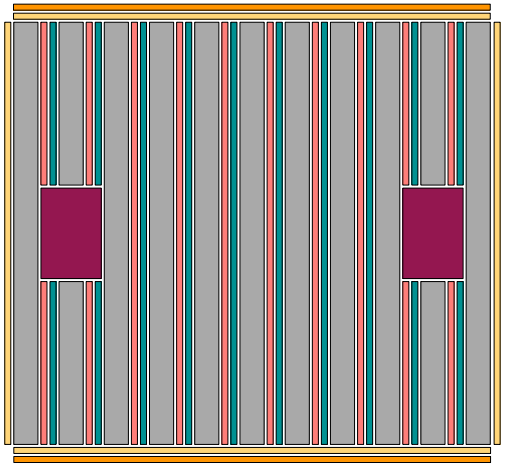


WARP Hardware

- WARP Hardware Components
  - FPGA Board
  - Radio Board
- FPGA Architecture
- Targeting WARP Hardware

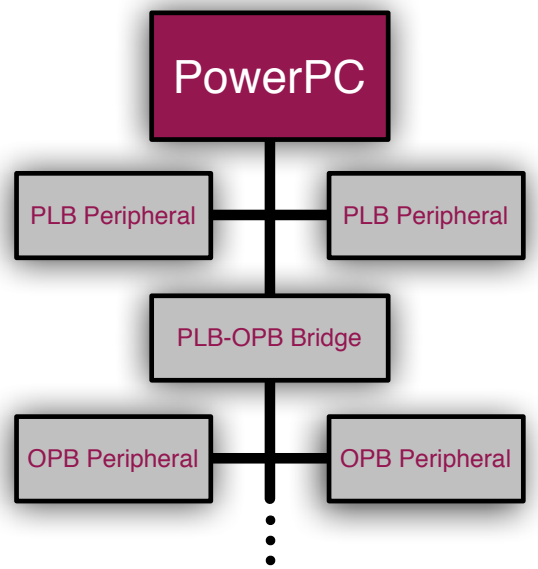
XC2VP70 Internal Resources

XC2VP70 Resources



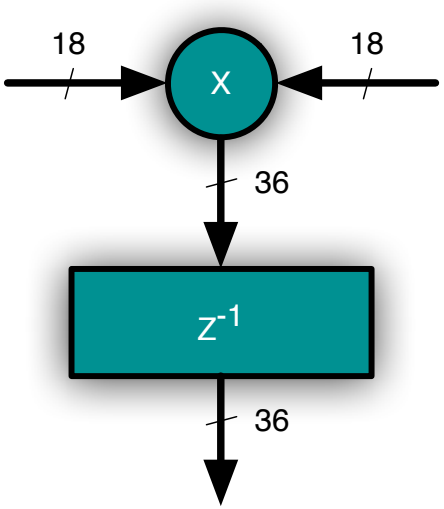
- Embedded PowerPC processors
- 18-Bit by 18-Bit multipliers
- 18 Kbit block RAMs
- General purpose I/Os
- Multi-gigabit transceivers (MGTs)
- Reconfigurable user logic (Fabric)

Embedded PowerPCs



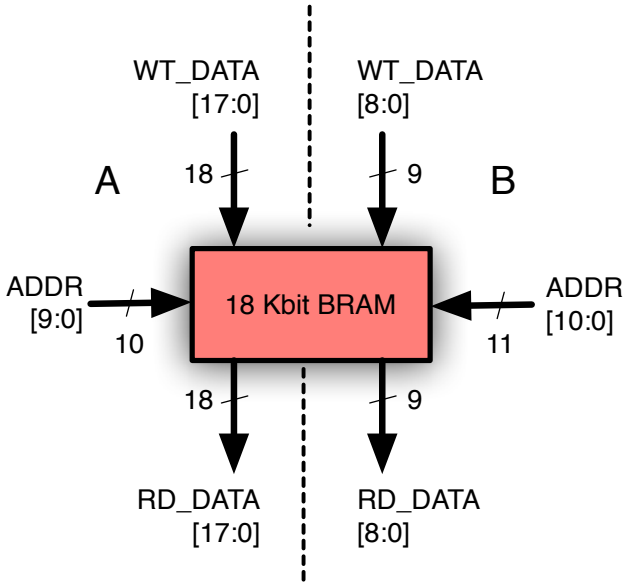
- PPCs connect to peripherals through the IBM Processor Local Bus (PLB)
- Alternative connections via the simpler On-Chip Peripheral Bus (OPB)
- PPCs execute user software for high-level control and data processing
- WARP tools simplify implementation of custom OPB-compliant peripheral cores

18-Bit x 18-Bit Multipliers



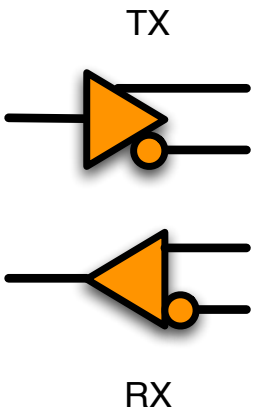
- Signed fixed-point inputs and outputs
- Fully synchronous operation with one result per clock cycle
- Tightly coupled with embedded block RAMs for very high throughput
- Operate independently and in parallel
- May be combined to support larger operands and results

18 Kbit Block RAMs



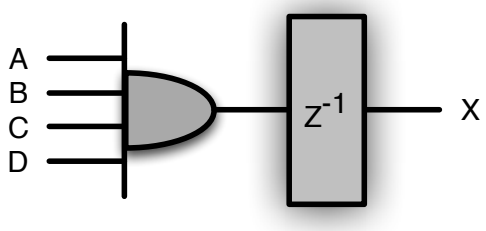
- Dual-ported for simultaneous reads and writes
- Simplifies construction of dual-port FIFOs
- Addressable via different aspect ratio on each port
- Coupled one-to-one with multipliers for extremely high throughput
- Operate independently and in parallel
- May be combined for increased capacity

Multi-Gbit Transceivers



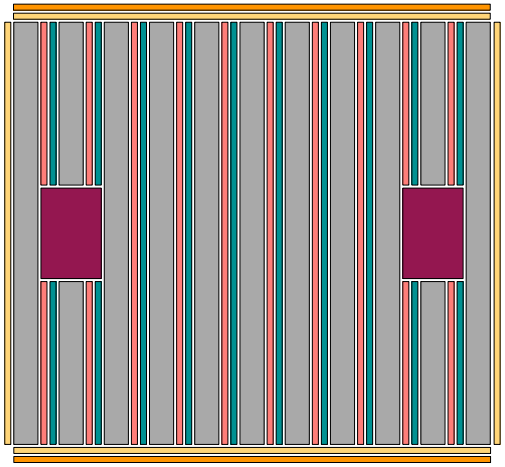
- High-speed serial links : 622 Mbps up to 3.125 Gbps
- Implement Physical Media Attachment and Physical Coding sublayers
- Perform 8b/10b encoding and decoding
- Clock and data recovered from received data stream
- Usable in low latency mode when clocks are matched at Tx and Rx

User Logic (FPGA Fabric)



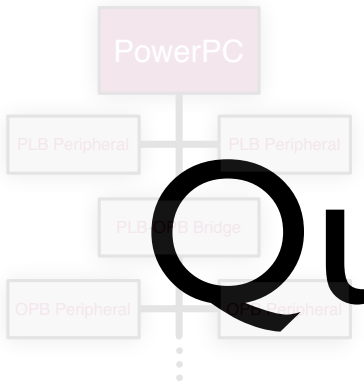
- Fine-grained array of reconfigurable logic based on 4-input LUTs
- Distributed throughout device
- Interspersed with discrete flip-flops for efficient implementation of registered logic
- Implements general purpose user functionality (e.g. WARP OFDM transceivers)
- Glues together and enhances dedicated cores within the FPGA

XC2VP70 Resources



- 2 PowerPC processors
- 328 multipliers
- 328 block RAMs
- 964 general purpose I/Os
- 16 MGTs (8 on WARP FPGA board)
- 66176 4-input LUTs
- 66176 flip-flops (plus I/O registers)

Questions?

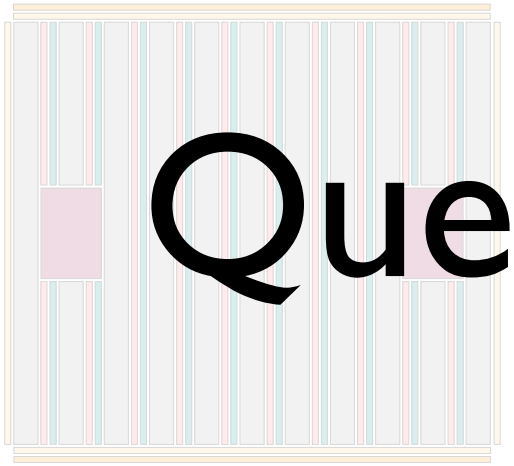

PowerPC
PLB Peripheral
PLB Peripheral
OPB Peripheral

A
B
C
D
Z-1
X

TX
RX

18
X
18
36
Z-1
36

WT_DATA
[17:0]
WT_DATA
[8:0]
A
18
9
B
ADDR
[9:0]
10
18 Kbit BRAM
11
ADDR
[10:0]
18
9
RD_DATA
[17:0]
RD_DATA
[8:0]



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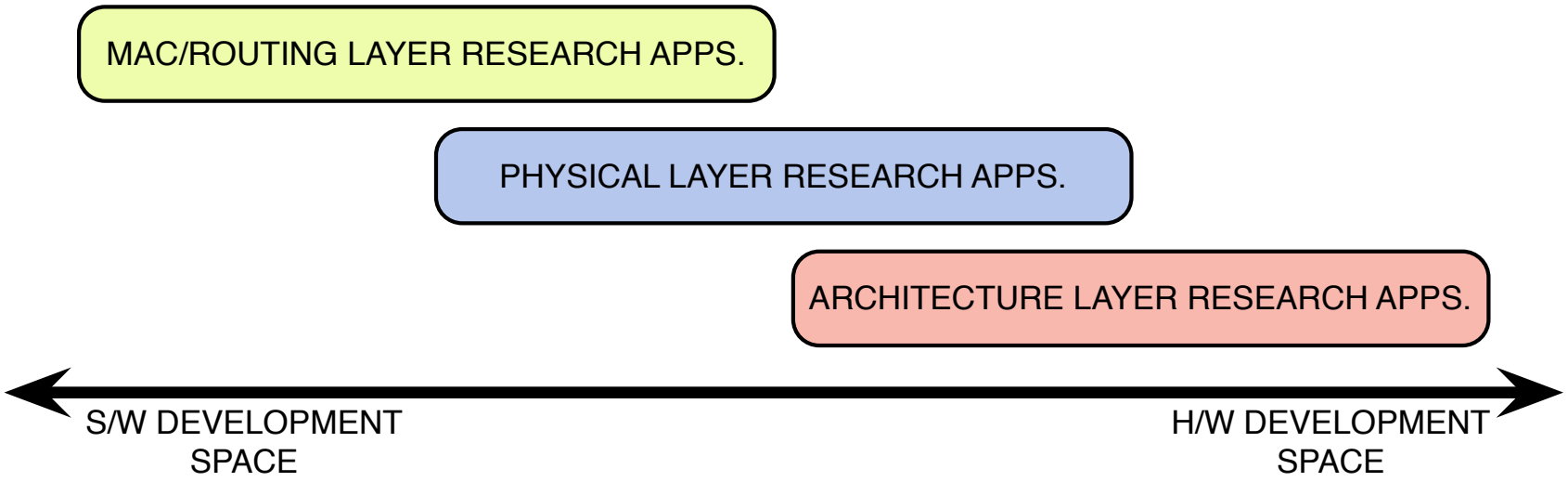
(Classifying Applications by Development Space)

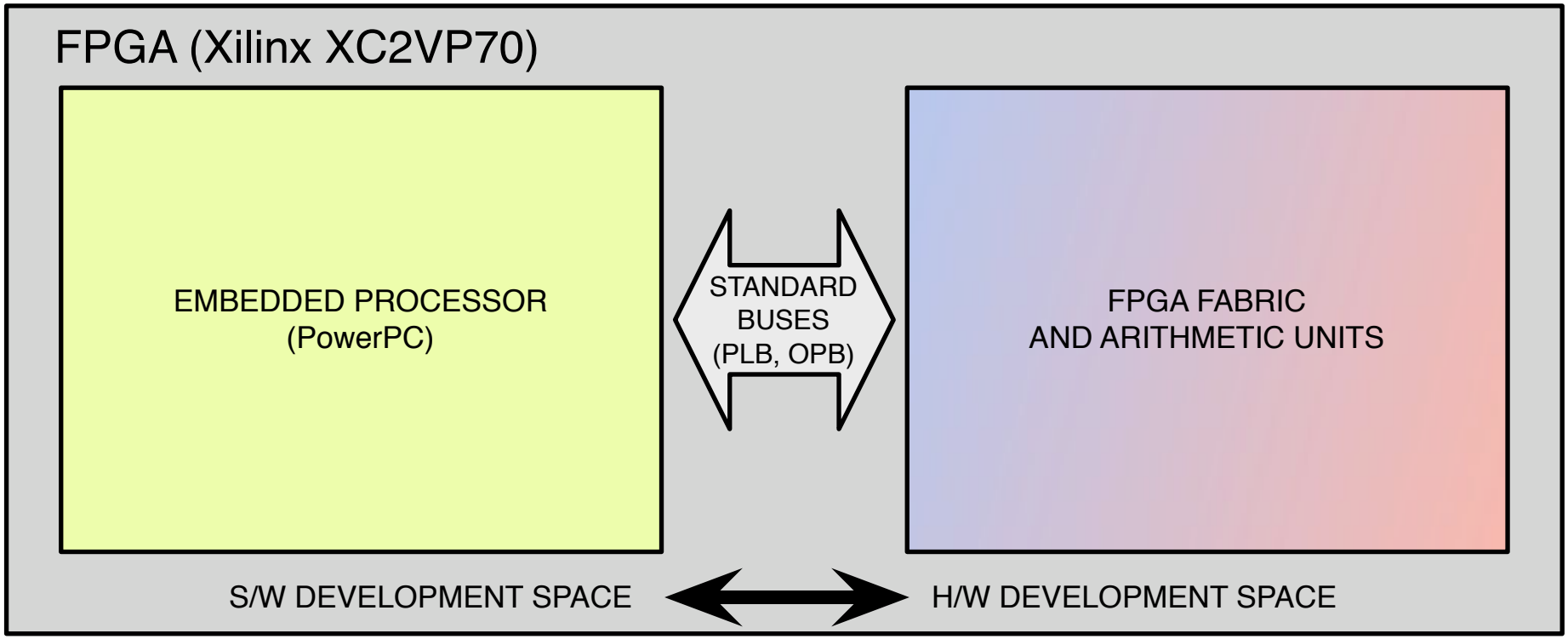


Targeting WARP Hardware

- Hardware Development Efforts
  - Hand-Coding Hardware Designs (Verilog, VHDL)
  - Generating Hardware Designs (System Generator)
  - Interfacing with Existing Hardware IP
- Software Development Efforts
  - Low-Level Driver Development
  - High-Level Application Development
  - Interfacing with Existing Software

Targeting WARP Hardware

(Classifying FPGA Resources by Development Space)



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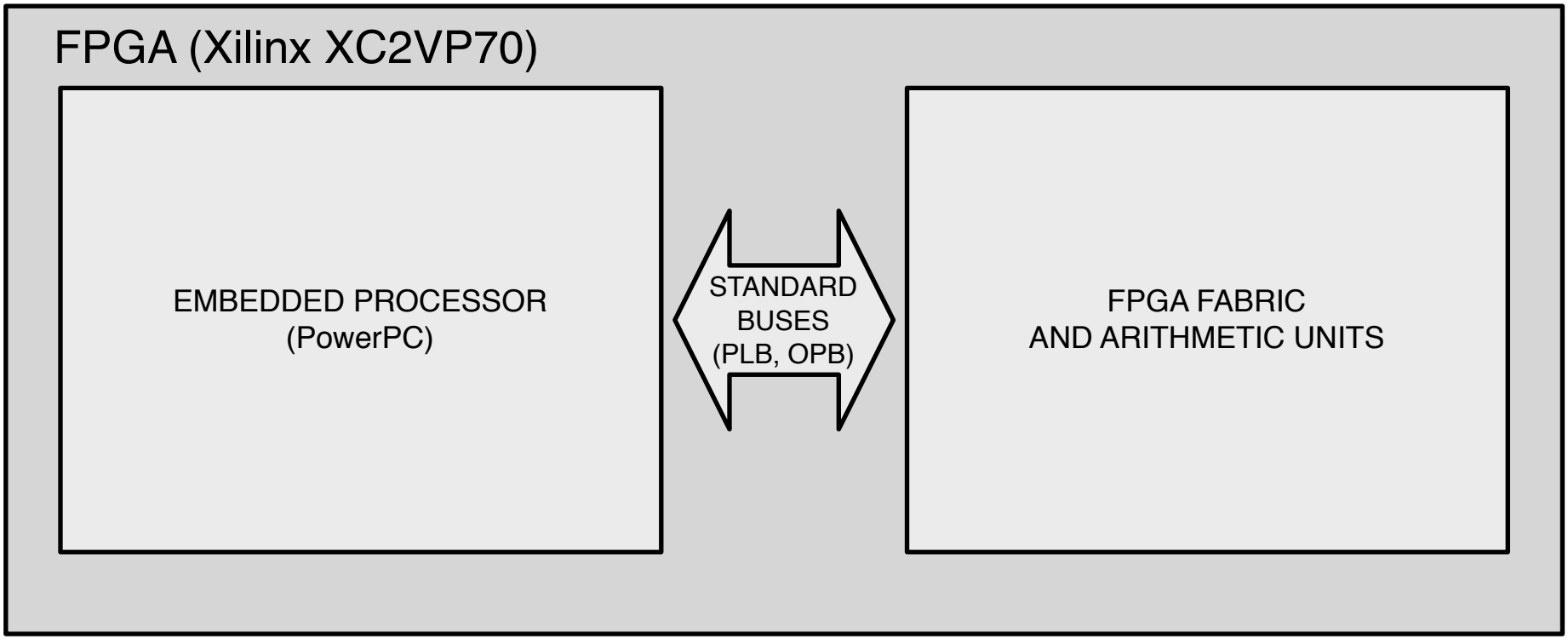
(Understanding the Development Environment)



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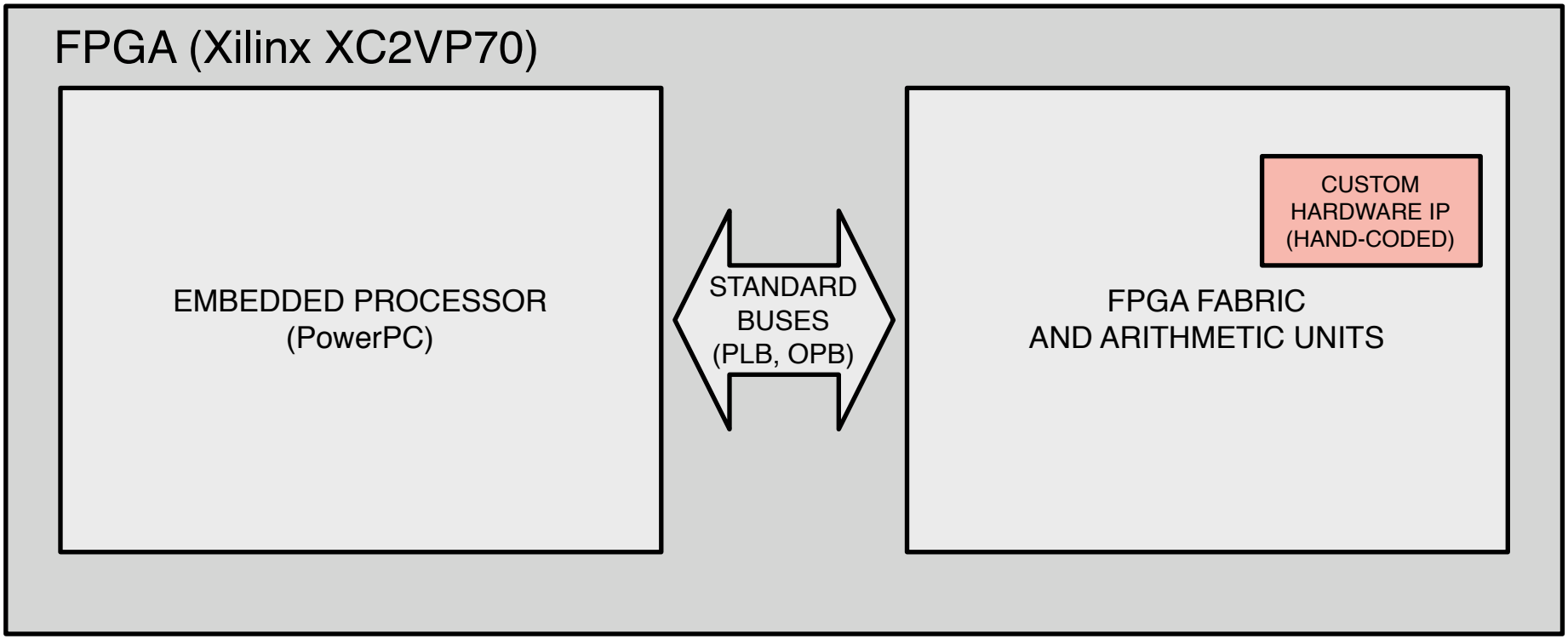

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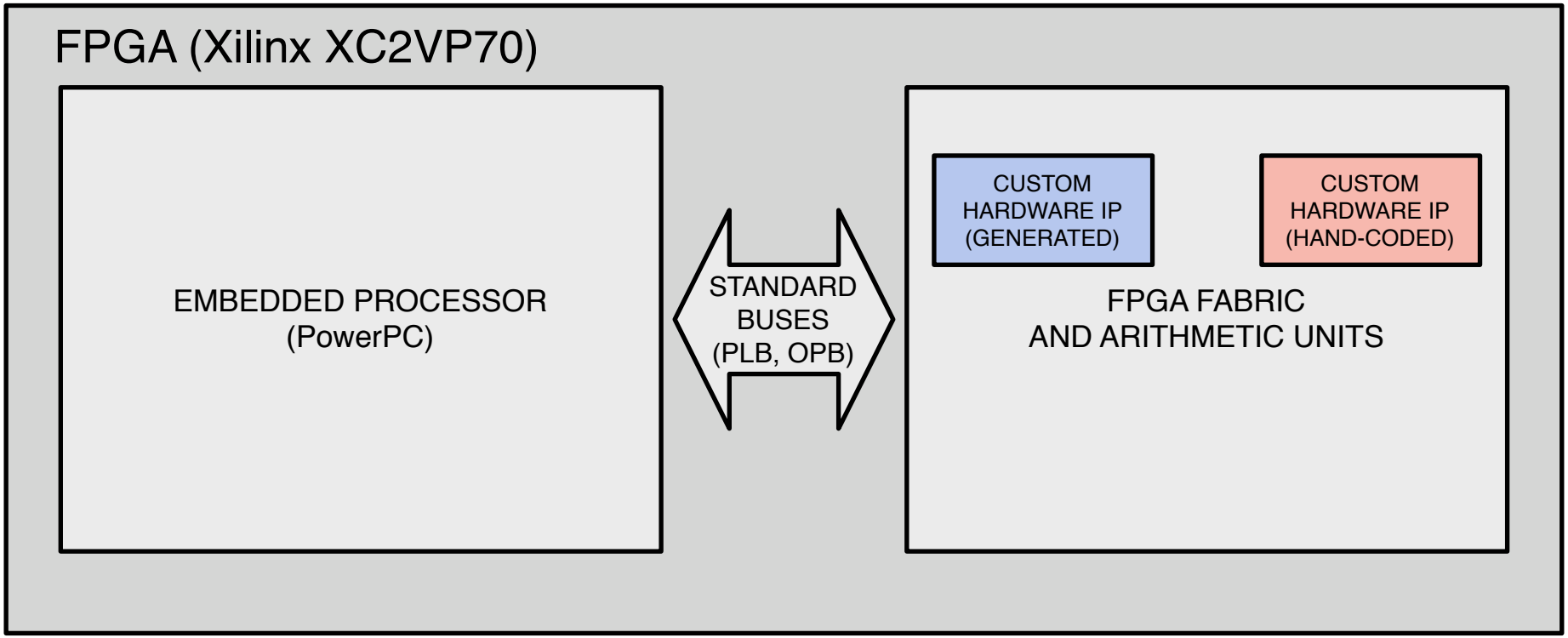
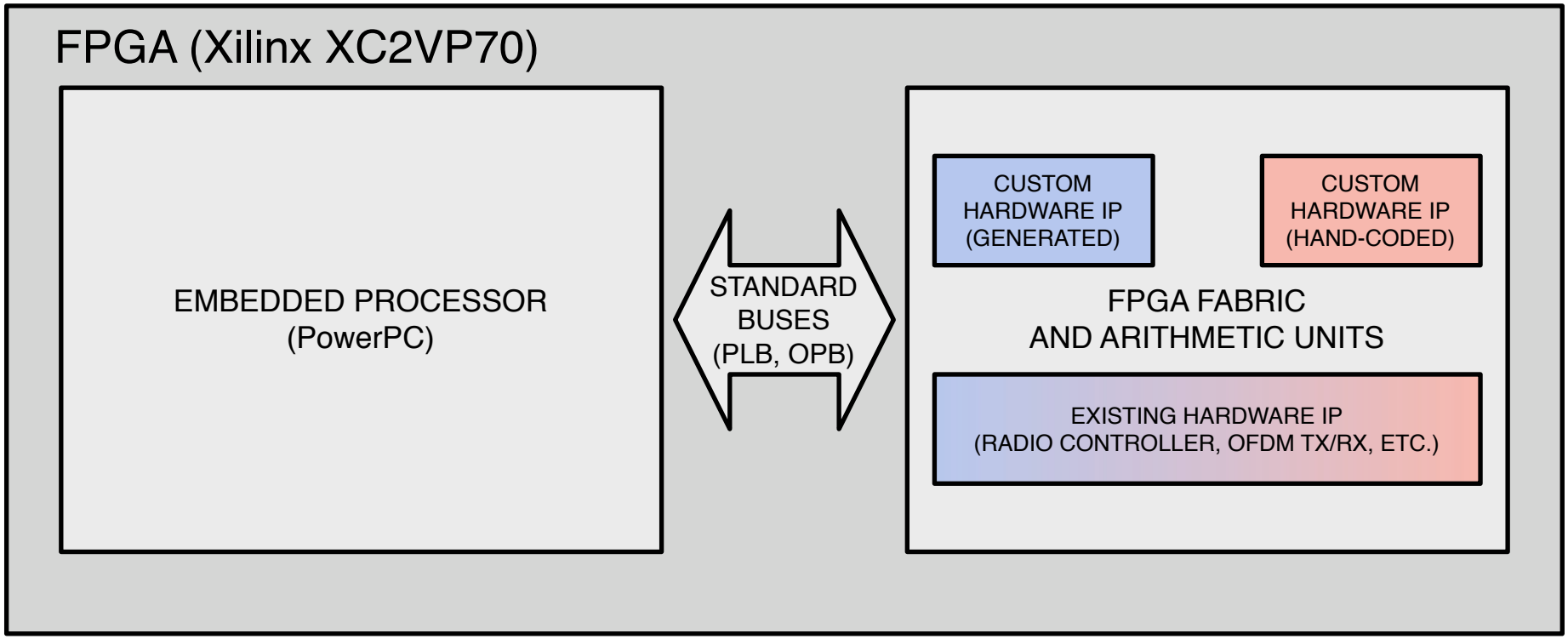


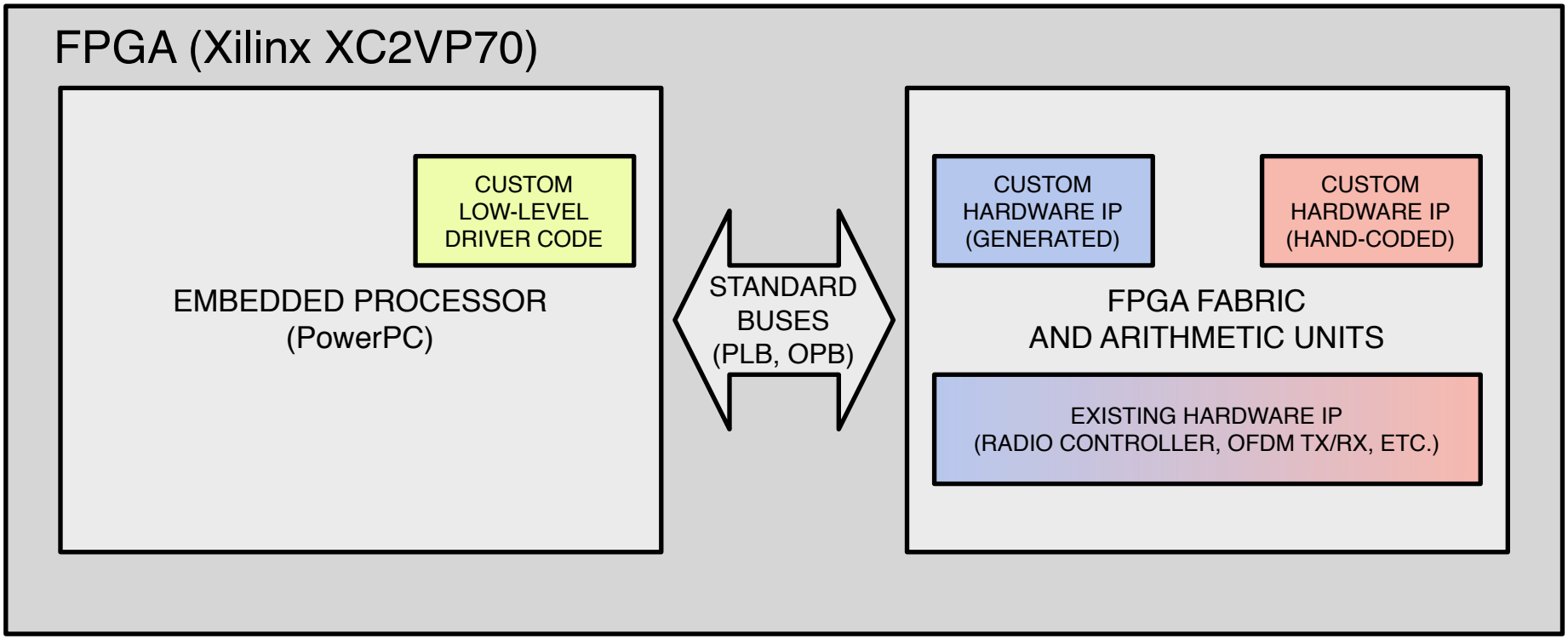
Targeting WARP Hardware

(Understanding the Development Environment)



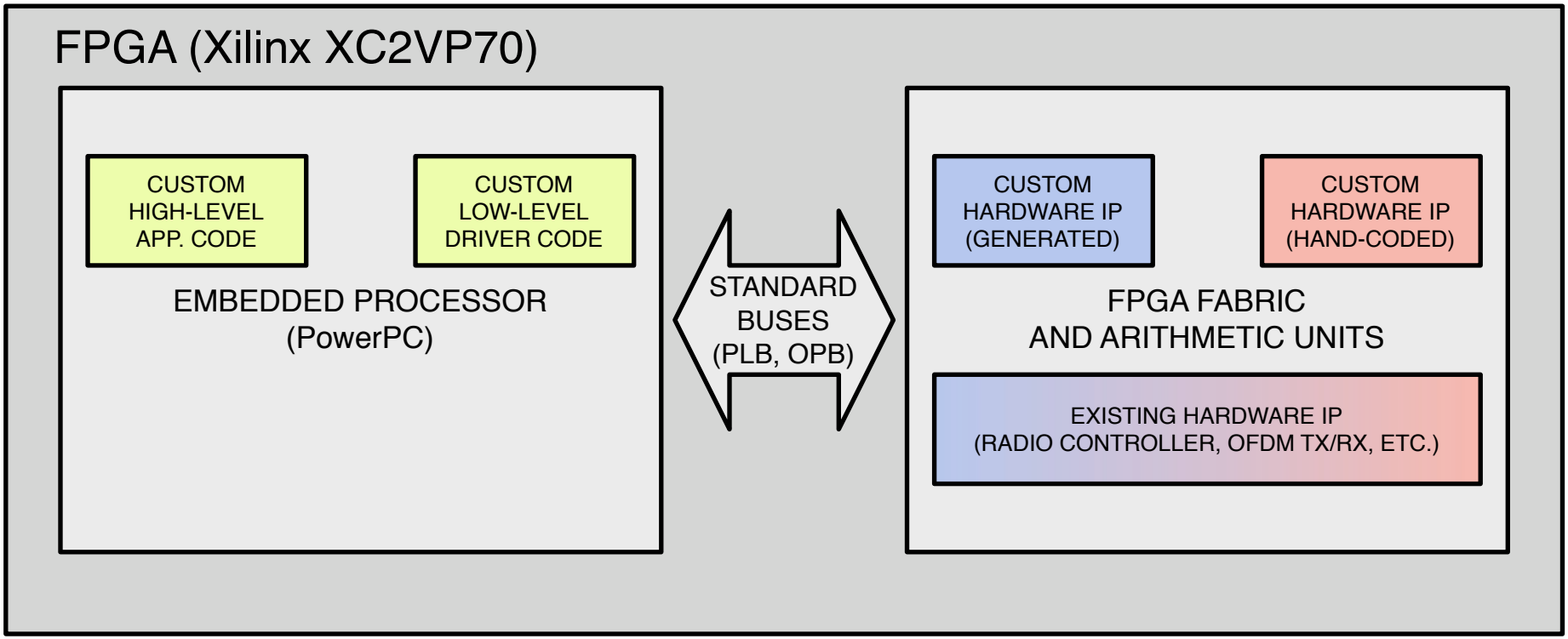
Targeting WARP Hardware

(Understanding the Development Environment)



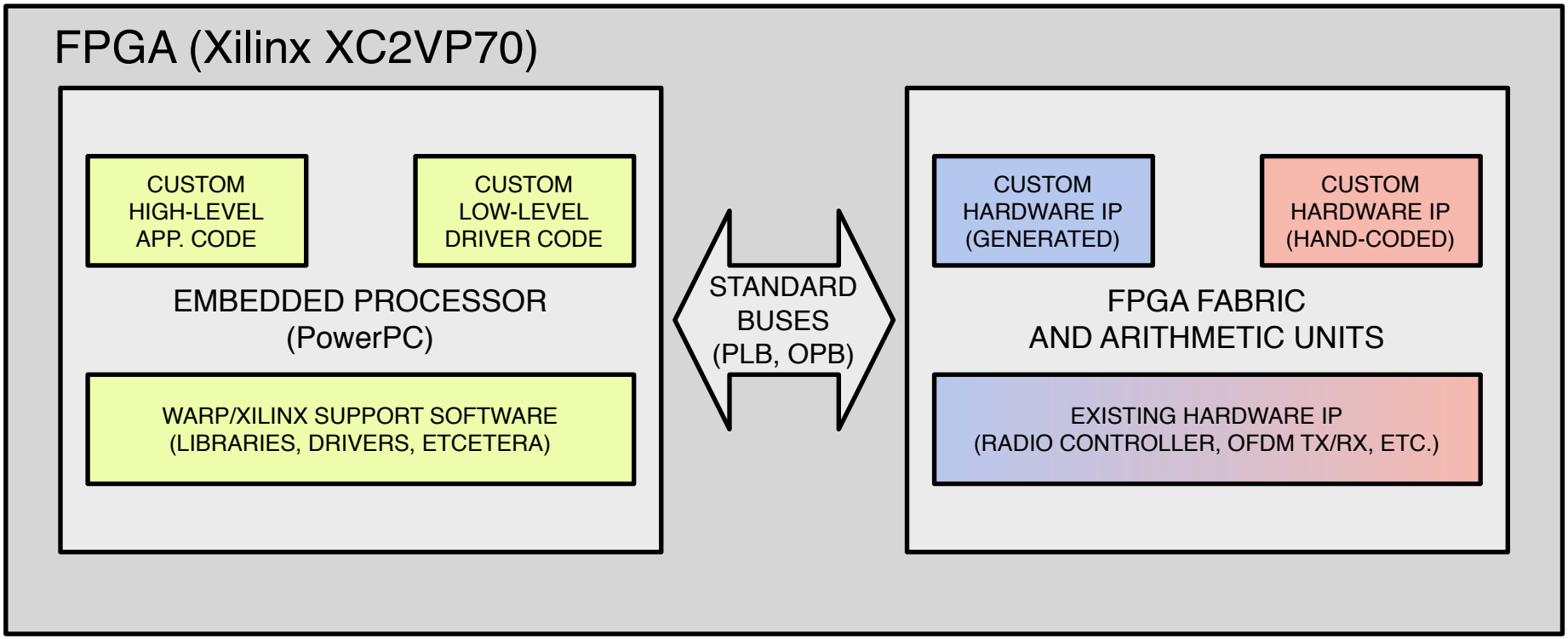
Targeting WARP Hardware

(Understanding the Development Environment)



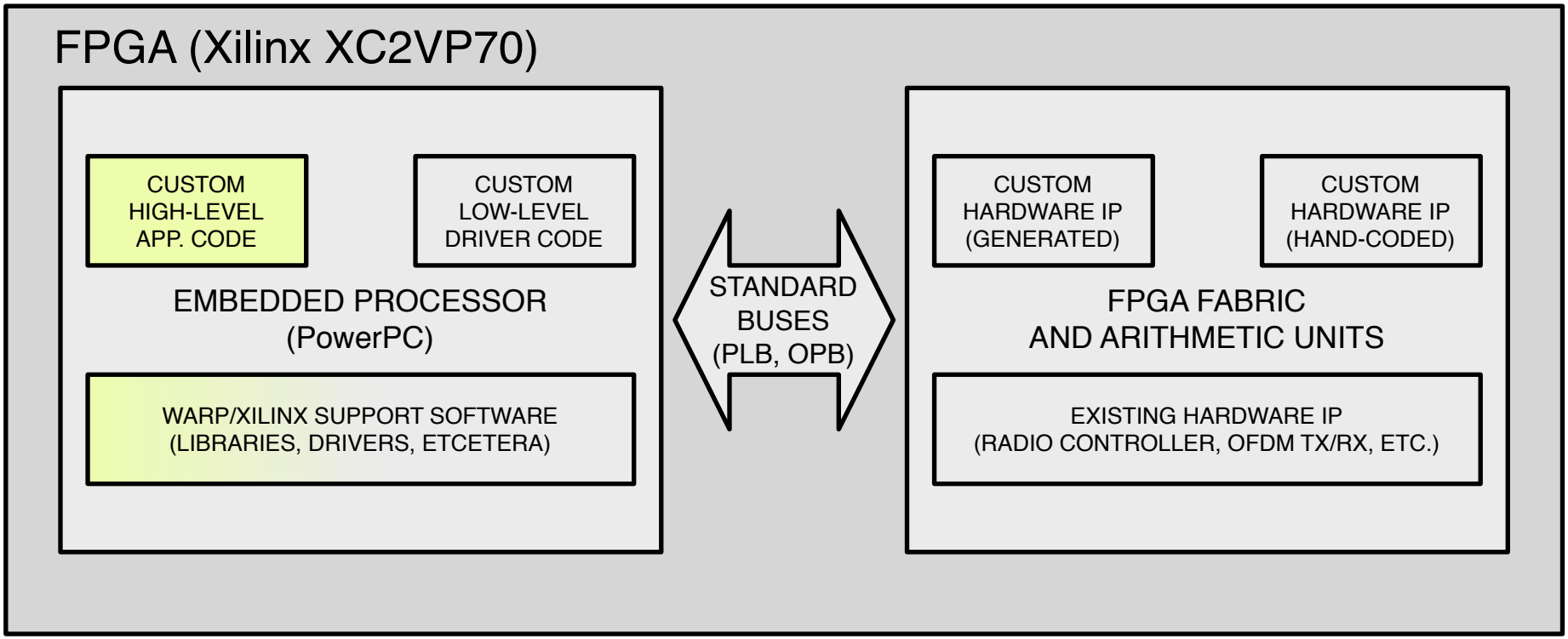
Targeting WARP Hardware

(Understanding the Development Environment)



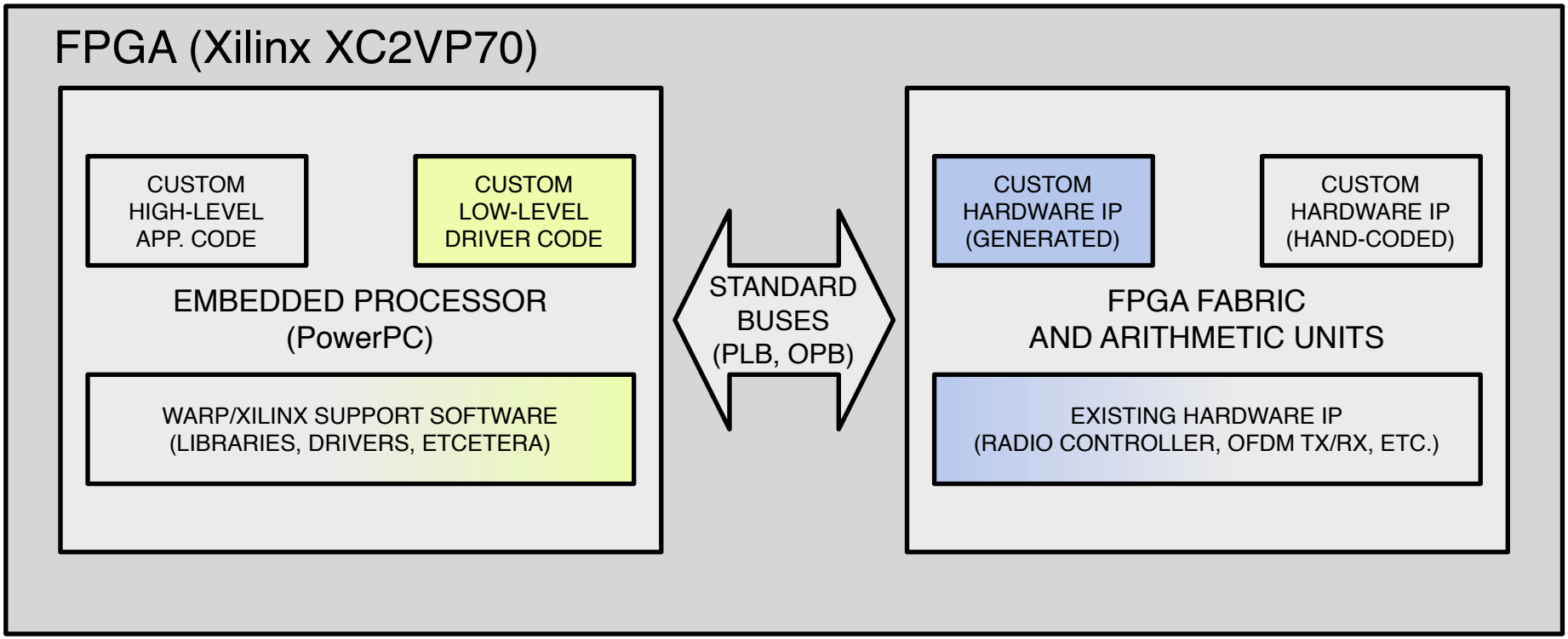
Targeting WARP Hardware

(MAC/Routing Layer Development Space)



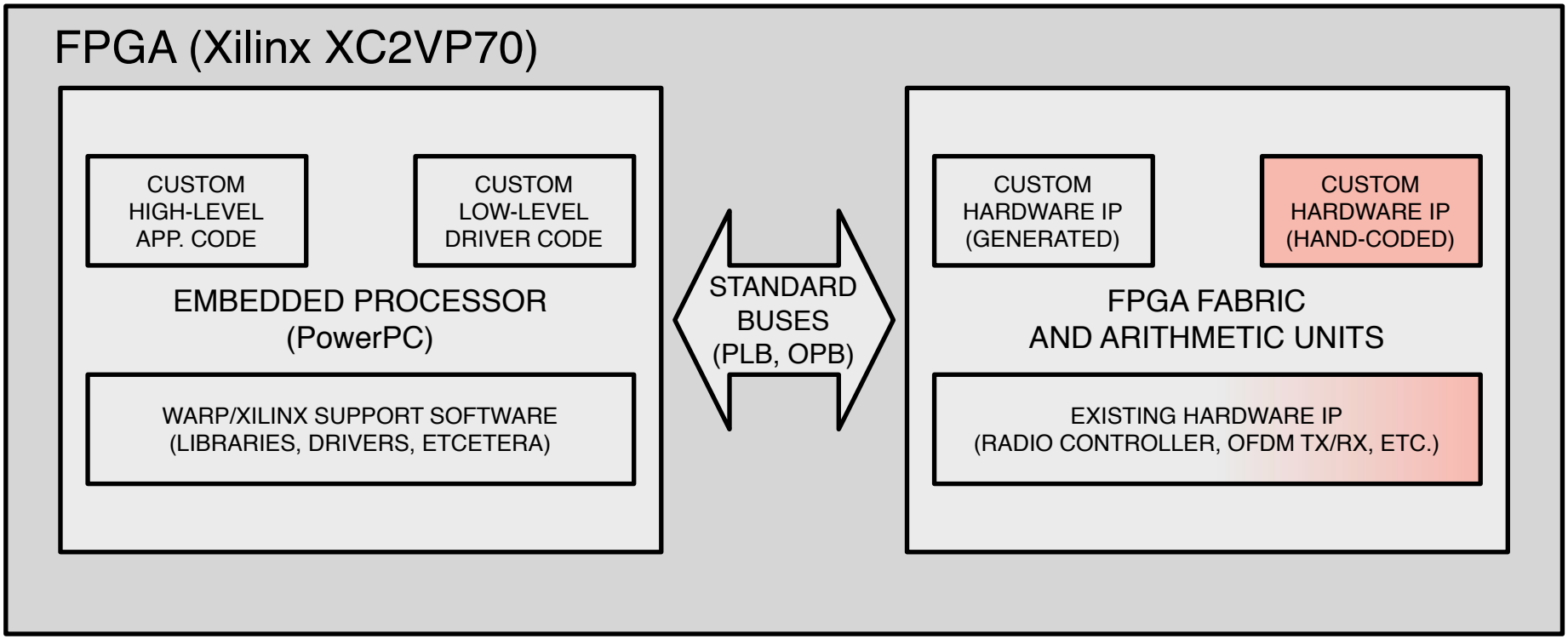
Targeting WARP Hardware

(Physical Layer Development Space)

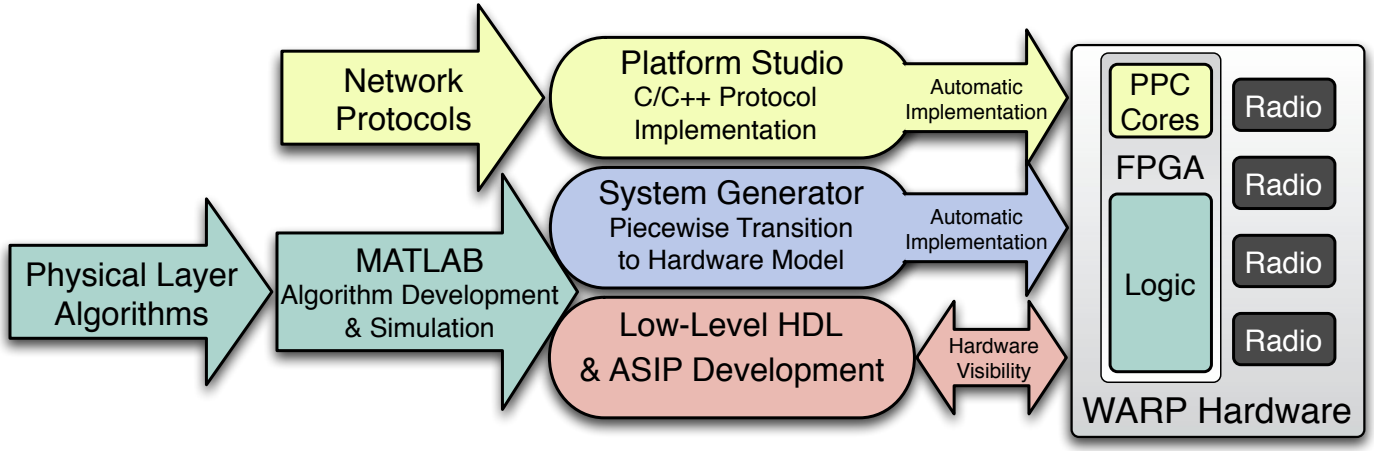


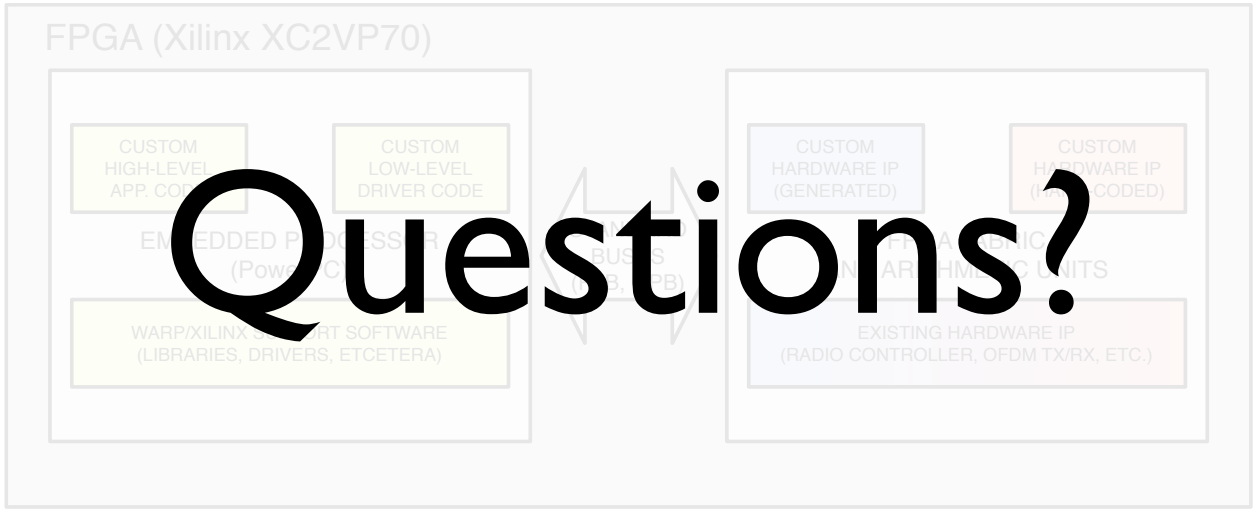
Targeting WARP Hardware

(Architecture Layer Development Space)



Targeting WARP Hardware
(Introducing Development Tools)




FPGA (Xilinx XC2VP70)
CUSTOM
HIGH-LEVEL
APP. CO
CUSTOM
LOW-LEVEL
DRIVER CODE
WARP/XILINX
(LIBRARIES, DRIVERS, ETCETERA)
CUSTOM
HARDWARE IP
(GENERATED)
CUSTOM
HARDWARE IP
(HAND-CODED)
EXISTING HARDWARE IP
(RADIO CONTROLLER, OFDM TX/RX, ETC.)

Questions?