Mango Communications
WARP v3 MMCX Clock Module
Rev 1.0

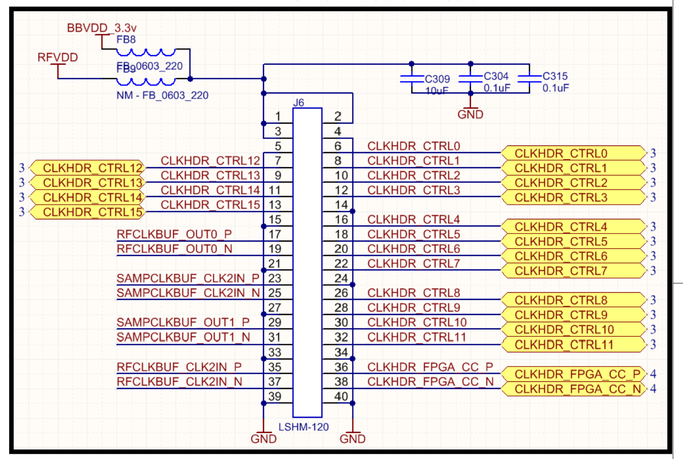
Clock module interface uses same connector on main board and clock module. When mated main board pin N connects to clock module pin (N+1) for odd N.

The clock module uses the same footprint as the WARP v3 main board. As a result, the connector symbols in the two schematics are mirror images.

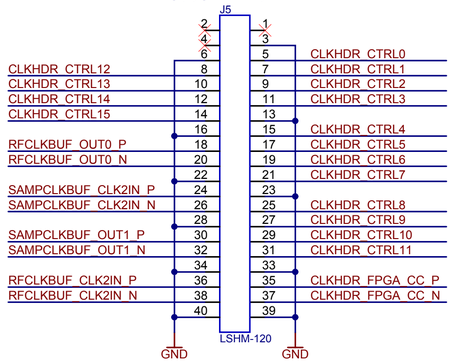
Pin mapping:

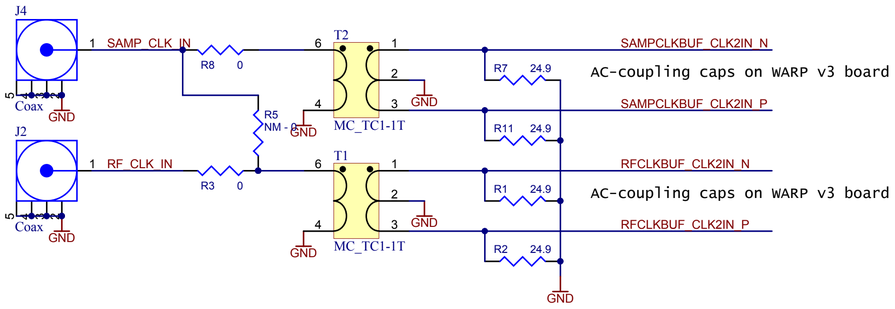
MB	CM
1	2
2	1
3	4
4	3
...	
39	40
40	39

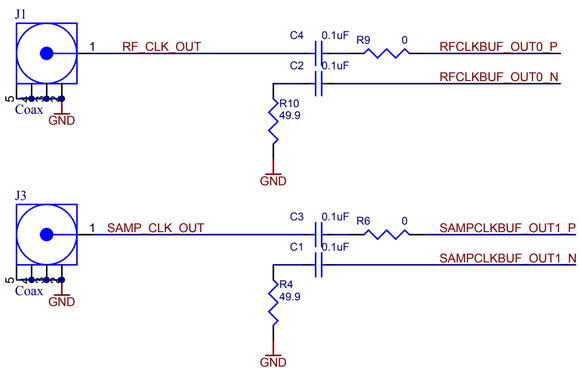
WARP v3 Main Board Circuit

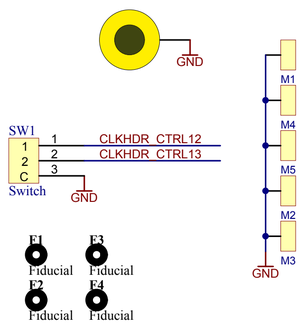


Pins [1,2,4] are VDD; unused on this board









RFCLKBUF_OUT0: Output from main board RF reference clock buffer
(AD9512 port OUT0; requires far-end LVPECL termination on clock module)

SAMPCLKBUF_CLK2IN: Input to main board sampling clock buffer
(AD9512 port CLK2; AC-coupled on main board)

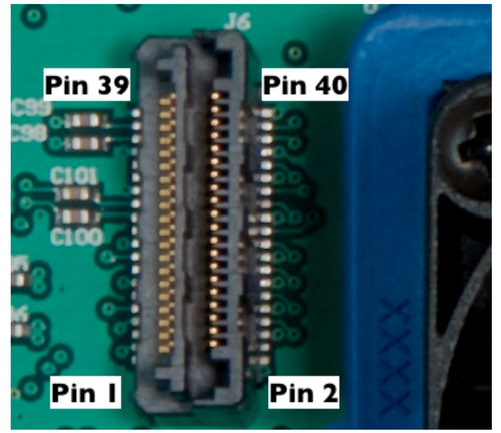
SAMPCLKBUF_OUT1: Output from main board sampling clock buffer
(AD9512 port OUT1; requires far-end LVPECL termination on clock module)

RFCLKBUF_CLK2IN: Input to main board RF reference clock buffer
(AD9512 port CLK2; AC-coupled on main board)

CLKHDR_FPGA_CC: Connected to column 2 SRCC LVDS I/O on FPGA

CLKHDR_CTRL[15:0]: Connected to general 2.5v I/O on FPGA

WARP v3 Main Board Pin Numbers



MB Dimensions:

	X	Y
J6.P1	2401.012mil	2020.91mil
J6.P2	2546.681mil	2020.91mil
J6.P39	2401.012mil	2394.926mil
J6.P40	2546.681mil	2394.926mil
MH3	1037.889mil	2207.819mil

=> J6 center: 2473.8 2207.9

MH to X of nearer pin column:
(2401.012 - 1037.889) = 1363.12

Design:	MMCX Clock Module
Revision:	1.0
Description:	Description
Date:	1/25/2013
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