Mango Communications WARP v3
Rev 1.1

Design:	WARP v3
Revision:	v1.1
Description:	Table of Contents
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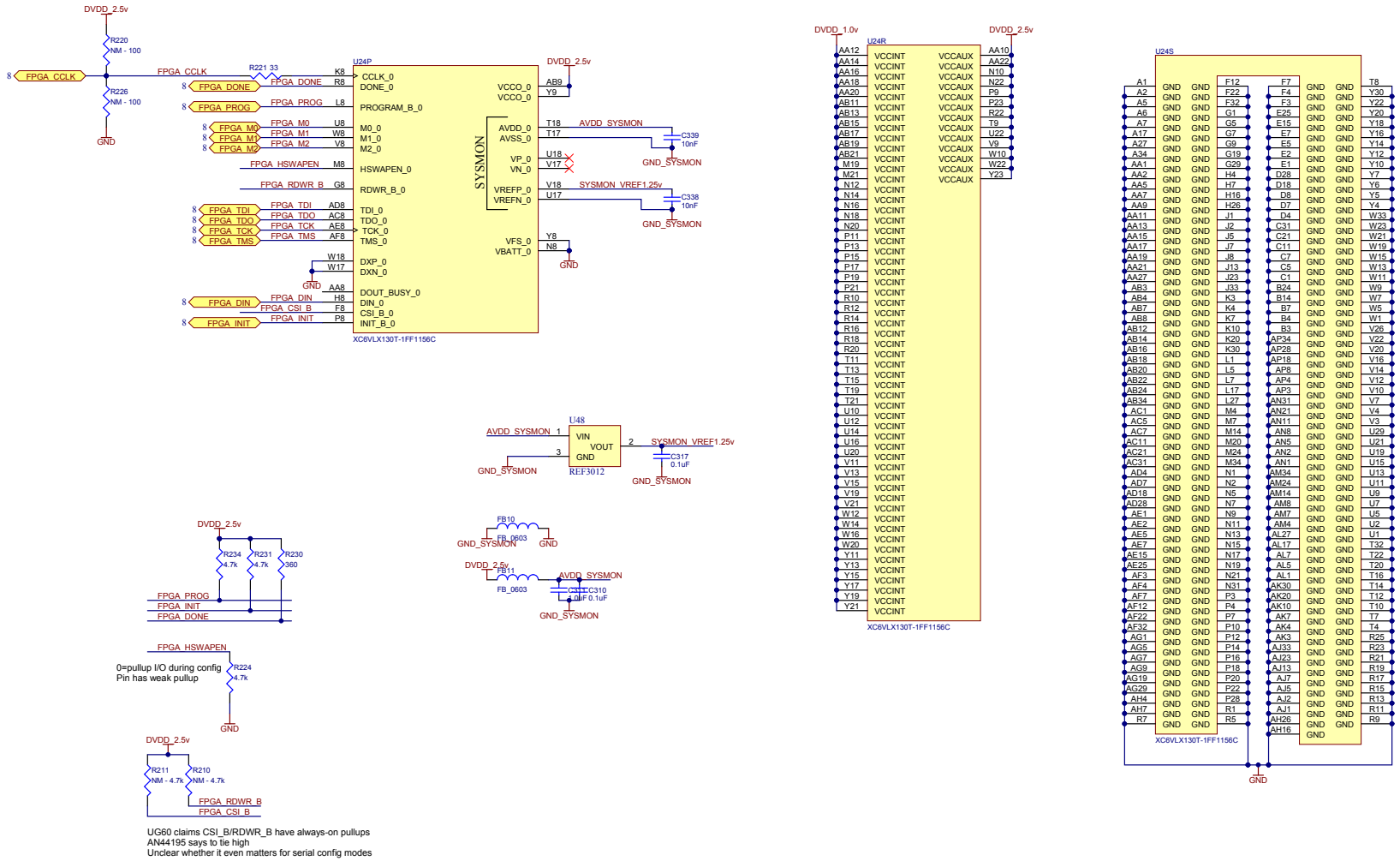

Design:	WARP v3
Revision:	v1.1
Description:	FPGA Power & Config
Date:	1/25/2013
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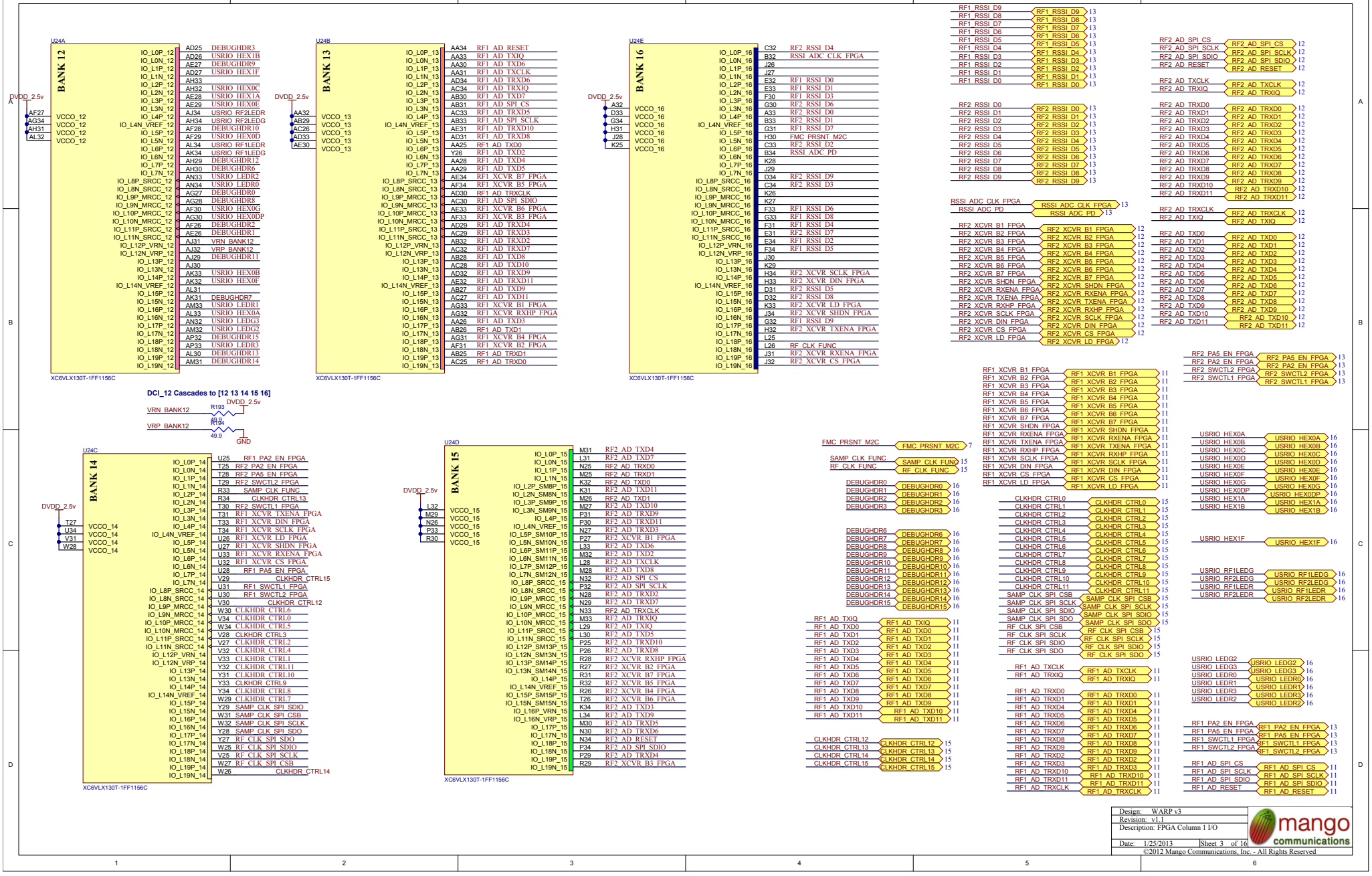
U24A
BANK 12
XC6VLX130T-1FF1156C
U24B
BANK 13
XC6VLX130T-1FF1156C
U24E
BANK 16
XC6VLX130T-1FF1156C
DVDD_2.5v
DCI_12 Cascades to [12 13 14 15 16]
VRN_BANK12
VRP_BANK12
R193
R194
49.9
GND
U24C
BANK 14
XC6VLX130T-1FF1156C
U24D
BANK 15
XC6VLX130T-1FF1156C
DEBUGHDR0
DEBUGHDR1
DEBUGHDR2
DEBUGHDR3
CLKHDR_CTRL0
CLKHDR_CTRL1
CLKHDR_CTRL2
CLKHDR_CTRL3
CLKHDR_CTRL4
CLKHDR_CTRL5
CLKHDR_CTRL6
CLKHDR_CTRL7
CLKHDR_CTRL8
CLKHDR_CTRL9
CLKHDR_CTRL10
CLKHDR_CTRL11
SAMP_CLK_SPI_CSB
SAMP_CLK_SPI_SCLK
SAMP_CLK_SPI_SDIO
SAMP_CLK_SPI_SDO
RF_CLK_SPI_CSB
RF_CLK_SPI_SCLK
RF_CLK_SPI_SDIO
RF_CLK_SPI_SDO
RF1_AD_TXCLK
RF1_AD_TRXIQ
RF1_AD_TRXCLK
RF2_AD_SPI_CS
RF2_AD_SPI_SCLK
RF2_AD_SPI_SDIO
RF2_AD_RESET
RF1_AD_SPI_CS
RF1_AD_SPI_SCLK
RF1_AD_SPI_SDIO
RF1_AD_RESET
Design: WARP v3
Revision: v1.1
Description: FPGA Column 1 I/O
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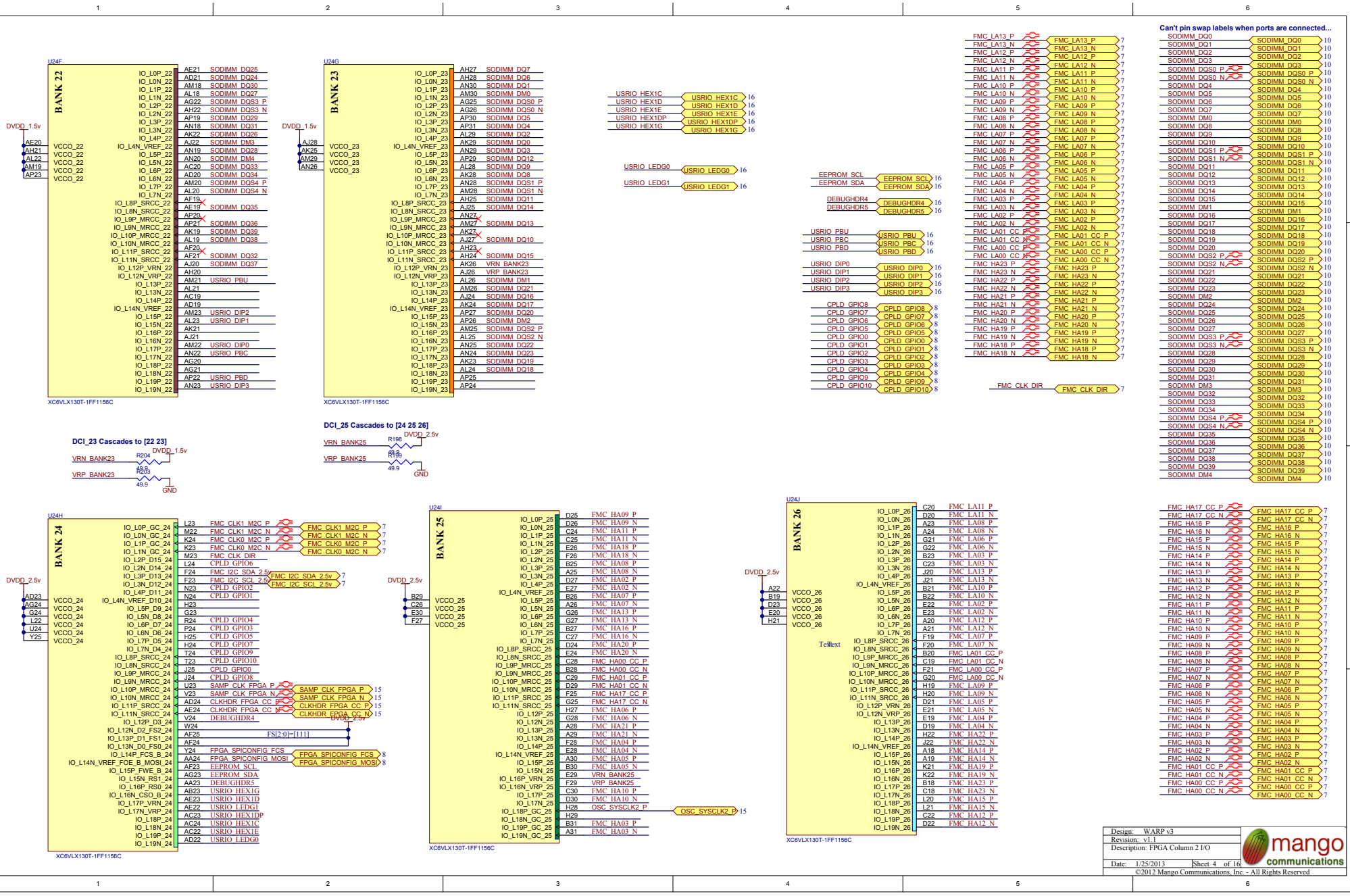
U24F
BANK 22
XC6VLX130T-1FF1156C
U24G
BANK 23
XC6VLX130T-1FF1156C
DVDD_1.5v
USRIO_HEX1C
USRIO_HEX1D
USRIO_HEX1E
USRIO_HEX1DP
USRIO_HEX1G
USRIO_LEDG0
USRIO_LEDG1
EEPROM_SCL
EEPROM_SDA
DEBUGHDR4
DEBUGHDR5
USRIO_PBU
USRIO_PBC
USRIO_PBD
USRIO_DIP0
USRIO_DIP1
USRIO_DIP2
USRIO_DIP3
CPLD_GPIO8
CPLD_GPIO7
CPLD_GPIO6
CPLD_GPIO5
CPLD_GPIO0
CPLD_GPIO1
CPLD_GPIO2
CPLD_GPIO3
CPLD_GPIO4
CPLD_GPIO9
CPLD_GPIO10
FMC_CLK_DIR
Can't pin swap labels when ports are connected...
DCI_23 Cascades to [22 23]
VRN_BANK23
VRP_BANK23
R204
R203
49.9
DCI_25 Cascades to [24 25 26]
VRN_BANK25
VRP_BANK25
R198
R199
DVDD_2.5v
GND
U24H
BANK 24
XC6VLX130T-1FF1156C
U24I
BANK 25
XC6VLX130T-1FF1156C
U24J
BANK 26
XC6VLX130T-1FF1156C
FMC_CLK1_M2C_P
FMC_CLK1_M2C_N
FMC_CLK0_M2C_P
FMC_CLK0_M2C_N
FMC_I2C_SDA_2.5v
FMC_I2C_SCL_2.5v
SAMP_CLK_FPGA_P
SAMP_CLK_FPGA_N
CLKHDR_FPGA_CC_P
CLKHDR_FPGA_CC_N
FS[2:0]=[111]
FPGA_SPICONFIG_FCS
FPGA_SPICONFIG_MOSI
OSC_SYSCLK2_P
Design: WARP v3
Revision: v1.1
Description: FPGA Column 2 I/O
Date: 1/25/2013
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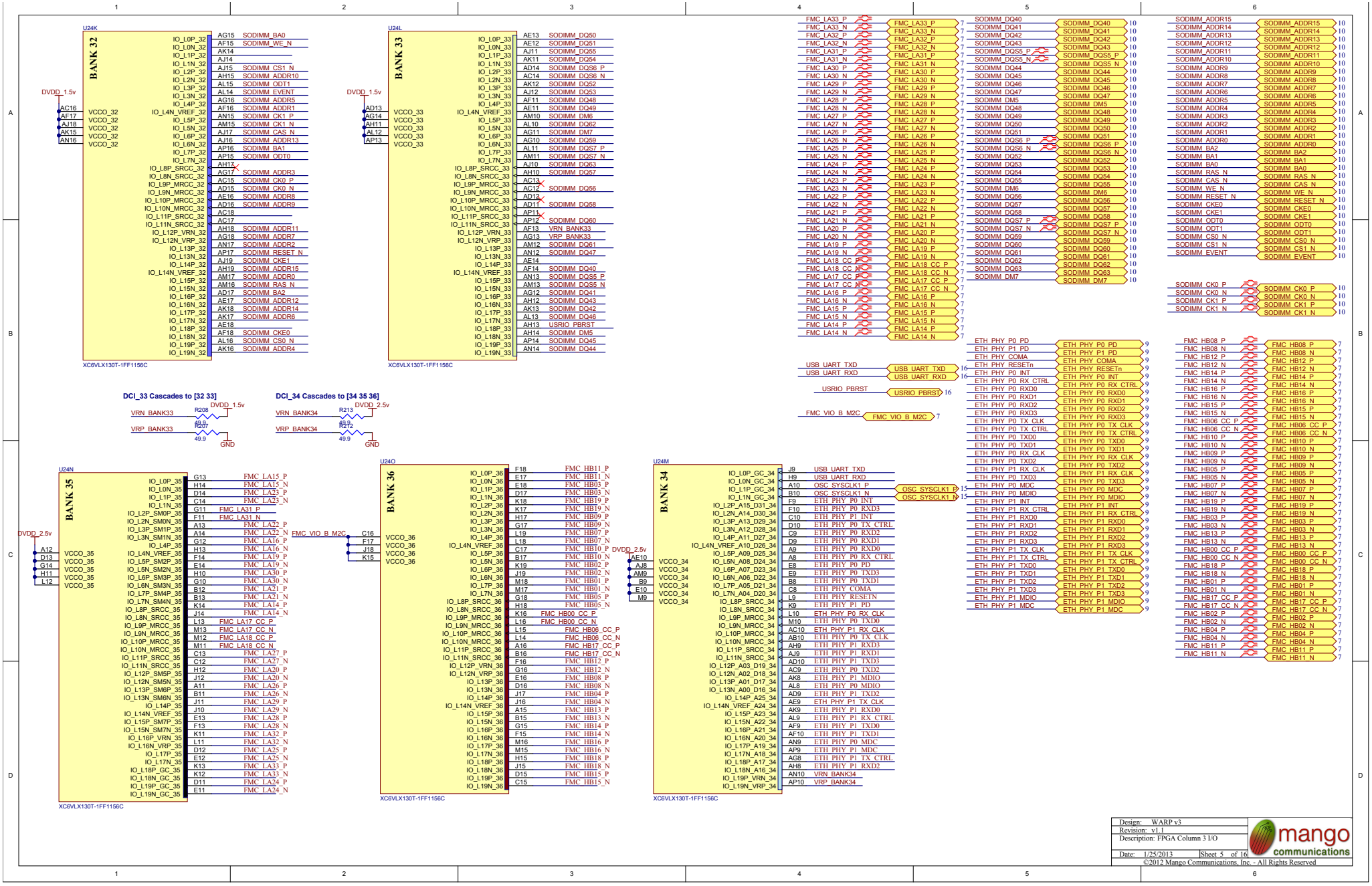
U24K
BANK 32
XC6VLX130T-1FF1156C
U24L
BANK 33
XC6VLX130T-1FF1156C
DCI_33 Cascades to [32 33]
DCI_34 Cascades to [34 35 36]
U24N
BANK 35
XC6VLX130T-1FF1156C
U24O
BANK 36
XC6VLX130T-1FF1156C
U24M
BANK 34
XC6VLX130T-1FF1156C
Design: WARP v3
Revision: v1.1
Description: FPGA Column 3 I/O
Date: 1/25/2013
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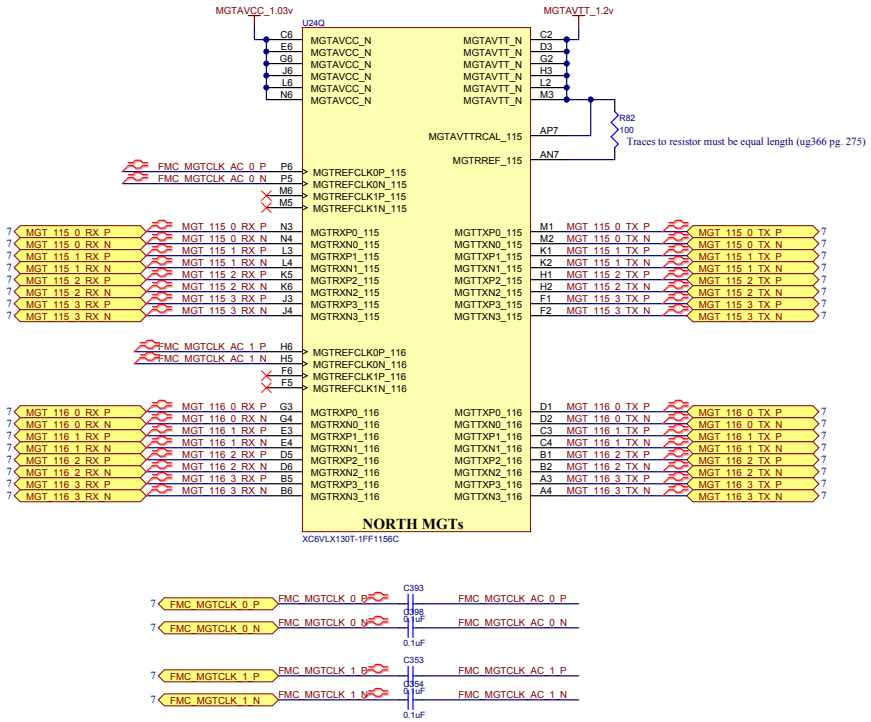

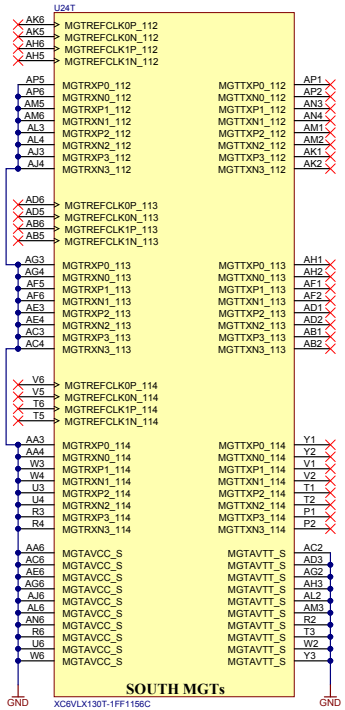

Only 8 MGTs are used, all in the North half of the chip.
South MGTs are unused.

Per UG366, unused MGTs are connected as:
MGTAVCC=GND
MGTAVTT=GND
MGTREFCLKx=Float
MGTRXx=GND
MGTTXx=Float

Design:	WARP v3
Revision:	v1.1
Description:	FPGA Column 4 I/O
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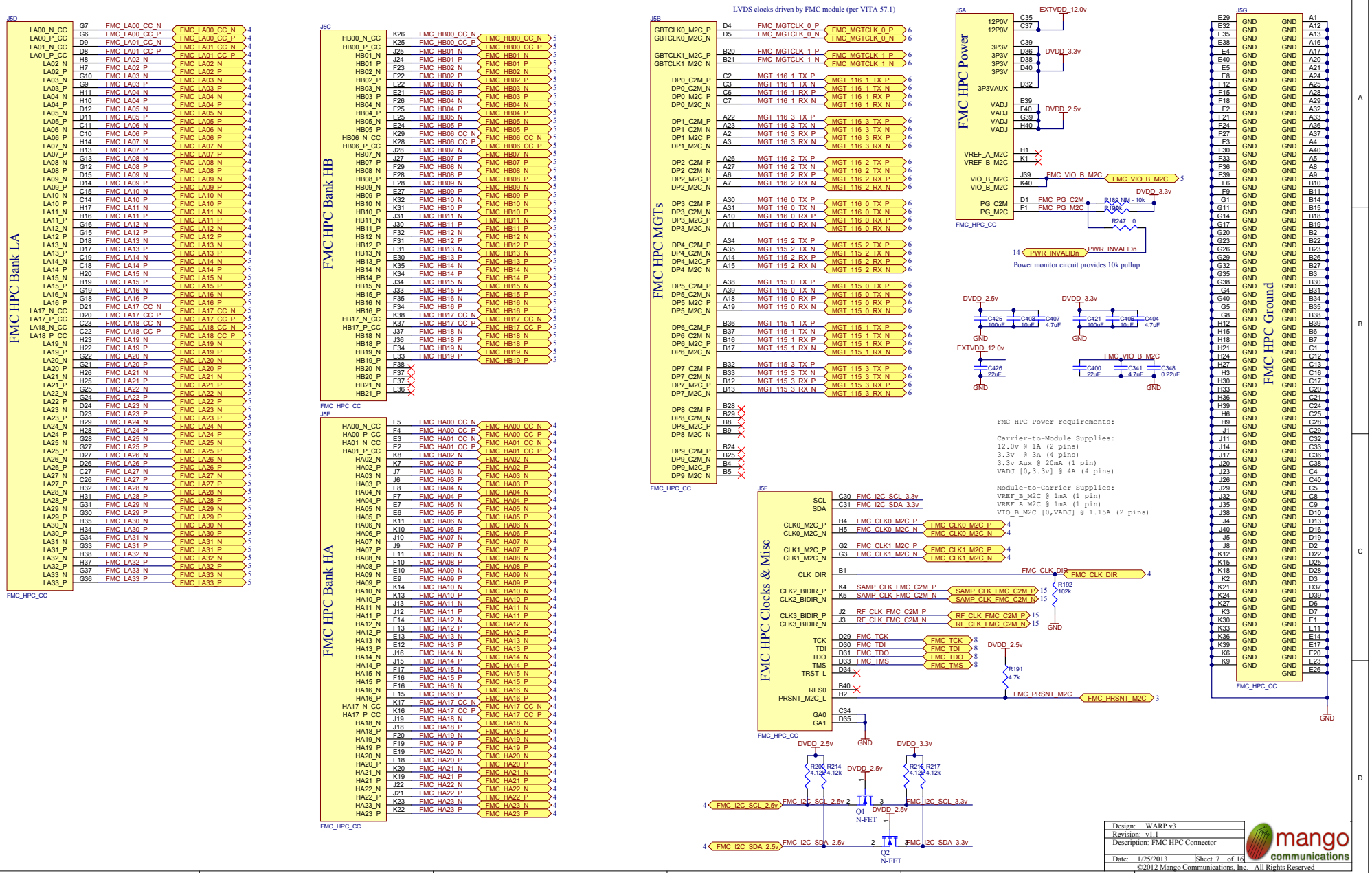
J5D
FMC HPC Bank LA
FMC_HPC_CC
J5C
FMC HPC Bank HB
FMC_HPC_CC
J5E
FMC HPC Bank HA
FMC_HPC_CC
J5B
FMC HPC MGTs
FMC_HPC_CC
LVDS clocks driven by FMC module (per VITA 57.1)
J5A
FMC HPC Power
FMC_HPC_CC
EXTVDD_12.0v
DVDD_3.3v
DVDD_2.5v
DVDD_3.3V
FMC_VIO_B_M2C
PWR_INVALIDn
Power monitor circuit provides 10k pullup
J5G
FMC HPC Ground
FMC_HPC_CC
J5F
FMC HPC Clocks & Misc
FMC_HPC_CC
FMC HPC Power requirements:
Carrier-to-Module Supplies:
12.0v @ 1A (2 pins)
3.3v @ 3A (4 pins)
3.3v Aux @ 20mA (1 pin)
VADJ [0,3.3v] @ 4A (4 pins)
Module-to-Carrier Supplies:
VREF_B_M2C @ 1mA (1 pin)
VREF_A_M2C @ 1mA (1 pin)
VIO_B_M2C [0,VADJ] @ 1.15A (2 pins)
Q1
N-FET
Q2
N-FET
Design: WARP v3
Revision: v1.1
Description: FMC HPC Connector
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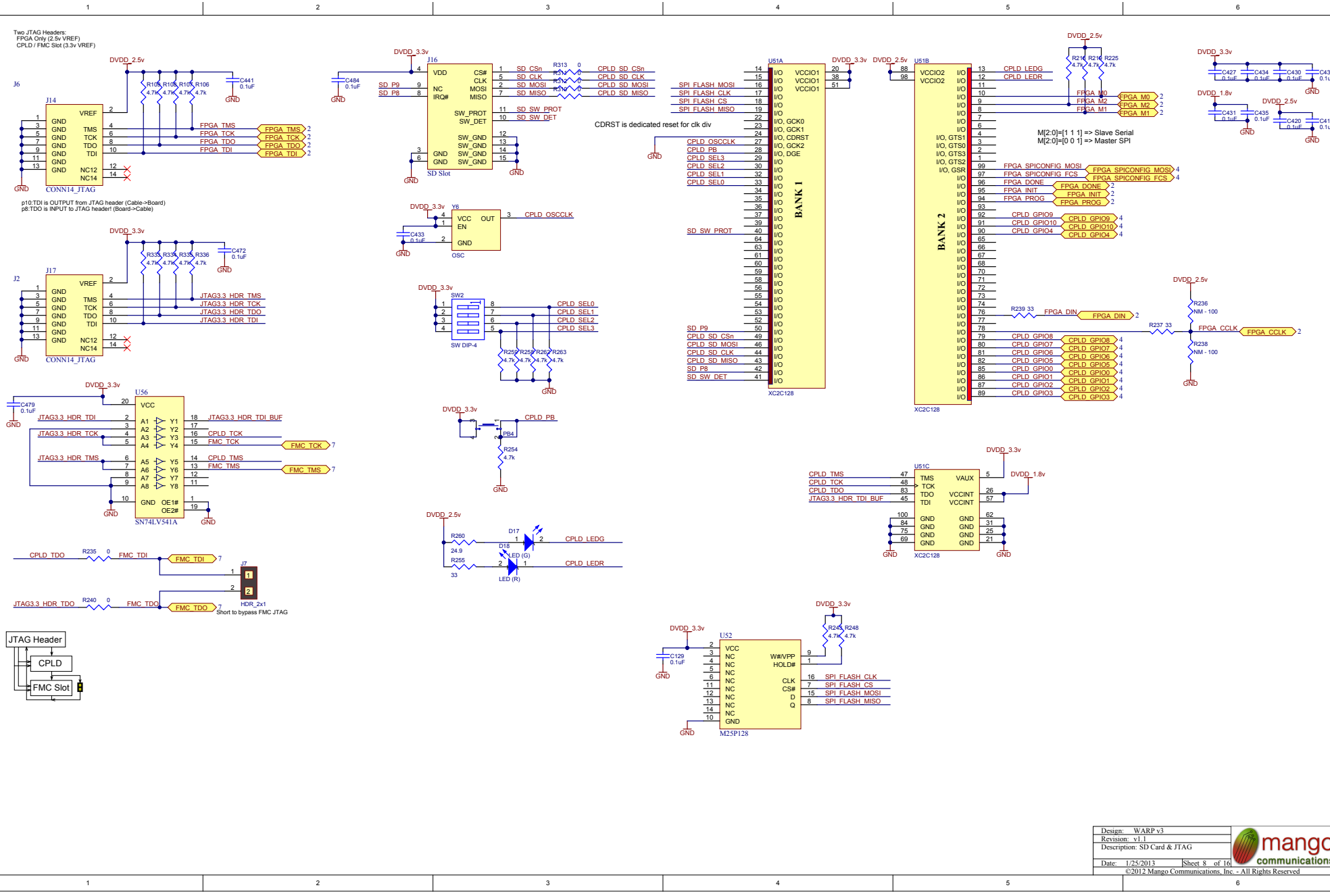
Two JTAG Headers:
FPGA Only (2.5v VREF)
CPLD / FMC Slot (3.3v VREF)
J6
J14
CONN14_JTAG
p10:TDI is OUTPUT from JTAG header (Cable->Board)
p8:TDO is INPUT to JTAG header! (Board->Cable)
J2
J17
CONN14_JTAG
U56
SN74LV541A
J7
HDR_2x1
Short to bypass FMC JTAG
JTAG Header
CPLD
FMC Slot
J16
SD Slot
Y6
OSC
SW2
SW DIP-4
D17
D18
LED (G)
LED (R)
U51A
BANK 1
XC2C128
U51B
BANK 2
XC2C128
U51C
XC2C128
U52
M25P128
CDRST is dedicated reset for clk div
M[2:0]=[1 1 1] => Slave Serial
M[2:0]=[0 0 1] => Master SPI
Design: WARP v3
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Description: SD Card & JTAG
Date: 1/25/2013
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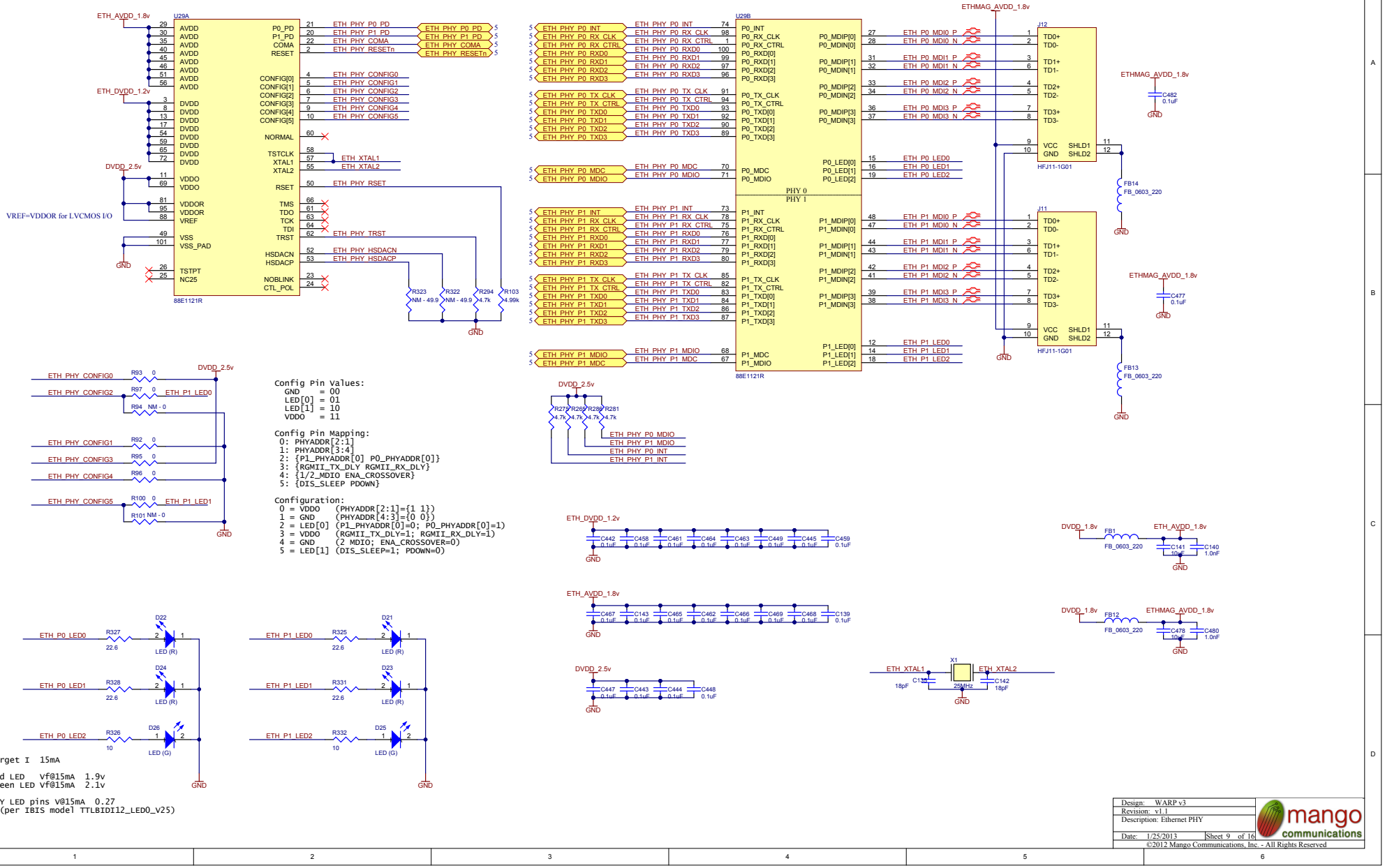
ETH_AVDD_1.8v
U29A
AVDD
ETH_DVDD_1.2v
DVDD
DVDD_2.5v
VDDO
VREF=VDDOR for LVCMOS I/O
VDDOR
VREF
VSS
VSS_PAD
TSTPT
NC25
88E1121R
P0_PD
P1_PD
COMA
RESET
CONFIG[0]
CONFIG[1]
CONFIG[2]
CONFIG[3]
CONFIG[4]
CONFIG[5]
NORMAL
TSTCLK
XTAL1
XTAL2
RSET
TMS
TDO
TCK
TDI
TRST
HSDACN
HSDACP
NOBLINK
CTL_POL
ETH_PHY_P0_PD
ETH_PHY_P1_PD
ETH_PHY_COMA
ETH_PHY_RESETn
ETH_PHY_CONFIG0
ETH_PHY_CONFIG1
ETH_PHY_CONFIG2
ETH_PHY_CONFIG3
ETH_PHY_CONFIG4
ETH_PHY_CONFIG5
ETH_XTAL1
ETH_XTAL2
ETH_PHY_RSET
ETH_PHY_TRST
ETH_PHY_HSDACN
ETH_PHY_HSDACP
R323 NM - 49.9
R322 NM - 49.9
R294 4.7k
R103 4.99k
GND
U29B
PHY 0
PHY 1
P0_INT
P0_RX_CLK
P0_RX_CTRL
P0_RXD[0]
P0_RXD[1]
P0_RXD[2]
P0_RXD[3]
P0_TX_CLK
P0_TX_CTRL
P0_TXD[0]
P0_TXD[1]
P0_TXD[2]
P0_TXD[3]
P0_MDC
P0_MDIO
P1_INT
P1_RX_CLK
P1_RX_CTRL
P1_RXD[0]
P1_RXD[1]
P1_RXD[2]
P1_RXD[3]
P1_TX_CLK
P1_TX_CTRL
P1_TXD[0]
P1_TXD[1]
P1_TXD[2]
P1_TXD[3]
P1_MDC
P1_MDIO
ETH_PHY_P0_INT
ETH_PHY_P0_RX_CLK
ETH_PHY_P0_RX_CTRL
ETH_PHY_P0_RXD0
ETH_PHY_P0_RXD1
ETH_PHY_P0_RXD2
ETH_PHY_P0_RXD3
ETH_PHY_P0_TX_CLK
ETH_PHY_P0_TX_CTRL
ETH_PHY_P0_TXD0
ETH_PHY_P0_TXD1
ETH_PHY_P0_TXD2
ETH_PHY_P0_TXD3
ETH_PHY_P0_MDC
ETH_PHY_P0_MDIO
ETH_PHY_P1_INT
ETH_PHY_P1_RX_CLK
ETH_PHY_P1_RX_CTRL
ETH_PHY_P1_RXD0
ETH_PHY_P1_RXD1
ETH_PHY_P1_RXD2
ETH_PHY_P1_RXD3
ETH_PHY_P1_TX_CLK
ETH_PHY_P1_TX_CTRL
ETH_PHY_P1_TXD0
ETH_PHY_P1_TXD1
ETH_PHY_P1_TXD2
ETH_PHY_P1_TXD3
ETH_PHY_P1_MDIO
ETH_PHY_P1_MDC
P0_MDIP[0]
P0_MDIN[0]
P0_MDIP[1]
P0_MDIN[1]
P0_MDIP[2]
P0_MDIN[2]
P0_MDIP[3]
P0_MDIN[3]
P0_LED[0]
P0_LED[1]
P0_LED[2]
P1_MDIP[0]
P1_MDIN[0]
P1_MDIP[1]
P1_MDIN[1]
P1_MDIP[2]
P1_MDIN[2]
P1_MDIP[3]
P1_MDIN[3]
P1_LED[0]
P1_LED[1]
P1_LED[2]
ETH_P0_MDI0_P
ETH_P0_MDI0_N
ETH_P0_MDI1_P
ETH_P0_MDI1_N
ETH_P0_MDI2_P
ETH_P0_MDI2_N
ETH_P0_MDI3_P
ETH_P0_MDI3_N
ETH_P0_LED0
ETH_P0_LED1
ETH_P0_LED2
ETH_P1_MDI0_P
ETH_P1_MDI0_N
ETH_P1_MDI1_P
ETH_P1_MDI1_N
ETH_P1_MDI2_P
ETH_P1_MDI2_N
ETH_P1_MDI3_P
ETH_P1_MDI3_N
ETH_P1_LED0
ETH_P1_LED1
ETH_P1_LED2
88E1121R
ETHMAG_AVDD_1.8v
J12
J11
TD0+
TD0-
TD1+
TD1-
TD2+
TD2-
TD3+
TD3-
VCC
GND
SHLD1
SHLD2
HFJ11-1G01
C482 0.1uF
C477 0.1uF
FB14 FB_0603_220
FB13 FB_0603_220
R93 0
R97 0
R94 NM - 0
R92 0
R95 0
R96 0
R100 0
R101 NM - 0
ETH_P1_LED0
ETH_P1_LED1
Config Pin Values:
GND = 00
LED[0] = 01
LED[1] = 10
VDDO = 11
Config Pin Mapping:
0: PHYADDR[2:1]
1: PHYADDR[3:4]
2: {P1_PHYADDR[0] P0_PHYADDR[0]}
3: {RGMII_TX_DLY RGMII_RX_DLY}
4: {1/2_MDIO ENA_CROSSOVER}
5: {DIS_SLEEP PDOWN}
Configuration:
0 = VDDO (PHYADDR[2:1]={1 1})
1 = GND (PHYADDR[4:3]={0 0})
2 = LED[0] (P1_PHYADDR[0]=0; P0_PHYADDR[0]=1)
3 = VDDO (RGMII_TX_DLY=1; RGMII_RX_DLY=1)
4 = GND (2 MDIO; ENA_CROSSOVER=0)
5 = LED[1] (DIS_SLEEP=1; PDOWN=0)
R272 4.7k
R282 4.7k
R280 4.7k
R281 4.7k
ETH_PHY_P0_MDIO
ETH_PHY_P1_MDIO
ETH_PHY_P0_INT
ETH_PHY_P1_INT
C442 0.1uF
C458 0.1uF
C461 0.1uF
C464 0.1uF
C463 0.1uF
C449 0.1uF
C445 0.1uF
C459 0.1uF
C467 0.1uF
C143 0.1uF
C465 0.1uF
C462 0.1uF
C466 0.1uF
C469 0.1uF
C468 0.1uF
C139 0.1uF
C447 0.1uF
C443 0.1uF
C444 0.1uF
C448 0.1uF
FB1 FB_0603_220
C141 10uF
C140 1.0nF
FB12 FB_0603_220
C478 10uF
C480 1.0nF
X1
25MHz
C138 18pF
C142 18pF
ETH_XTAL1
ETH_XTAL2
D22
D24
D26
D21
D23
D25
LED (R)
LED (G)
R327 22.6
R328 22.6
R326 10
R325 22.6
R331 22.6
R332 10
ETH_P0_LED0
ETH_P0_LED1
ETH_P0_LED2
ETH_P1_LED0
ETH_P1_LED1
ETH_P1_LED2
Target I 15mA
Red LED Vf@15mA 1.9v
Green LED Vf@15mA 2.1v
PHY_LED_pins V@15mA 0.27
(per IBIS model TTLBIDI12_LED0_V25)
Design: WARP v3
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Description: Ethernet PHY
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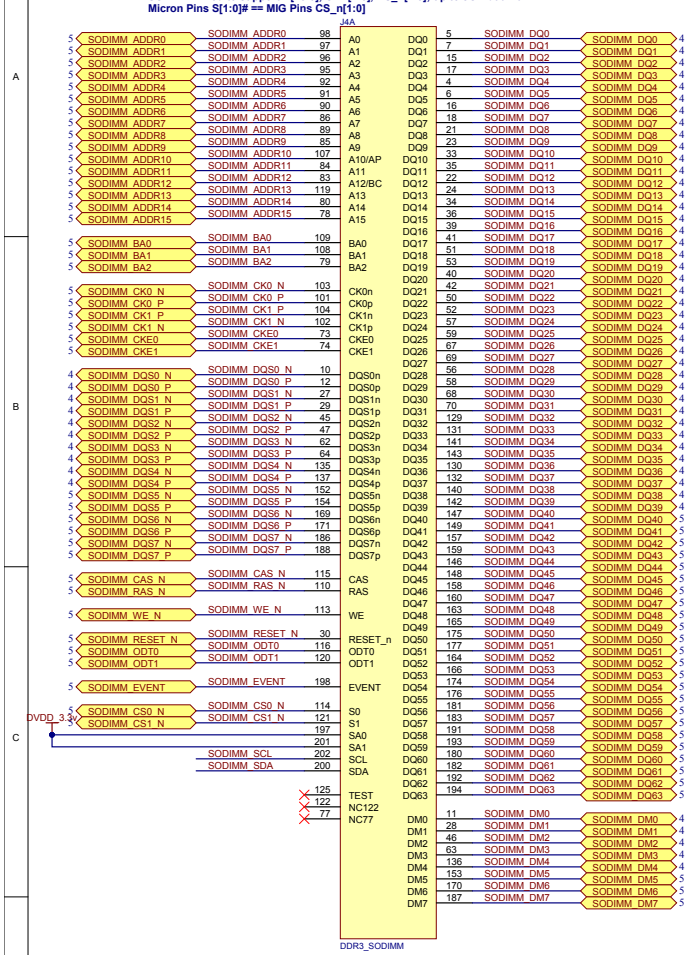
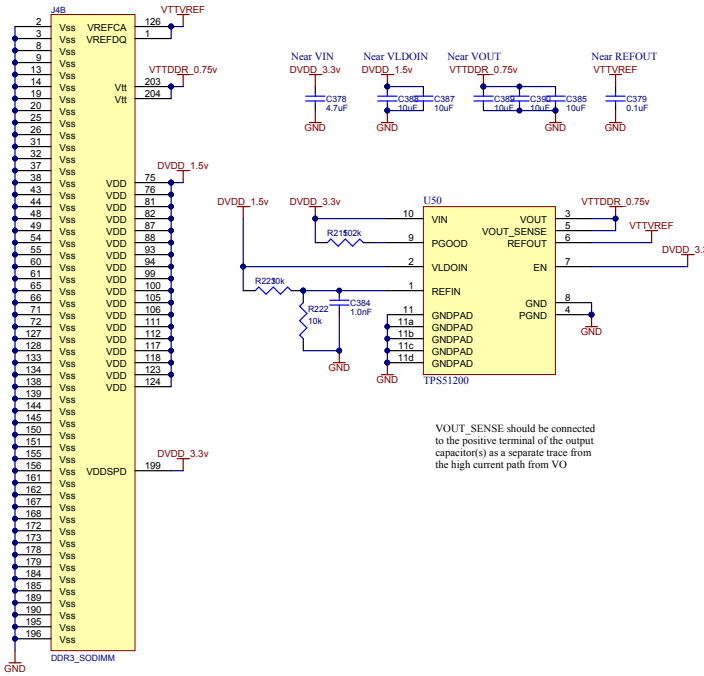
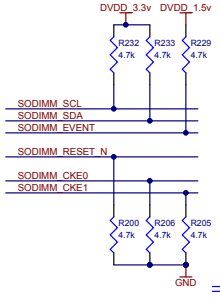
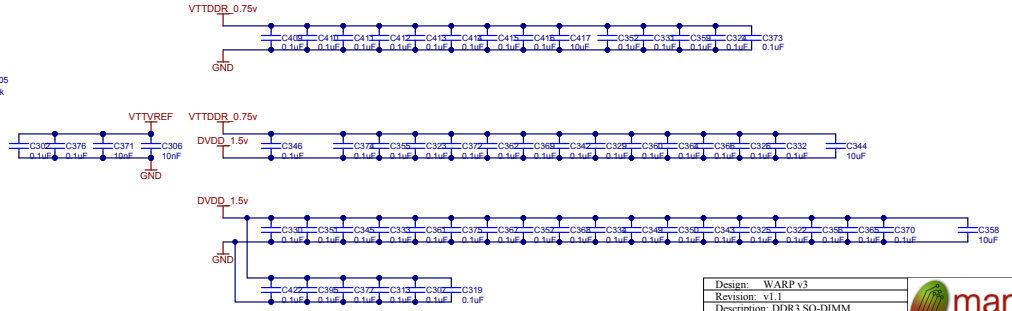
SODIMM wired to support A[15:0], ODT[1:0], CS_n[1:0]; up to 8GB dual rank
Micron Pins S[1:0]# == MIG Pins CS_n[1:0]









Design:	WARP v3
Revision:	v1.1
Description:	DDR3 SO-DIMM
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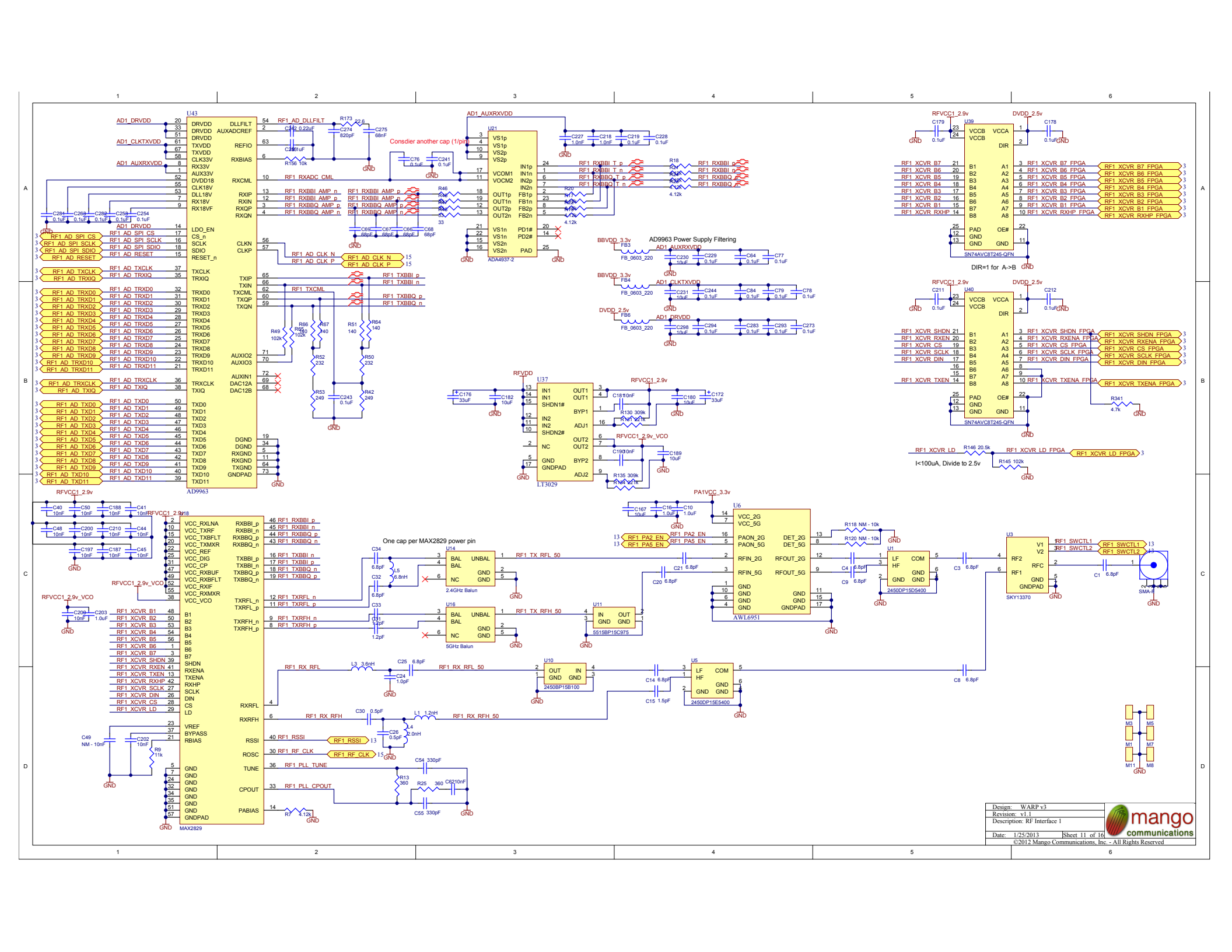
U43
AD9963
U21
ADA4937-2
U37
LT3029
U39
U40
SN74AVC8T245-QFN
U6
AWL6951
U18
MAX2829
U14
U16
2.4GHz Balun
5GHz Balun
U1
2450DP15D5400
U3
SKY13370
U10
2450BP15B100
U5
2450DP15E5400
U11
5515BP15C975
AD9963 Power Supply Filtering
DIR=1 for A->B
I<100uA, Divide to 2.5v
One cap per MAX2829 power pin
Consdier another cap (1/pin)
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Description: RF Interface 1
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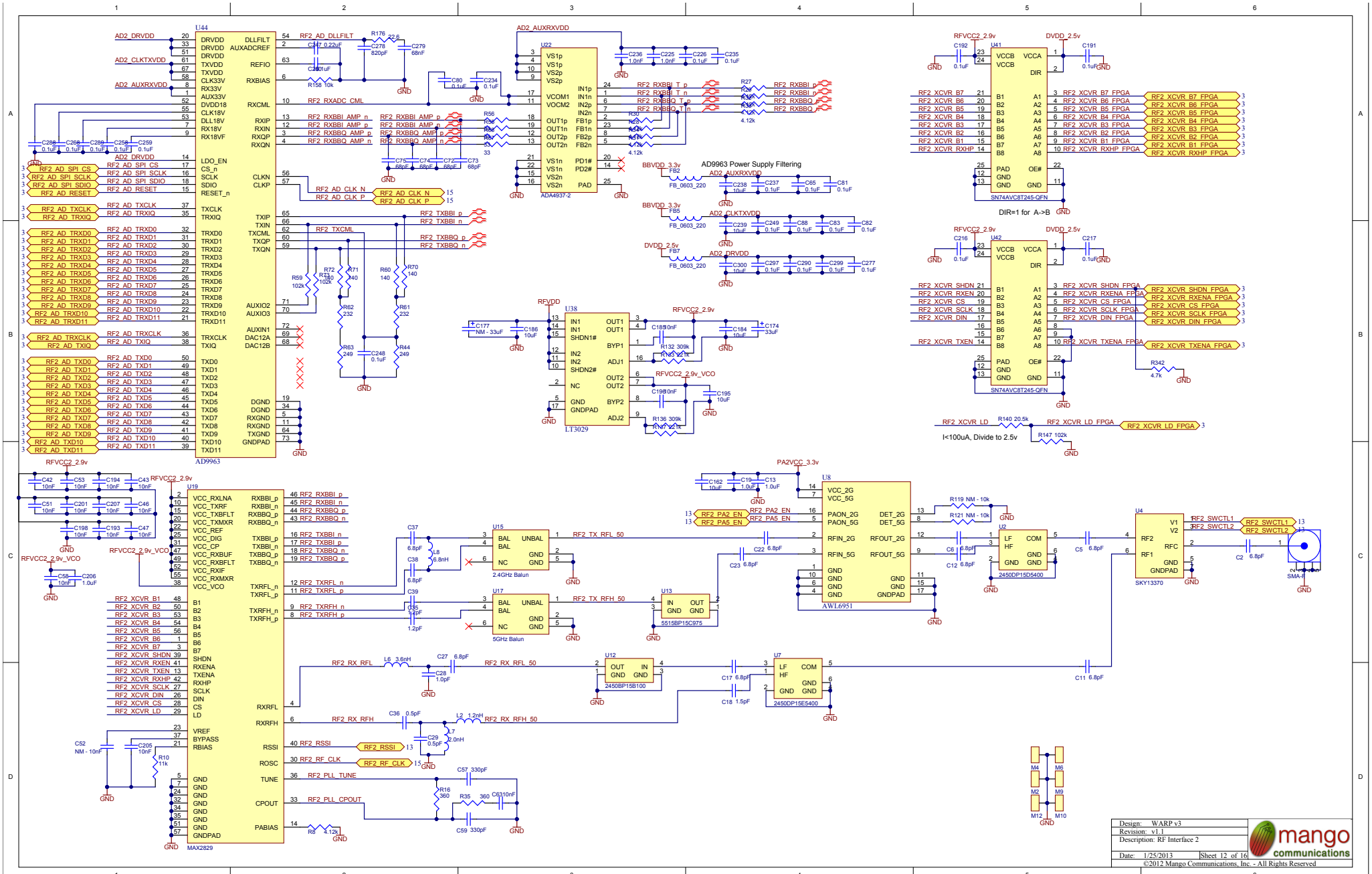
U44
AD9963
AD2_DRVDD
AD2_CLKTXVDD
AD2_AUXRXVDD
RF2_AD_DLLFILT
RF2_AD_RXADC_CML
RF2_AD_SPI_CS
RF2_AD_SPI_SCLK
RF2_AD_SPI_SDIO
RF2_AD_RESET
RF2_AD_CLK_N
RF2_AD_CLK_P
RF2_AD_TXCLK
RF2_AD_TRXIQ
RF2_AD_TXCML
RF2_AD_TRXCLK
RF2_AD_TXIQ
RF2_AD_TXBBI_p
RF2_AD_TXBBI_n
RF2_AD_TXBBQ_p
RF2_AD_TXBBQ_n
RF2_AD_RXBBI_AMP_p
RF2_AD_RXBBI_AMP_n
RF2_AD_RXBBQ_AMP_p
RF2_AD_RXBBQ_AMP_n
U22
ADA4937-2
AD9963 Power Supply Filtering
U38
LT3029
RFVDD
RFVCC2_2.9v
RFVCC2_2.9v_VCO
U41
U42
SN74AVC8T245-QFN
DIR=1 for A->B
RF2_XCVR_LD
I<100uA, Divide to 2.5v
U19
MAX2829
U8
AWL6951
PA2VCC_3.3v
RF2_PA2_EN
RF2_PA5_EN
U15
U17
2.4GHz Balun
5GHz Balun
U13
5515BP15C975
U4
SKY13370
U2
2450DP15D5400
U12
2450BP15B100
U7
2450DP15E5400
RF2_RX_RFL
RF2_RX_RFH
RF2_RSSI
RF2_RF_CLK
RF2_PLL_TUNE
RF2_PLL_CPOUT
RF2_SWCTL1
RF2_SWCTL2
SMA-F
Design: WARP v3
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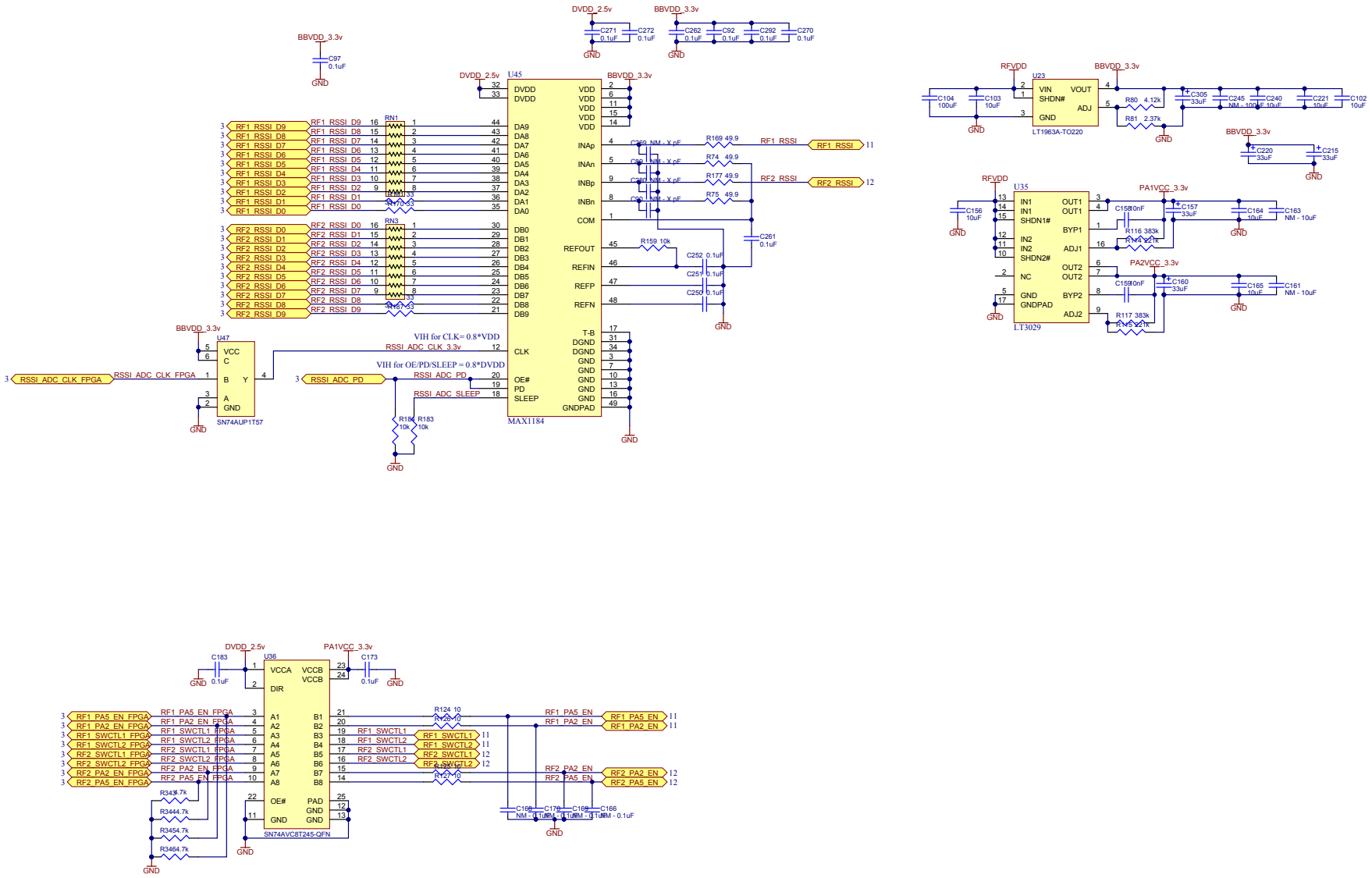
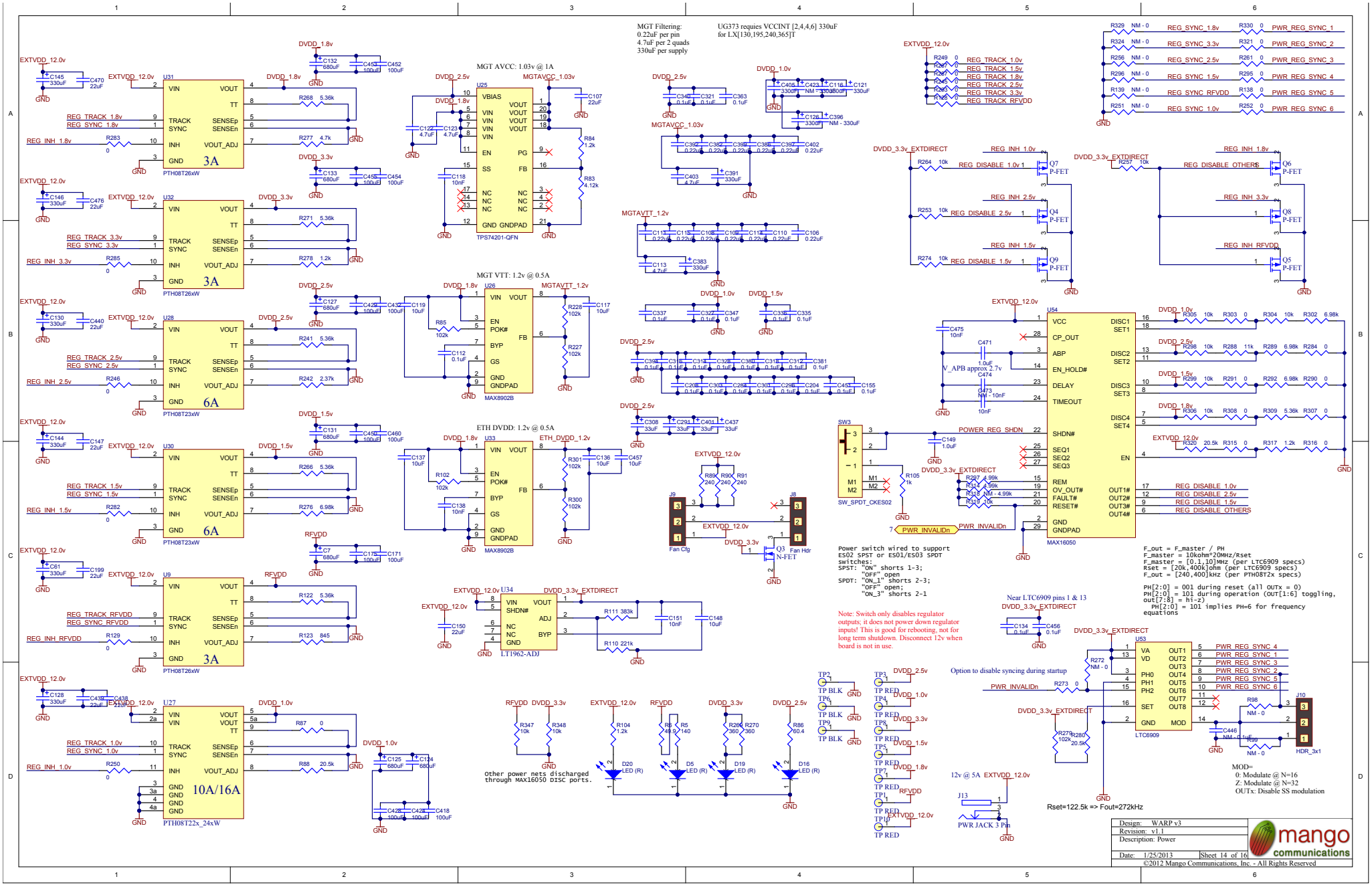


Design:	WARP v3
Revision:	v1.1
Description:	RF Common
Date:	1/25/2013
Sheet	13 of 16


MGT Filtering:
0.22uF per pin
4.7uF per 2 quads
330uF per supply
UG373 requies VCCINT [2,4,4,6] 330uF for LX[130,195,240,365]T
MGT AVCC: 1.03v @ 1A
MGT VTT: 1.2v @ 0.5A
ETH DVDD: 1.2v @ 0.5A
EXTVDD_12.0v
DVDD_1.8v
DVDD_2.5v
DVDD_3.3v
DVDD_1.5v
DVDD_1.0v
MGTAVCC_1.03v
MGTAVTT_1.2v
ETH_DVDD_1.2v
RFVDD
DVDD_3.3v_EXTDIRECT
PTH08T26xW
PTH08T23xW
PTH08T22x_24xW
TPS74201-QFN
MAX8902B
LT1962-ADJ
MAX16050
LTC6909
SW_SPDT_CKES02
Fan Cfg
Fan Hdr
N-FET
P-FET
LED (R)
TP BLK
TP RED
PWR JACK 3 Pin
HDR_3x1
REG_TRACK_1.0v
REG_TRACK_1.5v
REG_TRACK_1.8v
REG_TRACK_2.5v
REG_TRACK_3.3v
REG_TRACK_RFVDD
REG_SYNC_1.8v
REG_SYNC_3.3v
REG_SYNC_2.5v
REG_SYNC_1.5v
REG_SYNC_RFVDD
REG_SYNC_1.0v
PWR_REG_SYNC_1
PWR_REG_SYNC_2
PWR_REG_SYNC_3
PWR_REG_SYNC_4
PWR_REG_SYNC_5
PWR_REG_SYNC_6
REG_INH_1.8v
REG_INH_3.3v
REG_INH_2.5v
REG_INH_1.5v
REG_INH_RFVDD
REG_INH_1.0v
REG_DISABLE_1.0v
REG_DISABLE_2.5v
REG_DISABLE_1.5v
REG_DISABLE_OTHERS
POWER_REG_SHDN
PWR_INVALIDn
Power switch wired to support ES02 SPST or ES01/ES03 SPDT switches:
SPST: "ON" shorts 1-3; "OFF" open
SPDT: "ON_1" shorts 2-3; "OFF" open; "ON_3" shorts 2-1
Note: Switch only disables regulator outputs; it does not power down regulator inputs! This is good for rebooting, not for long term shutdown. Disconnect 12v when board is not in use.
Other power nets discharged through MAX16050 DISC ports.
Near LTC6909 pins 1 & 13
Option to disable syncing during startup
12v @ 5A EXTVDD_12.0v
F_out = F_master / PH
F_master = 10kohm*20Mhz/Rset
F_master = [0.1,10]Mhz (per LTC6909 specs)
Rset = [20k,400k]ohm (per LTC6909 specs)
F_out = [240,400]khz (per PTH08T2x specs)
PH[2:0] = 001 during reset (all OUTx = 0)
PH[2:0] = 101 during operation (OUT[1:6] toggling, out[7:8] = hi-z)
PH[2:0] = 101 implies PH=6 for frequency equations
MOD=
0: Modulate @ N=16
Z: Modulate @ N=32
OUTx: Disable SS modulation
Rset=122.5k => Fout=272kHz
Design: WARP v3
Revision: v1.1
Description: Power
Date: 1/25/2013
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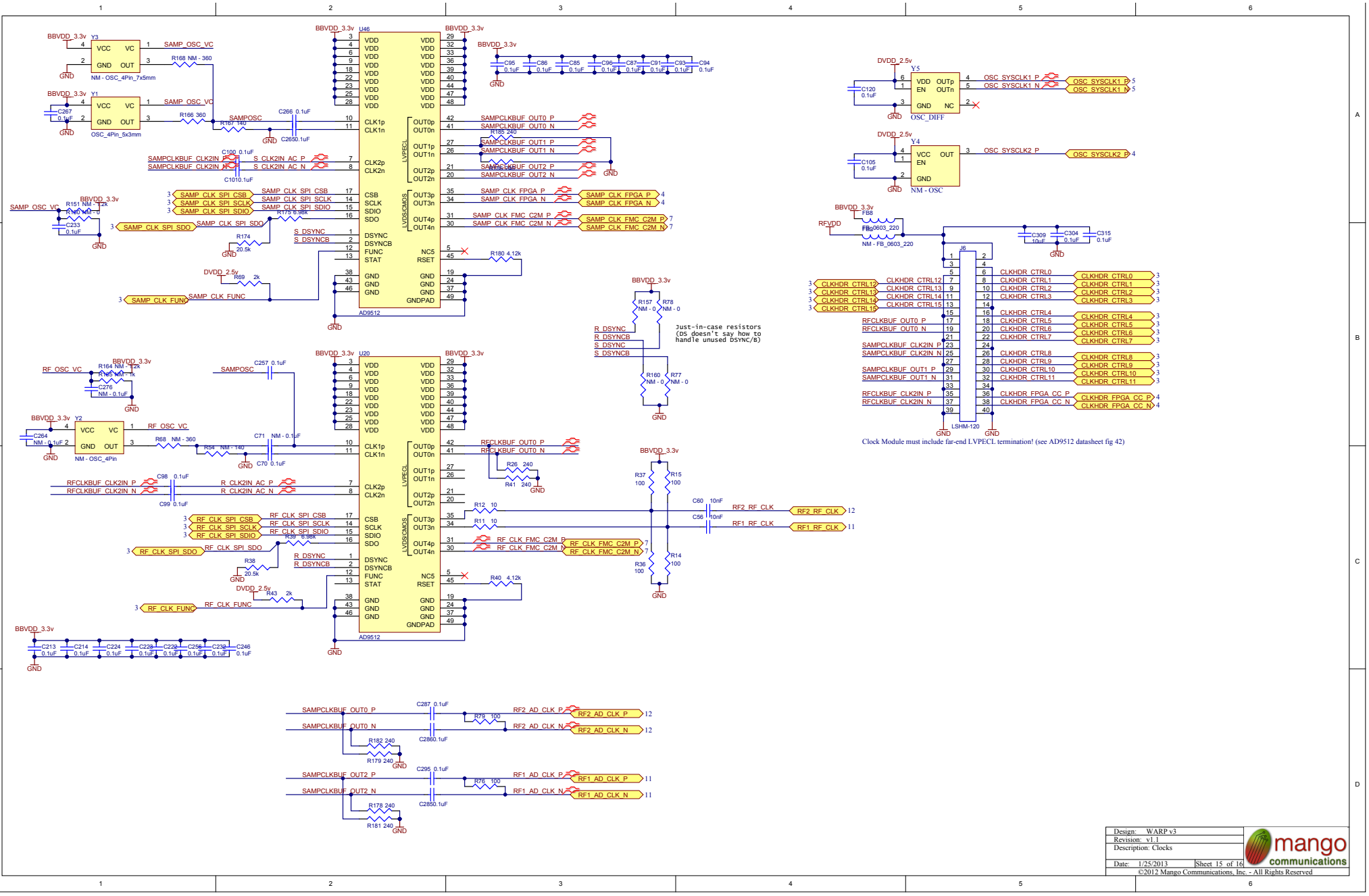
U46
AD9512
U20
AD9512
Y3
NM - OSC_4Pin_7x5mm
Y1
OSC_4Pin_5x3mm
Y2
NM - OSC_4Pin
Y5
OSC_DIFF
Y4
NM - OSC
J6
LSHM-120
Just-in-case resistors (DS doesn't say how to handle unused DSYNC/B)
Clock Module must include far-end LVPECL termination! (see AD9512 datasheet fig 42)
Design: WARP v3
Revision: v1.1
Description: Clocks
Date: 1/25/2013
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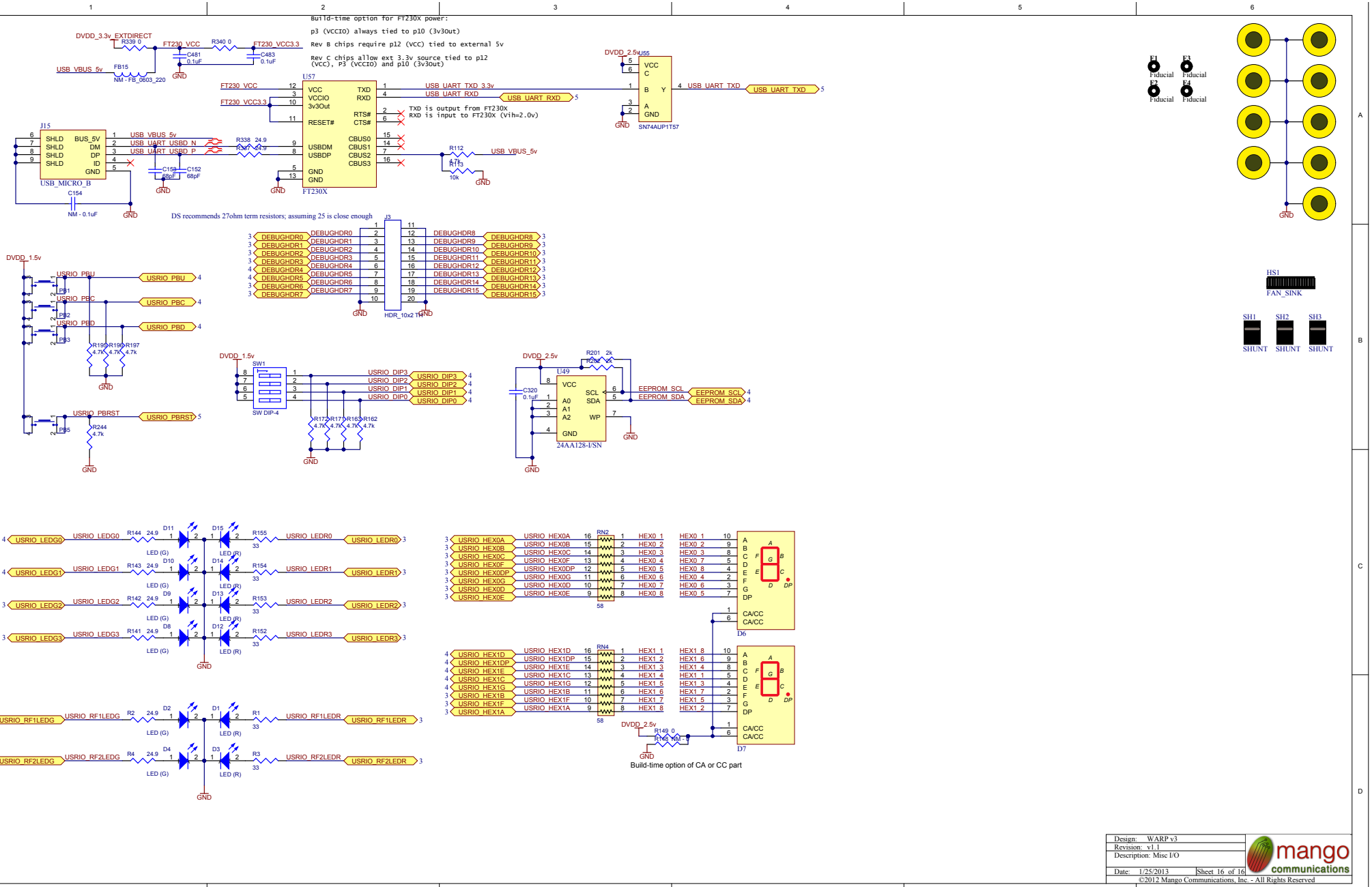

Design:	WARP v3
Revision:	v1.1
Description:	Misc I/O
Date:	1/25/2013
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