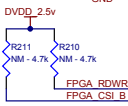
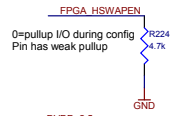
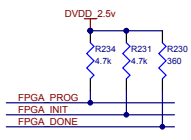
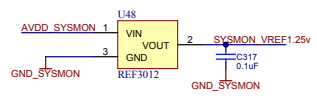
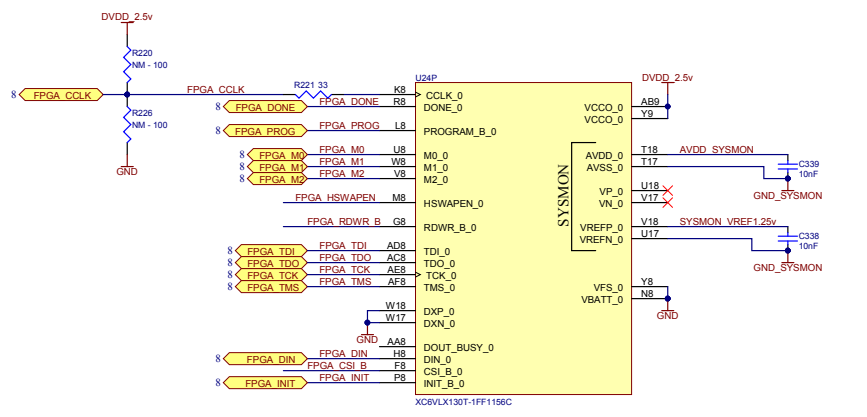
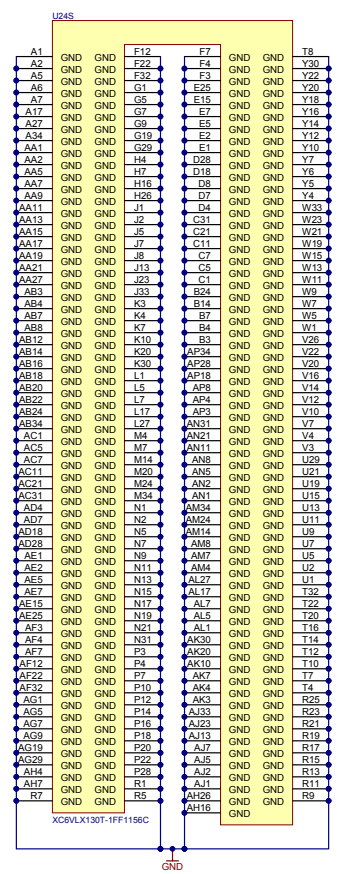
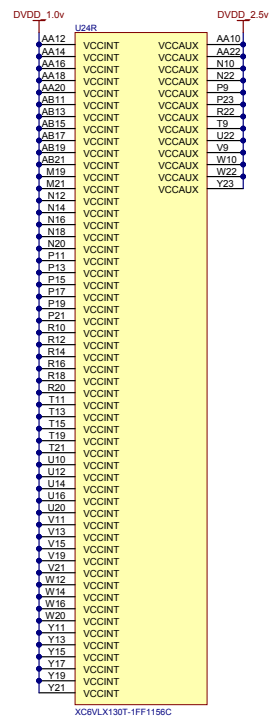


Mango Communications WARP v3  
Rev 1.1

- 1 - Table of Contents
- 2 - FPGA - Power & Config
- 3 - FPGA - Column 1 I/O (RF, User I/O)
- 4 - FPGA - Column 2 I/O (FMC, SO-DIMM)
- 5 - FPGA - Column 3 I/O (FMC, SO-DIMM, Ethernet)
- 6 - FPGA - Column 4 I/O (MGTS)
- 7 - FMC HPC Connector
- 8 - SD Card, Flash & JTAG Configuration
- 9 - Ethernet Interfaces
- 10 - DDR3 SO-DIMM Slot
- 11 - RF Interface 1
- 12 - RF Interface 2
- 13 - RF Common
- 14 - Power
- 15 - Clocks
- 16 - Misc I/O & Mechanical



UG60 claims CSI\_B, RDWR\_B have always-on pullups  
 AN4195 says to tie high  
 Unclear whether it even matters for serial config modes

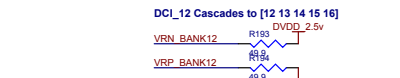


U24A			
<b>BANK 12</b>			
IO_L0P_12	AD25 DEBUGHDR3		
IO_L0N_12	AD26 USRIO HEX1B		
IO_L1P_12	AE7 DEBUGHDR9		
IO_L1N_12	AD27 USRIO HEX1F		
IO_L2P_12	AH33		
IO_L2N_12	AH32 USRIO HEX0A		
IO_L3P_12	AE28 USRIO HEX1C		
IO_L3N_12	AE29 USRIO HEX0E		
IO_L4P_12	AJ34 USRIO RF2LEDR		
IO_L4N_12	AH34 USRIO RF2LEDR		
IO_L5P_12	AF28 DEBUGHDR10		
IO_L5N_12	AF29 USRIO HEX0D		
IO_L6P_12	AL34 USRIO RF1LEDR		
IO_L6N_12	AK34 USRIO RF1LEDR		
IO_L7P_12	AH29 DEBUGHDR12		
IO_L7N_12	AH30 DEBUGHDR6		
IO_L8P_SRC0_12	AN33 USRIO LEDR2		
IO_L8N_SRC0_12	AN34 USRIO LEDR0		
IO_L9P_SRC0_12	AG27 DEBUGHDR0		
IO_L9N_SRC0_12	AG28 DEBUGHDR8		
IO_L10P_SRC0_12	AF30 USRIO HEX0K		
IO_L10N_SRC0_12	AG30 USRIO HEX0J		
IO_L11P_SRC0_12	AF26 DEBUGHDR2		
IO_L11N_SRC0_12	AE26 DEBUGHDR1		
IO_L12P_VRN_12	AJ31 VRN BANK12		
IO_L12N_VRN_12	AJ32 VSP BANK12		
IO_L13P_12	AJ30 DEBUGHDR11		
IO_L13N_12	AJ29 DEBUGHDR1		
IO_L14P_12	AK33 USRIO HEX0B		
IO_L14N_VREF_12	AL31		
IO_L15P_12	AK33 USRIO HEX0E		
IO_L15N_12	AK32 USRIO HEX0F		
IO_L16P_12	AK31 DEBUGHDR7		
IO_L16N_12	AM33 USRIO LEDR1		
IO_L17P_12	AL33 USRIO LEDR3		
IO_L17N_12	AN32 USRIO LEDG3		
IO_L18P_12	AP32 DEBUGHDR15		
IO_L18N_12	AP33 USRIO LEDR3		
IO_L19P_12	AL30 DEBUGHDR13		
IO_L19N_12	AM31 DEBUGHDR14		

U24B			
<b>BANK 13</b>			
IO_L0P_13	AA34 RF1 AD RESET		
IO_L0N_13	AA33 RF1 AD TX10		
IO_L1P_13	AA30 RF1 AD TXD6		
IO_L1N_13	AA31 RF1 AD TXCLK		
IO_L2P_13	AD34 RF1 AD TRXD6		
IO_L2N_13	AE34 RF1 AD TRX10		
IO_L3P_13	AB30 RF1 AD TXD7		
IO_L3N_13	AB31 RF1 AD SPI CS		
IO_L4P_13	AC33 RF1 AD TRXD		
IO_L4N_VREF_13	AE33 RF1 AD SPI SCLK		
IO_L5P_13	AD31 RF1 AD TRXD10		
IO_L5N_13	AD31 RF1 AD TRXD8		
IO_L6P_13	AA25 RF1 AD TXD0		
IO_L6N_13	Y26 RF1 AD TXD2		
IO_L7P_13	AA28 RF1 AD TXD4		
IO_L7N_13	AA29 RF1 AD TXD5		
IO_L8P_SRC0_13	AE34 RF1 XCVR B7 FPGA		
IO_L8N_SRC0_13	AD30 RF1 AD TRXCLK		
IO_L9P_SRC0_13	AC34 RF1 XCVR B5 FPGA		
IO_L9N_SRC0_13	AC30 RF1 AD SPI SDIO		
IO_L10P_SRC0_13	AE33 RF1 XCVR B6 FPGA		
IO_L10N_SRC0_13	AE33 RF1 XCVR B3 FPGA		
IO_L11P_SRC0_13	AD29 RF1 AD TRXD4		
IO_L11N_SRC0_13	AC29 RF1 AD TRXD3		
IO_L12P_VRN_13	AB32 RF1 AD TRXD2		
IO_L12N_VRN_13	AB28 RF1 AD TXD8		
IO_L13P_13	AC28 RF1 AD TXD10		
IO_L13N_13	AD32 RF1 AD TRXD9		
IO_L14P_13	AC22 RF1 AD TRXD7		
IO_L14N_VREF_13	AD27 RF1 AD TXD11		
IO_L15P_13	AG33 RF1 XCVR B1 FPGA		
IO_L15N_13	AG32 RF1 XCVR B2 FPGA		
IO_L16P_13	AA26 RF1 AD TXD3		
IO_L16N_13	AA26 RF1 AD TXD1		
IO_L17P_13	AG31 RF1 XCVR B4 FPGA		
IO_L17N_13	AE31 RF1 XCVR B2 FPGA		
IO_L18P_13	AG31 RF1 XCVR B4 FPGA		
IO_L18N_13	AB25 RF1 AD TRXD1		
IO_L19P_13	AC25 RF1 AD TRXD0		
IO_L19N_13			

U24E			
<b>BANK 16</b>			
IO_L0P_16	C32 RF2 RSSI D4		
IO_L0N_16	B32 RSSI ADC CLK FPGA		
IO_L1P_16	J27		
IO_L1N_16	E32 RF1 RSSI D0		
IO_L2P_16	E33 RF1 RSSI D1		
IO_L2N_16	F30 RF1 RSSI D3		
IO_L3P_16	G30 RF2 RSSI D6		
IO_L3N_16	B33 RF2 RSSI D1		
IO_L4P_16	G31 RF1 RSSI D7		
IO_L4N_VREF_16	H30 FMC PRSNT M2C		
IO_L5P_16	G33 RF2 RSSI D2		
IO_L5N_16	B34 RSSI ADC PD		
IO_L6P_16	K28		
IO_L6N_16	J29		
IO_L7P_16	D34 RF2 RSSI D9		
IO_L7N_16	C34 RF2 RSSI D3		
IO_L8P_SRC0_16	K26		
IO_L8N_SRC0_16	K27		
IO_L9P_SRC0_16	F33 RF1 RSSI D6		
IO_L9N_SRC0_16	G33 RF1 RSSI D8		
IO_L10P_SRC0_16	F31 RF1 RSSI D4		
IO_L10N_SRC0_16	E31 RF2 RSSI D7		
IO_L11P_SRC0_16	E34 RF1 RSSI D2		
IO_L11N_SRC0_16	F34 RF1 RSSI D5		
IO_L12P_VRN_16	J30		
IO_L12N_VRN_16	K29		
IO_L13P_16	H34 RF2 XCVR SCLK FPGA		
IO_L13N_16	H33 RF2 XCVR DIN FPGA		
IO_L14P_16	D31 RF2 RSSI D5		
IO_L14N_VREF_16	D32 RF2 RSSI D8		
IO_L15P_16	K33 RF2 XCVR LD FPGA		
IO_L15N_16	J34 RF2 XCVR SHDN FPGA		
IO_L16P_16	G32 RF1 RSSI D9		
IO_L16N_16	L25 RF2 XCVR TXENA FPGA		
IO_L17P_16			
IO_L17N_16			
IO_L18P_16	L26 RF CLK FUNC		
IO_L18N_16	J31 RF2 XCVR RXENA FPGA		
IO_L19P_16	J32 RF2 XCVR CS FPGA		
IO_L19N_16			

U24F			
<b>BANK 17</b>			
RF1 RSSI D9	RF1 RSSI D8	13	
RF1 RSSI D7	RF1 RSSI D8	13	
RF1 RSSI D6	RF1 RSSI D7	13	
RF1 RSSI D5	RF1 RSSI D6	13	
RF1 RSSI D4	RF1 RSSI D5	13	
RF1 RSSI D3	RF1 RSSI D4	13	
RF1 RSSI D2	RF1 RSSI D3	13	
RF1 RSSI D1	RF1 RSSI D2	13	
RF1 RSSI D0	RF1 RSSI D1	13	
RF2 RSSI D9	RF2 RSSI D8	13	
RF2 RSSI D7	RF2 RSSI D8	13	
RF2 RSSI D6	RF2 RSSI D7	13	
RF2 RSSI D5	RF2 RSSI D6	13	
RF2 RSSI D4	RF2 RSSI D5	13	
RF2 RSSI D3	RF2 RSSI D4	13	
RF2 RSSI D2	RF2 RSSI D3	13	
RF2 RSSI D1	RF2 RSSI D2	13	
RF2 RSSI D0	RF2 RSSI D1	13	
RF2 AD SPI CS	RF2 AD SPI CS	12	
RF2 AD SPI SCLK	RF2 AD SPI SCLK	12	
RF2 AD SPI SDIO	RF2 AD SPI SDIO	12	
RF2 AD RESET	RF2 AD RESET	12	
RF2 AD TXCLK	RF2 AD TXCLK	12	
RF2 AD TRXIQ	RF2 AD TRXIQ	12	
RF2 AD TRXD0	RF2 AD TRXD0	12	
RF2 AD TRXD1	RF2 AD TRXD1	12	
RF2 AD TRXD2	RF2 AD TRXD2	12	
RF2 AD TRXD3	RF2 AD TRXD3	12	
RF2 AD TRXD4	RF2 AD TRXD4	12	
RF2 AD TRXD5	RF2 AD TRXD5	12	
RF2 AD TRXD6	RF2 AD TRXD6	12	
RF2 AD TRXD7	RF2 AD TRXD7	12	
RF2 AD TRXD8	RF2 AD TRXD8	12	
RF2 AD TRXD9	RF2 AD TRXD9	12	
RF2 AD TRXD10	RF2 AD TRXD10	12	
RF2 AD TRXD11	RF2 AD TRXD11	12	
RSSI ADC CLK FPGA	RSSI ADC CLK FPGA	13	
RSSI ADC PD	RSSI ADC PD	13	
RF2 XCVR B1 FPGA	RF2 XCVR B1 FPGA	12	
RF2 XCVR B2 FPGA	RF2 XCVR B2 FPGA	12	
RF2 XCVR B3 FPGA	RF2 XCVR B3 FPGA	12	
RF2 XCVR B4 FPGA	RF2 XCVR B4 FPGA	12	
RF2 XCVR B5 FPGA	RF2 XCVR B5 FPGA	12	
RF2 XCVR B6 FPGA	RF2 XCVR B6 FPGA	12	
RF2 XCVR B7 FPGA	RF2 XCVR B7 FPGA	12	
RF2 XCVR SHDN FPGA	RF2 XCVR SHDN FPGA	12	
RF2 XCVR RXENA FPGA	RF2 XCVR RXENA FPGA	12	
RF2 XCVR TXENA FPGA	RF2 XCVR TXENA FPGA	12	
RF2 XCVR RHPH FPGA	RF2 XCVR RHPH FPGA	12	
RF2 XCVR DIN FPGA	RF2 XCVR SCLK FPGA	12	
RF2 XCVR CS FPGA	RF2 XCVR DIN FPGA	12	
RF2 XCVR LD FPGA	RF2 XCVR LD FPGA	12	
RF2 PA5 EN FPGA	RF2 PA5 EN FPGA	13	
RF2 PA2 EN FPGA	RF2 PA2 EN FPGA	13	
RF2 SWCTL2 FPGA	RF2 SWCTL2 FPGA	13	
RF2 SWCTL1 FPGA	RF2 SWCTL1 FPGA	13	



U24G			
<b>BANK 15</b>			
IO_L0P_15	M31 RF2 AD TXD4		
IO_L0N_15	L31 RF2 AD TXD7		
IO_L1P_15	N25 RF2 AD TRXD0		
IO_L1N_15	M25 RF2 AD TRXD1		
IO_L2P_15	K31 RF2 AD TXD11		
IO_L2N_15	M29 RF2 AD TRXD1		
IO_L3P_15	P30 RF2 AD TRXD9		
IO_L3N_15	P31 RF2 AD TRXD11		
IO_L4P_15	N27 RF2 AD TRXD3		
IO_L4N_VREF_15	P27 RF2 XCVR B1 FPGA		
IO_L5P_15	L33 RF2 AD TXD6		
IO_L5N_SRC0_15	M32 RF2 AD TXD2		
IO_L6P_15	L28 RF2 AD TXCLK		
IO_L6N_SRC0_15	M29 RF2 AD TXD8		
IO_L7P_15	N32 RF2 AD SPI CS		
IO_L7N_15	P32 RF2 AD SPI SCLK		
IO_L8P_SRC0_15	N28 RF2 AD TRXD2		
IO_L8N_SRC0_15	N29 RF2 AD TRXD7		
IO_L9P_SRC0_15	N33 RF2 AD TRXCLK		
IO_L9N_SRC0_15	M33 RF2 AD TRXIQ		
IO_L10P_SRC0_15	L29 RF2 AD TXD0		
IO_L10N_SRC0_15	L30 RF2 AD TXD5		
IO_L11P_SRC0_15	P25 RF2 AD TRXD10		
IO_L11N_SRC0_15	P26 RF2 AD TRXD8		
IO_L12P_VRN_15	R28 RF2 XCVR RHPH FPGA		
IO_L12N_VRN_15	R28 RF2 XCVR B2 FPGA		
IO_L13P_15	R31 RF2 XCVR B7 FPGA		
IO_L13N_15	R32 RF2 XCVR B5 FPGA		
IO_L14P_15	R26 RF2 XCVR B4 FPGA		
IO_L14N_VREF_15	R26 RF2 XCVR B6 FPGA		
IO_L15P_15	X34 RF2 AD TXD3		
IO_L15N_SRC0_15	L34 RF2 AD TXD9		
IO_L16P_15	M30 RF2 AD TRXD5		
IO_L16N_VRN_15	N32 RF2 AD TRXD6		
IO_L17P_15	N34 RF2 AD RESET		
IO_L17N_15	P34 RF2 AD SPI SDIO		
IO_L18P_15	P29 RF2 AD TRXD4		
IO_L18N_15	R29 RF2 XCVR B3 FPGA		
IO_L19P_15			
IO_L19N_15			

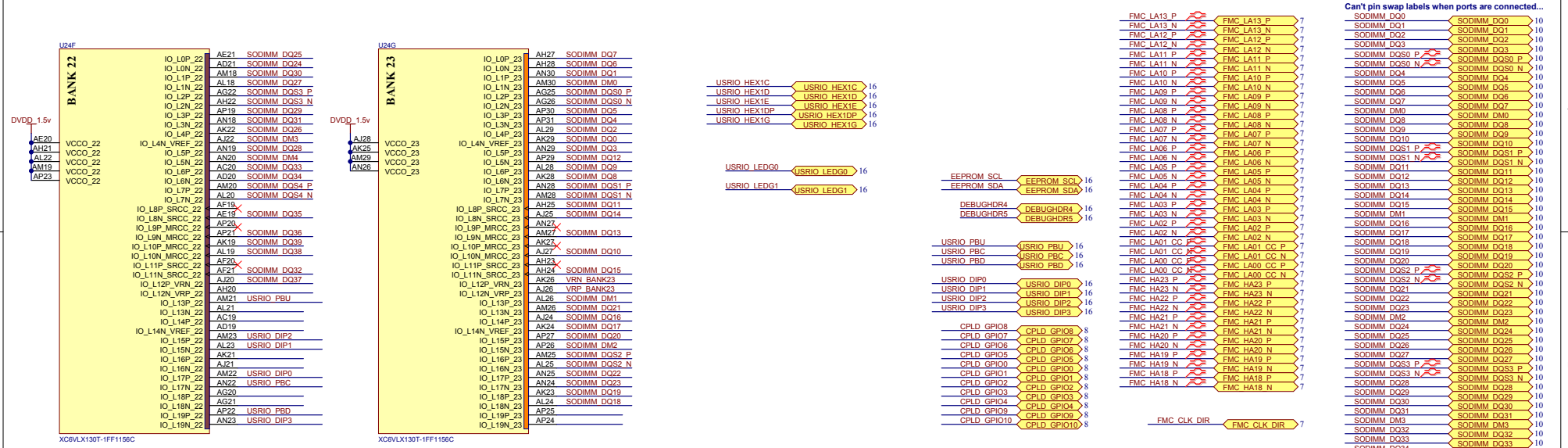
U24C			
<b>BANK 14</b>			
IO_L0P_14	U25 RF1 PA2 EN FPGA		
IO_L0N_14	T25 RF2 PA2 EN FPGA		
IO_L1P_14	T29 RF2 SWCTL2 FPGA		
IO_L1N_14	R33 SAMP CLK FUNC		
IO_L2P_14	R34 CLKHDR CTRL13		
IO_L2N_14	T30 RF2 SWCTL1 FPGA		
IO_L3P_14	T31 RF1 XCVR TXENA FPGA		
IO_L3N_14	T33 RF1 XCVR DIN FPGA		
IO_L4P_14	T34 RF1 XCVR SCLK FPGA		
IO_L4N_VREF_14	U27 RF1 XCVR LD FPGA		
IO_L5P_14	U27 RF1 XCVR SHDN FPGA		
IO_L5N_14	U33 RF1 XCVR RXENA FPGA		
IO_L6P_14	U32 RF1 XCVR CS FPGA		
IO_L6N_14	U29 RF1 PA5 EN FPGA		
IO_L7P_14	U29 CLKHDR CTRL15		
IO_L7N_14	U31 RF1 SWCTL1 FPGA		
IO_L8P_SRC0_14	U30 RF1 SWCTL2 FPGA		
IO_L8N_SRC0_14	W30 CLKHDR CTRL12		
IO_L9P_SRC0_14	U30 CLKHDR CTRL6		
IO_L9N_SRC0_14	V34 CLKHDR CTRL0		
IO_L10P_SRC0_14	U34 CLKHDR CTRL3		
IO_L10N_SRC0_14	V32 CLKHDR CTRL4		
IO_L11P_SRC0_14	V27 CLKHDR CTRL2		
IO_L11N_SRC0_14	V32 CLKHDR CTRL4		
IO_L12P_VRN_14	V33 CLKHDR CTRL1		
IO_L12N_VRN_14	V32 CLKHDR CTRL1		
IO_L13P_14	V31 CLKHDR CTRL10		
IO_L13N_14	V33 CLKHDR CTRL9		
IO_L14P_14	V34 CLKHDR CTRL5		
IO_L14N_VREF_14	V29 CLKHDR CTRL1		
IO_L15P_14	W29 SAMP CLK SPI SDIO		
IO_L15N_14	W31 SAMP CLK SPI CSB		
IO_L16P_14	W29 SAMP CLK SPI SCLK		
IO_L16N_14	W29 SAMP CLK SPI SCLK		
IO_L17P_14	W27 RF CLK SPI SDIO		
IO_L17N_14	W25 RF CLK SPI SDIO		
IO_L18P_14	W25 RF CLK SPI SCLK		
IO_L18N_14	W27 RF CLK SPI CSB		
IO_L19P_14			
IO_L19N_14	W26 CLKHDR CTRL14		



U24D			
<b>BANK 15</b>			
VCCO_15	M29		
VCCO_15	N26		
VCCO_15	P33		
VCCO_15	R30		

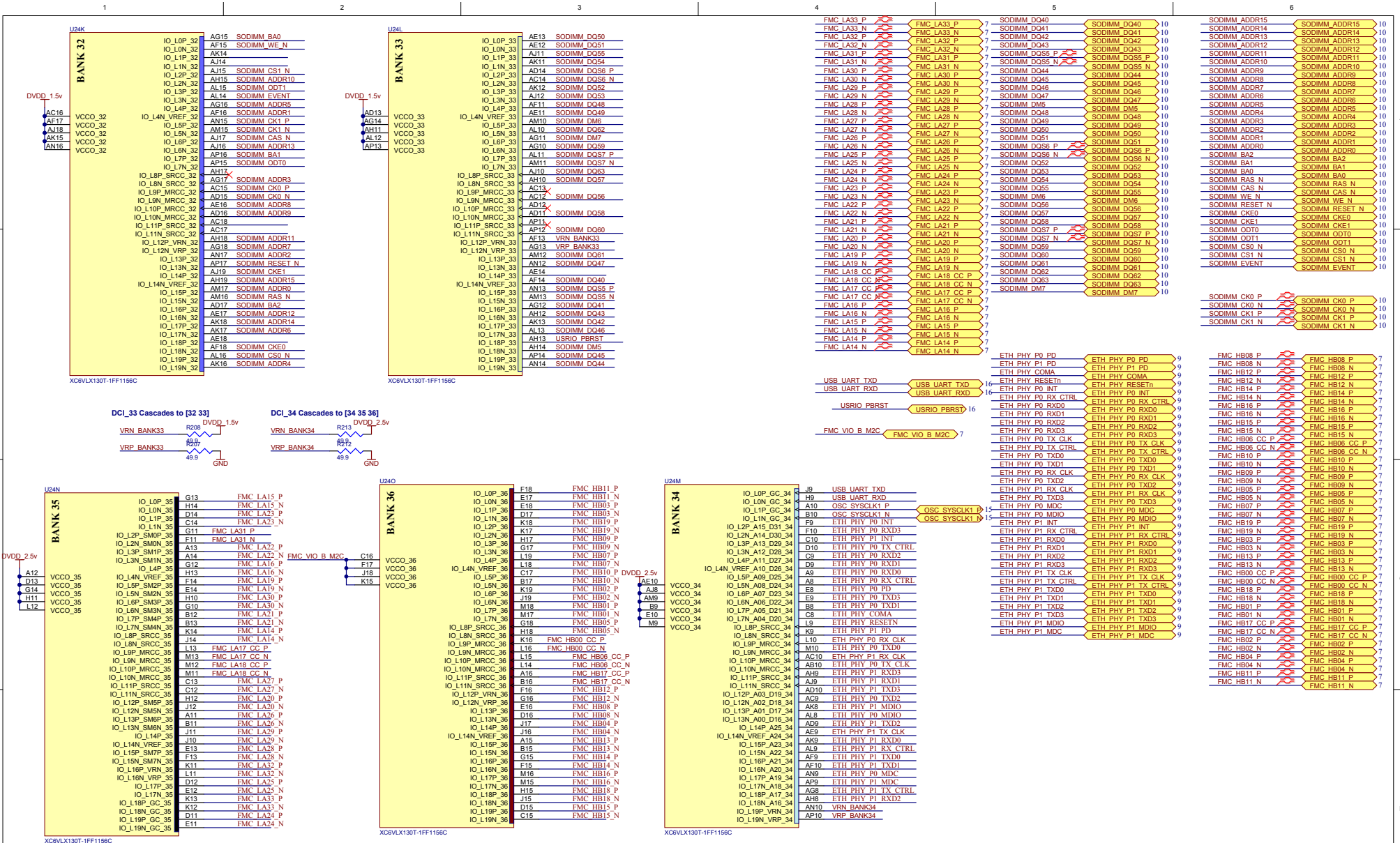
U24H			
<b>BANK 17</b>			
DEBUGHDR0	DEBUGHDR0	16	
DEBUGHDR1	DEBUGHDR1	16	
DEBUGHDR2	DEBUGHDR2	16	
DEBUGHDR3	DEBUGHDR3	16	
DEBUGHDR6	DEBUGHDR6	16	
DEBUGHDR7	DEBUGHDR7	16	
DEBUGHDR8	DEBUGHDR8	16	
DEBUGHDR9	DEBUGHDR9	16	
DEBUGHDR10	DEBUGHDR10	16	
DEBUGHDR11	DEBUGHDR11	16	
DEBUGHDR12	DEBUGHDR12	16	
DEBUGHDR14	DEBUGHDR14	16	
DEBUGHDR15	DEBUGHDR15	16	
RF1 AD TXIQ	RF1 AD TXIQ	11	
RF1 AD TXD0	RF1 AD TXD0	11	
RF1 AD TXD1	RF1 AD TXD1	11	
RF1 AD TXD2	RF1 AD TXD2	11	
RF1 AD TXD3	RF1 AD TXD3	11	
RF1 AD TXD4	RF1 AD TXD4	11	
RF1 AD TXD5	RF1 AD TXD5	11	
RF1 AD TXD6	RF1 AD TXD6	11	
RF1 AD TXD7	RF1 AD TXD7	11	
RF1 AD TXD8	RF1 AD TXD8	11	
RF1 AD TXD9	RF1 AD TXD9	11	
RF1 AD TXD10	RF1 AD TXD10	11	
RF1 AD TXD11	RF1 AD TXD11	11	
CLKHDR CTRL12	CLKHDR CTRL12	15	
CLKHDR CTRL13	CLKHDR CTRL13	15	
CLKHDR CTRL14	CLKHDR CTRL14	15	
CLKHDR CTRL15	CLKHDR CTRL15	15	





Can't pin swap labels when ports are connected...





A

A

B

B

C

C

D

D



Only 8 MGTs are used, all in the North half of the chip. South MGTs are unused.

Per UG366, unused MGTs are connected as:  
 MGTAVCC=GND  
 MGTAVTT=GND  
 MGTREFCLKx=Float  
 MGTTRXx=GND  
 MGTTXx=Float

FMC HPC Bank LA			
LA00_N_CC	G7	FMC LA00 CC N	FMC LA00 CC N
LA00_P_CC	D6	FMC LA00 CC P	FMC LA00 CC P
LA01_N_CC	D9	FMC LA01 CC N	FMC LA01 CC N
LA01_P_CC	H7	FMC LA02 N	FMC LA01 CC P
LA02_N	H8	FMC LA02 P	FMC LA02 N
LA03_N	G9	FMC LA03 P	FMC LA03 N
LA03_P	H10	FMC LA04 N	FMC LA03 P
LA04_N	H11	FMC LA04 P	FMC LA04 N
LA04_P	H12	FMC LA05 N	FMC LA04 P
LA05_N	C10	FMC LA06 N	FMC LA05 N
LA05_P	C11	FMC LA06 P	FMC LA06 N
LA06_N	D11	FMC LA07 N	FMC LA06 P
LA06_P	D12	FMC LA07 P	FMC LA07 N
LA07_N	H13	FMC LA08 N	FMC LA07 P
LA07_P	G13	FMC LA08 P	FMC LA08 N
LA08_N	D12	FMC LA08 P	FMC LA08 N
LA08_P	G15	FMC LA09 N	FMC LA09 N
LA09_N	D14	FMC LA09 P	FMC LA09 N
LA09_P	C15	FMC LA10 N	FMC LA09 P
LA10_N	C14	FMC LA10 P	FMC LA10 N
LA10_P	H17	FMC LA11 N	FMC LA11 N
LA11_N	H18	FMC LA11 P	FMC LA11 P
LA11_P	G16	FMC LA12 N	FMC LA12 N
LA12_N	G15	FMC LA12 P	FMC LA12 N
LA12_P	D18	FMC LA13 N	FMC LA13 N
LA13_N	D17	FMC LA13 P	FMC LA13 P
LA13_P	C19	FMC LA14 N	FMC LA14 N
LA14_N	C18	FMC LA14 P	FMC LA14 P
LA14_P	H20	FMC LA15 N	FMC LA15 N
LA15_N	H19	FMC LA15 P	FMC LA15 P
LA15_P	G19	FMC LA16 N	FMC LA16 N
LA16_N	H18	FMC LA16 P	FMC LA16 P
LA16_P	D21	FMC LA17 CC N	FMC LA17 CC N
LA17_N_CC	D20	FMC LA17 CC P	FMC LA17 CC P
LA17_P_CC	C22	FMC LA18 CC N	FMC LA18 CC N
LA18_N_CC	C23	FMC LA18 CC P	FMC LA18 CC P
LA18_P_CC	H23	FMC LA19 N	FMC LA19 N
LA19_N	H22	FMC LA19 P	FMC LA19 P
LA19_P	G22	FMC LA20 N	FMC LA20 N
LA20_N	G21	FMC LA20 P	FMC LA20 P
LA20_P	H25	FMC LA21 N	FMC LA21 N
LA21_N	H26	FMC LA21 P	FMC LA21 P
LA21_P	G25	FMC LA22 N	FMC LA22 N
LA22_N	G24	FMC LA22 P	FMC LA22 P
LA22_P	D24	FMC LA23 N	FMC LA23 N
LA23_N	D23	FMC LA23 P	FMC LA23 P
LA23_P	H29	FMC LA24 N	FMC LA24 N
LA24_N	H28	FMC LA24 P	FMC LA24 P
LA24_P	G28	FMC LA25 N	FMC LA25 N
LA25_N	G27	FMC LA25 P	FMC LA25 P
LA25_P	D27	FMC LA26 N	FMC LA26 N
LA26_N	D26	FMC LA26 P	FMC LA26 P
LA26_P	C27	FMC LA27 N	FMC LA27 N
LA27_N	C28	FMC LA27 P	FMC LA27 P
LA27_P	H32	FMC LA28 N	FMC LA28 N
LA28_N	H31	FMC LA28 P	FMC LA28 P
LA28_P	G30	FMC LA29 N	FMC LA29 N
LA29_N	G31	FMC LA29 P	FMC LA29 P
LA29_P	H34	FMC LA30 N	FMC LA30 N
LA30_N	H33	FMC LA30 P	FMC LA30 P
LA30_P	G34	FMC LA31 N	FMC LA31 N
LA31_N	G33	FMC LA31 P	FMC LA31 P
LA31_P	H38	FMC LA32 N	FMC LA32 N
LA32_N	H37	FMC LA32 P	FMC LA32 P
LA32_P	G37	FMC LA33 N	FMC LA33 N
LA33_N	G36	FMC LA33 P	FMC LA33 P

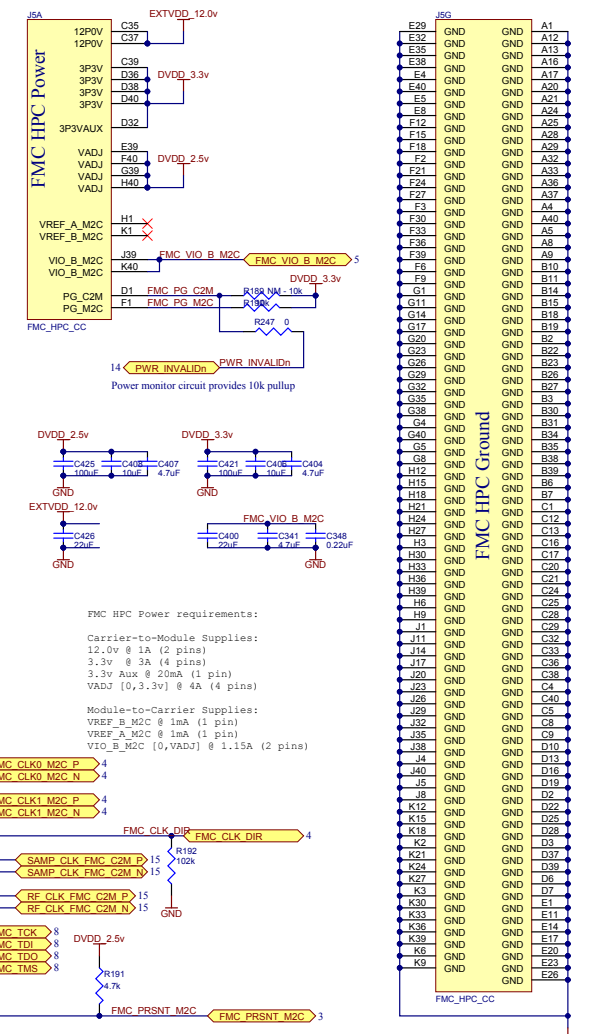
FMC HPC Bank HB			
HB00_N_CC	K26	FMC HB00 CC N	FMC HB00 CC N
HB00_P_CC	K25	FMC HB00 CC P	FMC HB00 CC P
HB01_N	J24	FMC HB01 N	FMC HB01 N
HB01_P	J23	FMC HB01 P	FMC HB01 P
HB02_N	F22	FMC HB02 N	FMC HB02 N
HB02_P	F21	FMC HB02 P	FMC HB02 P
HB03_N	E22	FMC HB03 N	FMC HB03 N
HB03_P	E21	FMC HB03 P	FMC HB03 P
HB04_N	F26	FMC HB04 N	FMC HB04 N
HB04_P	F25	FMC HB04 P	FMC HB04 P
HB05_N	E24	FMC HB05 N	FMC HB05 N
HB05_P	E23	FMC HB05 P	FMC HB05 P
HB06_N_CC	K29	FMC HB06 CC N	FMC HB06 CC N
HB06_P_CC	K28	FMC HB06 CC P	FMC HB06 CC P
HB07_N	J27	FMC HB07 N	FMC HB07 N
HB07_P	J26	FMC HB07 P	FMC HB07 P
HB08_N	F28	FMC HB08 N	FMC HB08 N
HB08_P	F27	FMC HB08 P	FMC HB08 P
HB09_N	E27	FMC HB09 N	FMC HB09 N
HB09_P	E26	FMC HB09 P	FMC HB09 P
HB10_N	K32	FMC HB10 N	FMC HB10 N
HB10_P	K31	FMC HB10 P	FMC HB10 P
HB11_N	J30	FMC HB11 N	FMC HB11 N
HB11_P	J29	FMC HB11 P	FMC HB11 P
HB12_N	F32	FMC HB12 N	FMC HB12 N
HB12_P	F31	FMC HB12 P	FMC HB12 P
HB13_N	E31	FMC HB13 N	FMC HB13 N
HB13_P	E30	FMC HB13 P	FMC HB13 P
HB14_N	K34	FMC HB14 N	FMC HB14 N
HB14_P	K33	FMC HB14 P	FMC HB14 P
HB15_N	J33	FMC HB15 N	FMC HB15 N
HB15_P	J32	FMC HB15 P	FMC HB15 P
HB16_N	F34	FMC HB16 N	FMC HB16 N
HB16_P	F33	FMC HB16 P	FMC HB16 P
HB17_N_CC	K37	FMC HB17 CC N	FMC HB17 CC N
HB17_P_CC	K36	FMC HB17 CC P	FMC HB17 CC P
HB18_N	J37	FMC HB18 N	FMC HB18 N
HB18_P	J36	FMC HB18 P	FMC HB18 P
HB19_N	F34	FMC HB19 N	FMC HB19 N
HB19_P	F33	FMC HB19 P	FMC HB19 P
HB20_N	F38	FMC HB20 N	FMC HB20 N
HB20_P	F37	FMC HB20 P	FMC HB20 P
HB21_N	E36	FMC HB21 N	FMC HB21 N
HB21_P	E35	FMC HB21 P	FMC HB21 P

FMC HPC Bank HA			
HA00_N_CC	F5	FMC HA00 CC N	FMC HA00 CC N
HA00_P_CC	F4	FMC HA00 CC P	FMC HA00 CC P
HA01_N_CC	E3	FMC HA01 CC N	FMC HA01 CC N
HA01_P_CC	E2	FMC HA01 CC P	FMC HA01 CC P
HA02_N	K8	FMC HA02 N	FMC HA02 N
HA02_P	K7	FMC HA02 P	FMC HA02 P
HA03_N	J7	FMC HA03 N	FMC HA03 N
HA03_P	J6	FMC HA03 P	FMC HA03 P
HA04_N	F8	FMC HA04 N	FMC HA04 N
HA04_P	F7	FMC HA04 P	FMC HA04 P
HA05_N	E7	FMC HA05 N	FMC HA05 N
HA05_P	E6	FMC HA05 P	FMC HA05 P
HA06_N	K11	FMC HA06 N	FMC HA06 N
HA06_P	K10	FMC HA06 P	FMC HA06 P
HA07_N	J10	FMC HA07 N	FMC HA07 N
HA07_P	J9	FMC HA07 P	FMC HA07 P
HA08_N	F11	FMC HA08 N	FMC HA08 N
HA08_P	F10	FMC HA08 P	FMC HA08 P
HA09_N	E10	FMC HA09 N	FMC HA09 N
HA09_P	E9	FMC HA09 P	FMC HA09 P
HA10_N	K14	FMC HA10 N	FMC HA10 N
HA10_P	K13	FMC HA10 P	FMC HA10 P
HA11_N	J13	FMC HA11 N	FMC HA11 N
HA11_P	J12	FMC HA11 P	FMC HA11 P
HA12_N	F14	FMC HA12 N	FMC HA12 N
HA12_P	F13	FMC HA12 P	FMC HA12 P
HA13_N	E13	FMC HA13 N	FMC HA13 N
HA13_P	E12	FMC HA13 P	FMC HA13 P
HA14_N	J16	FMC HA14 N	FMC HA14 N
HA14_P	J15	FMC HA14 P	FMC HA14 P
HA15_N	F17	FMC HA15 N	FMC HA15 N
HA15_P	F16	FMC HA15 P	FMC HA15 P
HA16_N	E16	FMC HA16 N	FMC HA16 N
HA16_P	E15	FMC HA16 P	FMC HA16 P
HA17_N_CC	K17	FMC HA17 CC N	FMC HA17 CC N
HA17_P_CC	K16	FMC HA17 CC P	FMC HA17 CC P
HA18_N	J19	FMC HA18 N	FMC HA18 N
HA18_P	J18	FMC HA18 P	FMC HA18 P
HA19_N	F20	FMC HA19 N	FMC HA19 N
HA19_P	F19	FMC HA19 P	FMC HA19 P
HA20_N	E18	FMC HA20 N	FMC HA20 N
HA20_P	E17	FMC HA20 P	FMC HA20 P
HA21_N	K20	FMC HA21 N	FMC HA21 N
HA21_P	K19	FMC HA21 P	FMC HA21 P
HA22_N	J22	FMC HA22 N	FMC HA22 N
HA22_P	J21	FMC HA22 P	FMC HA22 P
HA23_N	K23	FMC HA23 N	FMC HA23 N
HA23_P	K22	FMC HA23 P	FMC HA23 P

LVDS clocks driven by FMC module (per VITA 57.1)

FMC HPC MGTS			
GBTCLK0_M2C_P	D4	FMC MGTCLK 0 P	FMC MGTCLK 0 P
GBTCLK0_M2C_N	D5	FMC MGTCLK 0 N	FMC MGTCLK 0 N
GBTCLK1_M2C_P	B20	FMC MGTCLK 1 P	FMC MGTCLK 1 P
GBTCLK1_M2C_N	B21	FMC MGTCLK 1 N	FMC MGTCLK 1 N
DP0_C2M_P	C2	MGT 116 1 TX P	MGT 116 1 TX P
DP0_C2M_N	C3	MGT 116 1 TX N	MGT 116 1 TX N
DP0_M2C_P	C6	MGT 116 1 RX P	MGT 116 1 RX P
DP0_M2C_N	C7	MGT 116 1 RX N	MGT 116 1 RX N
DP1_C2M_P	A22	MGT 116 3 TX P	MGT 116 3 TX P
DP1_C2M_N	A23	MGT 116 3 TX N	MGT 116 3 TX N
DP1_M2C_P	A2	MGT 116 3 RX P	MGT 116 3 RX P
DP1_M2C_N	A3	MGT 116 3 RX N	MGT 116 3 RX N
DP2_C2M_P	A26	MGT 116 2 TX P	MGT 116 2 TX P
DP2_C2M_N	A27	MGT 116 2 TX N	MGT 116 2 TX N
DP2_M2C_P	A6	MGT 116 2 RX P	MGT 116 2 RX P
DP2_M2C_N	A7	MGT 116 2 RX N	MGT 116 2 RX N
DP3_C2M_P	A30	MGT 116 0 TX P	MGT 116 0 TX P
DP3_C2M_N	A31	MGT 116 0 TX N	MGT 116 0 TX N
DP3_M2C_P	A10	MGT 116 0 RX P	MGT 116 0 RX P
DP3_M2C_N	A11	MGT 116 0 RX N	MGT 116 0 RX N
DP4_C2M_P	A34	MGT 115 2 TX P	MGT 115 2 TX P
DP4_C2M_N	A35	MGT 115 2 TX N	MGT 115 2 TX N
DP4_M2C_P	A14	MGT 115 2 RX P	MGT 115 2 RX P
DP4_M2C_N	A15	MGT 115 2 RX N	MGT 115 2 RX N
DP5_C2M_P	A38	MGT 115 0 TX P	MGT 115 0 TX P
DP5_C2M_N	A39	MGT 115 0 TX N	MGT 115 0 TX N
DP5_M2C_P	A18	MGT 115 0 RX P	MGT 115 0 RX P
DP5_M2C_N	A19	MGT 115 0 RX N	MGT 115 0 RX N
DP6_C2M_P	B36	MGT 115 1 TX P	MGT 115 1 TX P
DP6_C2M_N	B37	MGT 115 1 TX N	MGT 115 1 TX N
DP6_M2C_P	B16	MGT 115 1 RX P	MGT 115 1 RX P
DP6_M2C_N	B17	MGT 115 1 RX N	MGT 115 1 RX N
DP7_C2M_P	B32	MGT 115 3 TX P	MGT 115 3 TX P
DP7_C2M_N	B33	MGT 115 3 TX N	MGT 115 3 TX N
DP7_M2C_P	B12	MGT 115 3 RX P	MGT 115 3 RX P
DP7_M2C_N	B13	MGT 115 3 RX N	MGT 115 3 RX N
DP8_C2M_P	B28	FMC MGT 8 TX P	FMC MGT 8 TX P
DP8_C2M_N	B29	FMC MGT 8 TX N	FMC MGT 8 TX N
DP8_M2C_P	B8	FMC MGT 8 RX P	FMC MGT 8 RX P
DP8_M2C_N	B9	FMC MGT 8 RX N	FMC MGT 8 RX N
DP9_C2M_P	B24	FMC MGT 9 TX P	FMC MGT 9 TX P
DP9_C2M_N	B25	FMC MGT 9 TX N	FMC MGT 9 TX N
DP9_M2C_P	B4	FMC MGT 9 RX P	FMC MGT 9 RX P
DP9_M2C_N	B5	FMC MGT 9 RX N	FMC MGT 9 RX N

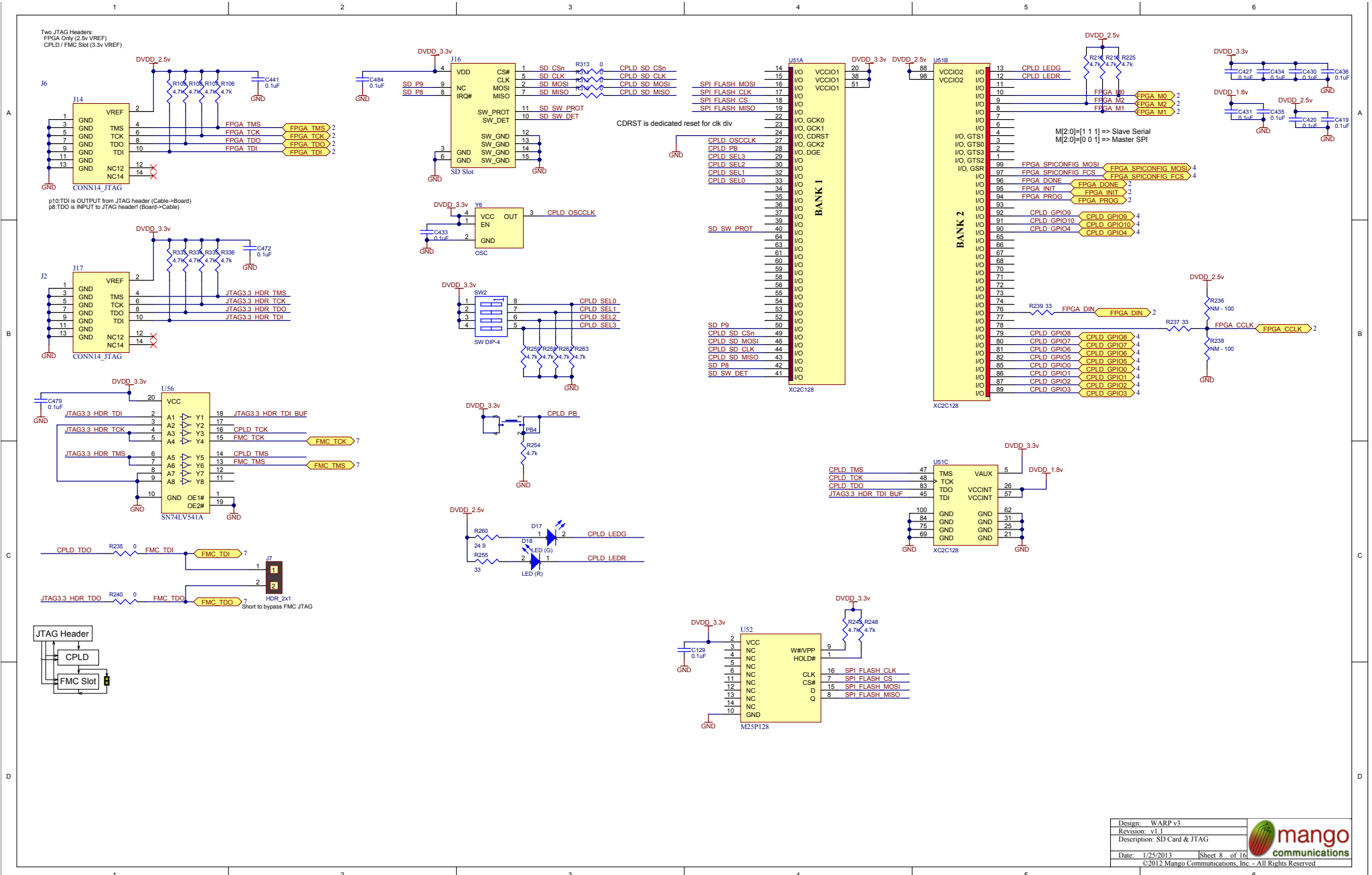
FMC HPC Clocks & Misc			
CLK0_M2C_P	C30	FMC I2C SCL 3.3v	FMC I2C SCL 3.3v
CLK0_M2C_N	C31	FMC I2C SDA 3.3v	FMC I2C SDA 3.3v
CLK1_M2C_P	H4	FMC CLK0 M2C P	FMC CLK0 M2C P
CLK1_M2C_N	H5	FMC CLK0 M2C N	FMC CLK0 M2C N
CLK2_BIDIR_P	G2	FMC CLK1 M2C P	FMC CLK1 M2C P
CLK2_BIDIR_N	G3	FMC CLK1 M2C N	FMC CLK1 M2C N
CLK3_BIDIR_P	J2	RF CLK FMC C2M P	RF CLK FMC C2M P
CLK3_BIDIR_N	J3	RF CLK FMC C2M N	RF CLK FMC C2M N
TCK	D29	FMC TCK	FMC TCK
TDI	D30	FMC TDI	FMC TDI
TMS	D33	FMC TMS	FMC TMS
TRST_L	D34	FMC TRST	FMC TRST
PRNST_M2C_N	H2	FMC PRNST M2C	FMC PRNST M2C
GA0	C34	FMC GA0	FMC GA0
GA1	D35	FMC GA1	FMC GA1



FMC HPC Power requirements:  
Carrier-to-Module Supplies:  
12.0v @ 1a (2 pins)  
3.3v @ 3A (4 pins)  
3.3v Aux @ 20mA (1 pin)  
VADJ [0,3,5v] @ 4A (4 pins)

Module-to-Carrier Supplies:  
VREF\_B\_M2C @ 1mA (1 pin)  
VREF\_A\_M2C @ 1mA (1 pin)  
VIO\_B\_M2C [0,VADJ] @ 1.15A (2 pins)







A

B

C

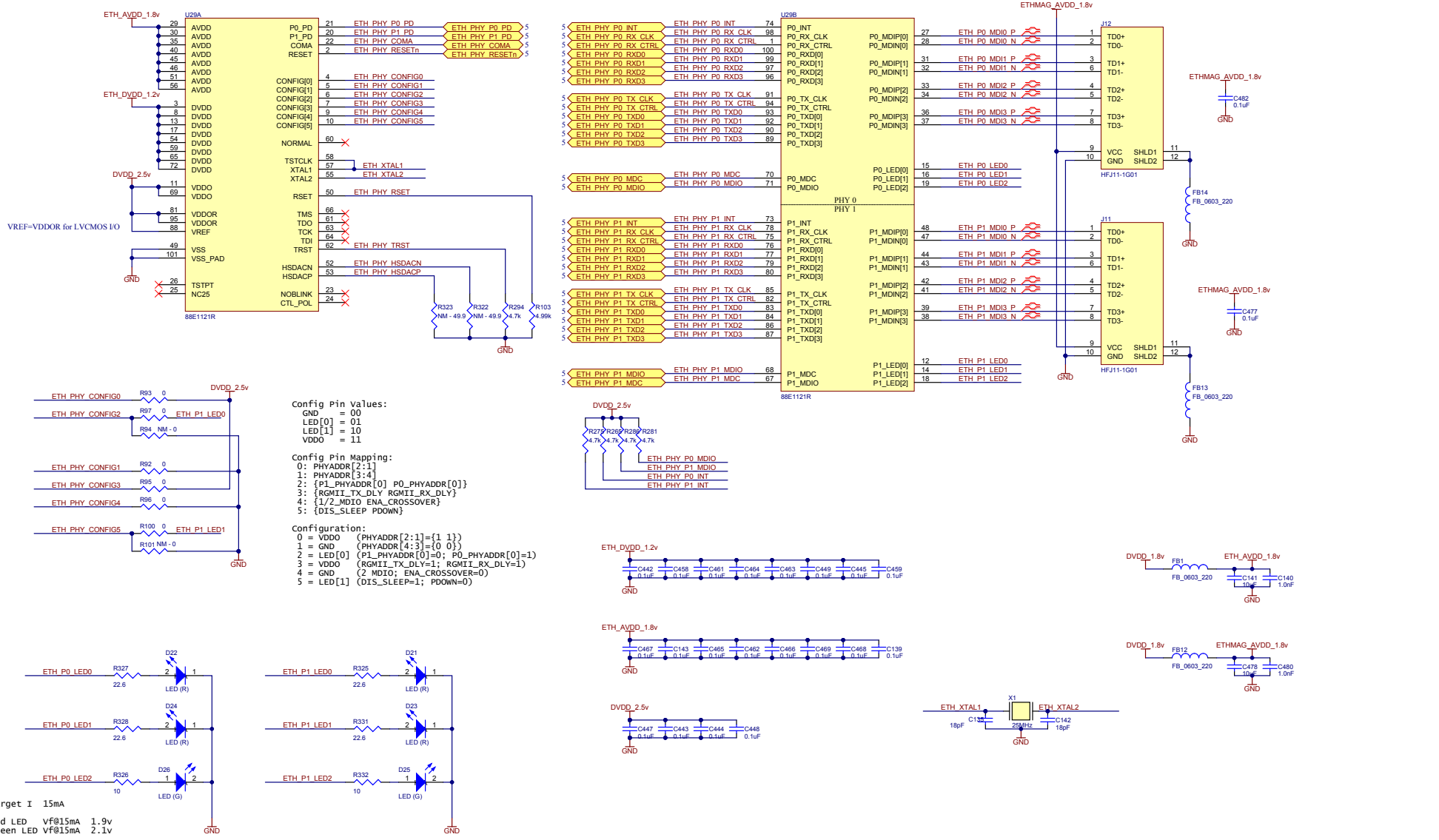
D

A

B

C

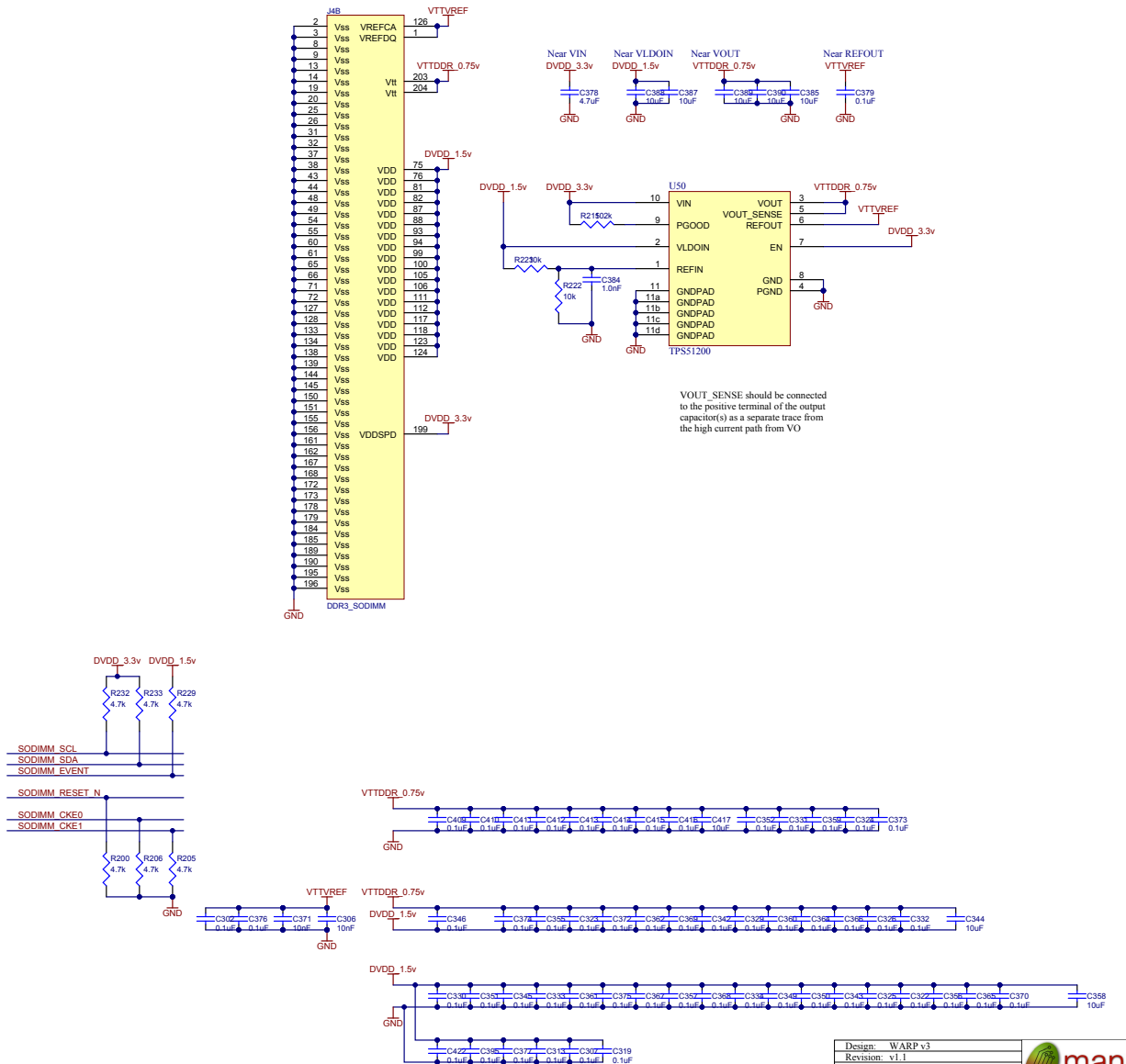
D



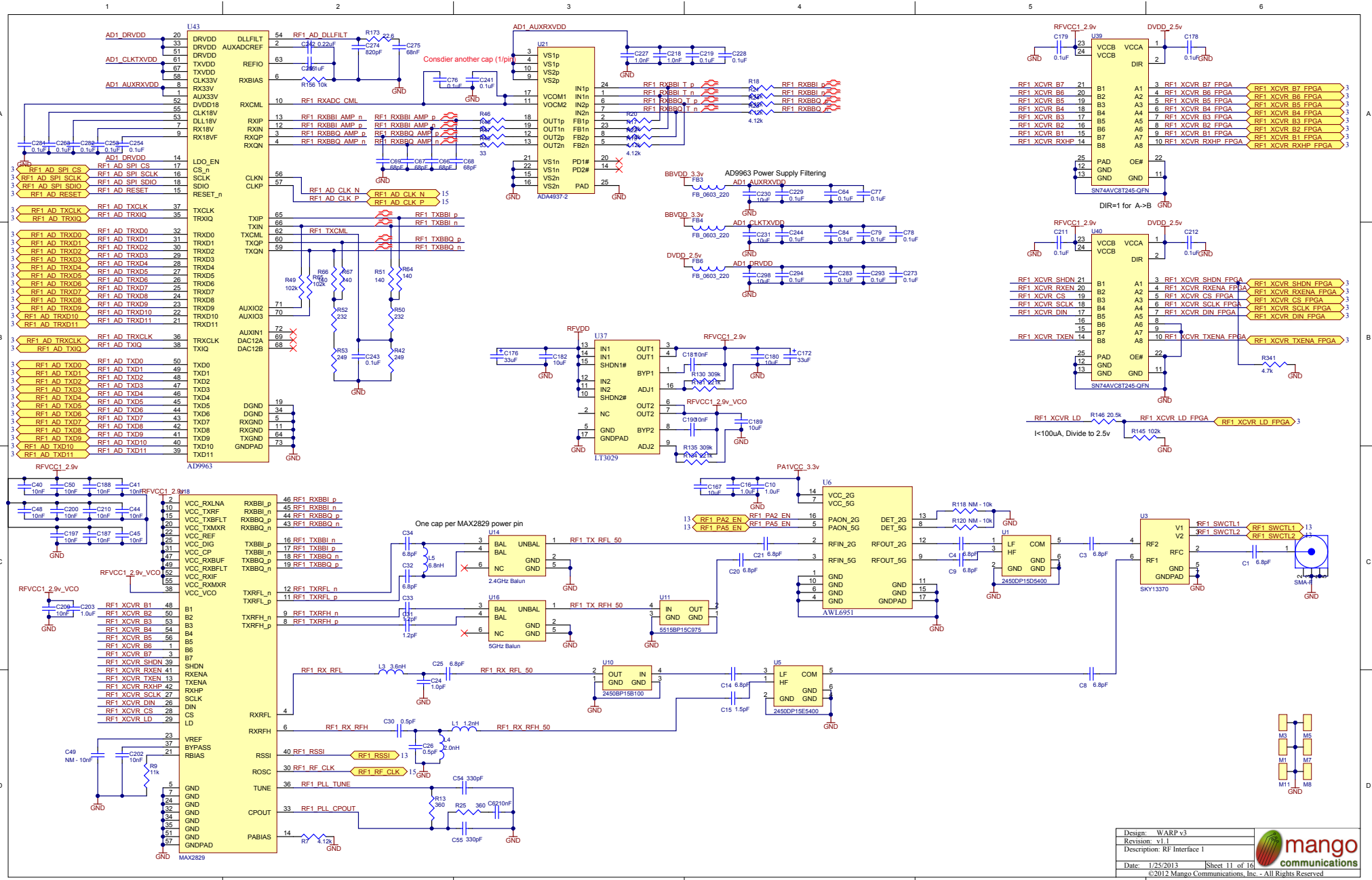
Target I 15mA  
 Red LED Vf@15mA 1.9V  
 Green LED Vf@15mA 2.1V  
 PHY LED pins V@15mA 0.27  
 (per 1B1S model TTLBID112\_LED0\_V25)

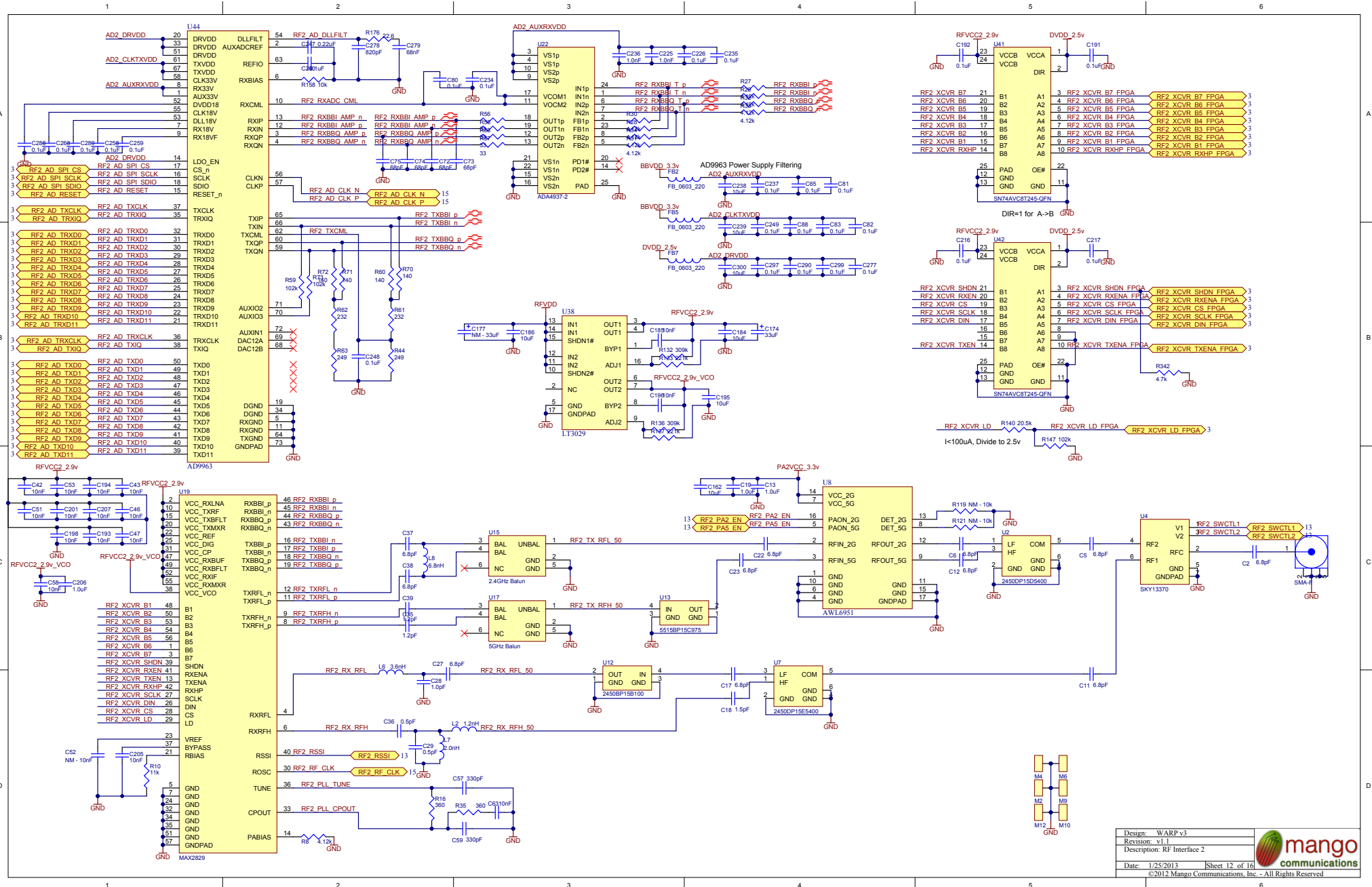
SODIMM wired to support A[15:0], ODT[1:0], CS\_n[1:0]; up to 8GB dual rank  
 Micron Pins S[1:0]# = MIG Pins CS\_n[1:0]

SODIMM ADDR0		SODIMM ADDR1		SODIMM ADDR2		SODIMM ADDR3		SODIMM ADDR4		SODIMM ADDR5		SODIMM ADDR6		SODIMM ADDR7		SODIMM ADDR8		SODIMM ADDR9		SODIMM ADDR10		SODIMM ADDR11		SODIMM ADDR12		SODIMM ADDR13		SODIMM ADDR14		SODIMM ADDR15	
98	A0	97	A1	96	A2	95	A3	94	A4	93	A5	92	A6	91	A7	90	A8	89	A9	88	A10/AP	87	A11	86	A12/BC	85	A13	84	A14	83	A15
109	BA0	108	BA1	107	BA2	106	BA3	105	BA4	104	BA5	103	BA6	102	BA7	101	BA8	100	BA9	99	BA10	98	BA11	97	BA12	96	BA13	95	BA14	94	BA15
103	CK0n	102	CK0p	101	CK1n	100	CK1p	99	CK2n	98	CK2p	97	CK3n	96	CK3p	95	CK4n	94	CK4p	93	CK5n	92	CK5p	91	CK6n	90	CK6p	89	CK7n	88	CK7p
10	DQS0n	12	DQS0p	27	DQS1n	29	DQS1p	45	DQS2n	47	DQS2p	64	DQS3n	66	DQS3p	82	DQS4n	84	DQS4p	100	DQS5n	102	DQS5p	117	DQS6n	119	DQS6p	134	DQS7n	136	DQS7p
115	CAS	110	RAS	113	WE	30	RESET_n	116	ODT0	120	ODT1	198	EVENT	114	CS0	121	CS1	197	SA0	201	SA1	202	SCL	200	SDA	125	NC122	122	77	NC77	
5	DM0	6	DM1	7	DM2	8	DM3	9	DM4	10	DM5	11	DM6	12	DM7	13	DM8	14	DM9	15	DM10	16	DM11	17	DM12	18	DM13	19	DM14	20	DM15



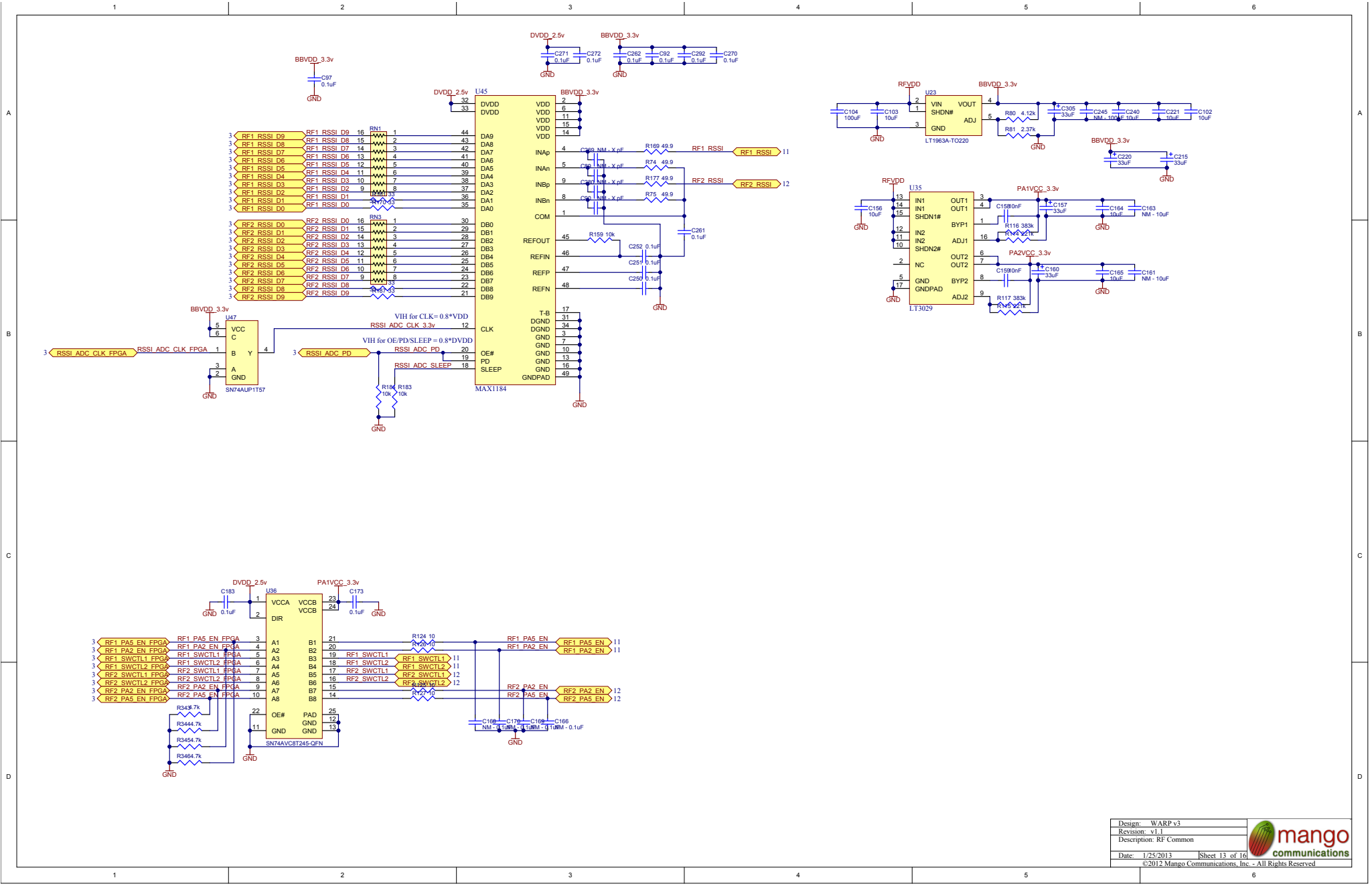
VOUT\_SENSE should be connected to the positive terminal of the output capacitor(s) as a separate trace from the high current path from VO

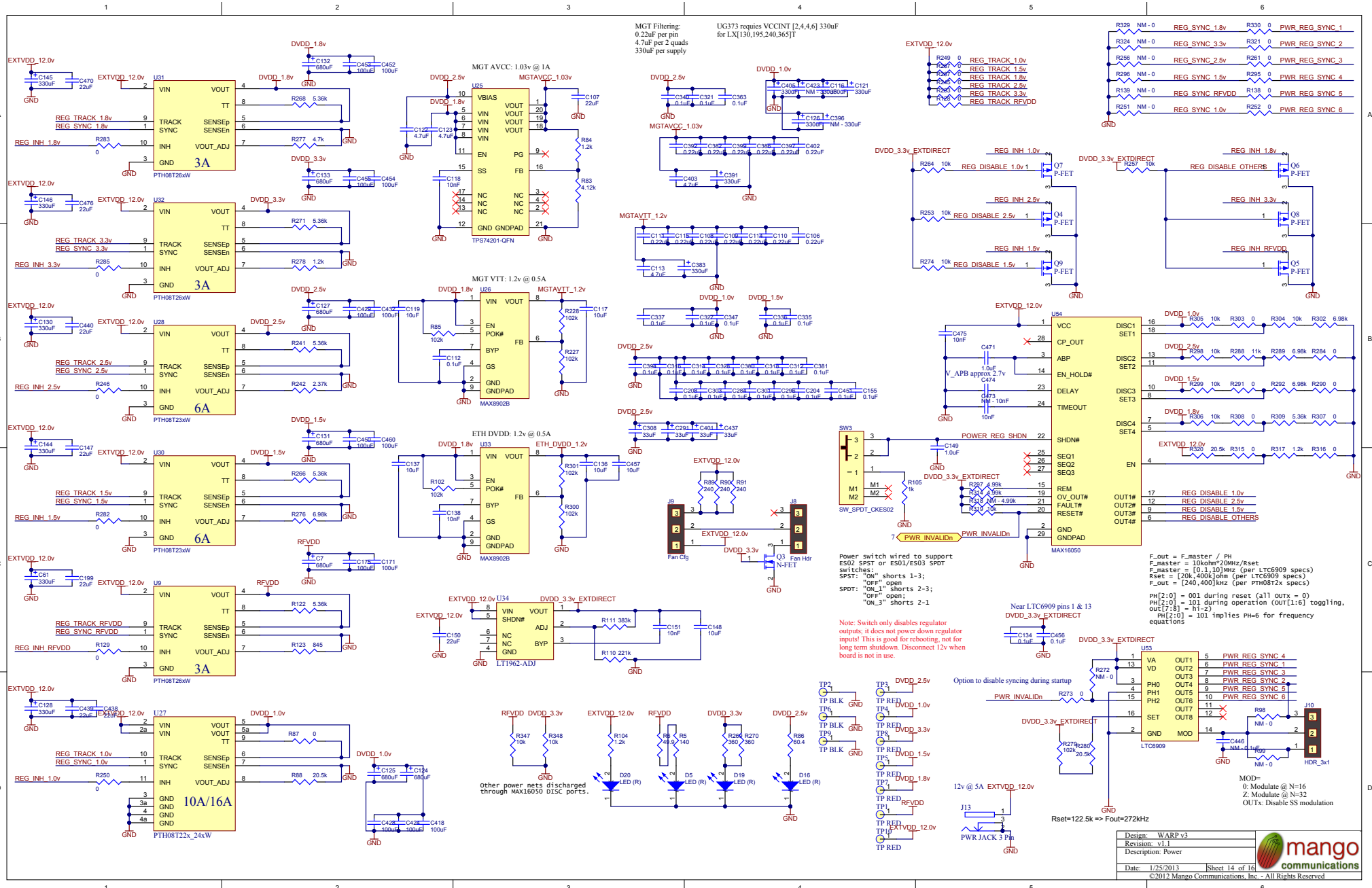




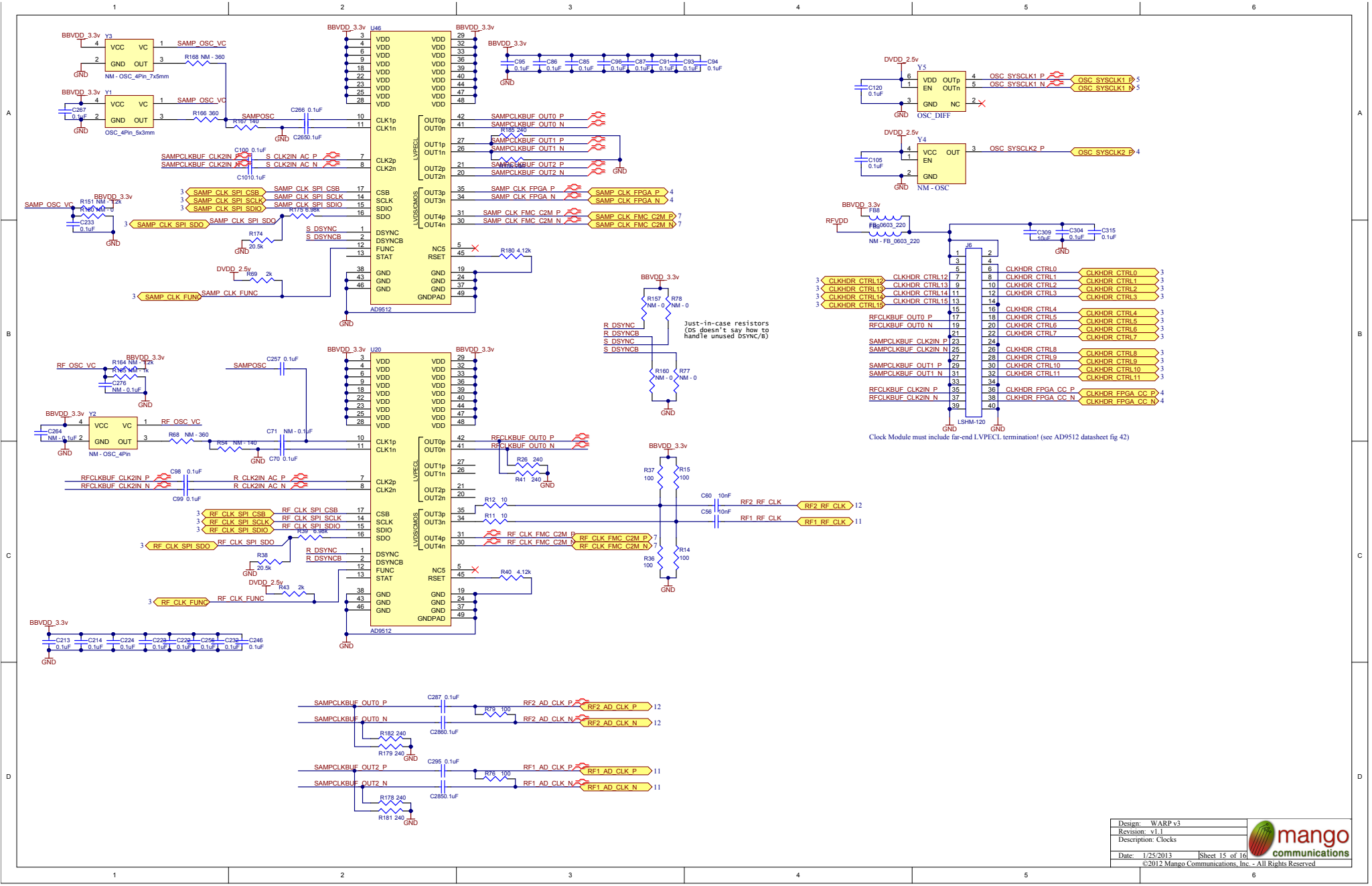
Design:	WARP v3
Revision:	v1.1
Description:	RF Interface 2
Date:	1/25/2013
Sheet 12 of 16	
Sheet 12 of 16	
©2012 Mango Communications, Inc. - All Rights Reserved	







Design: WARP v3
Revision: v1.1
Description: Power
Date: 1/25/2013
Sheet 14 of 16
©2012 Mango Communications, Inc. - All Rights Reserved



Just-in-case resistors  
(DS doesn't say how to  
handle unused S5YNC/S6)

Clock Module must include far-end LVPECL termination! (see AD9512 datasheet fig 42)

