WARPMAC

A Framework for Wireless Medium Access development on
Rice University's Wireless Open-Access Research Platform

Christopher Hunter, Joseph Camp, Patrick Murphy, Ashu Sabharwal, Chris Dick

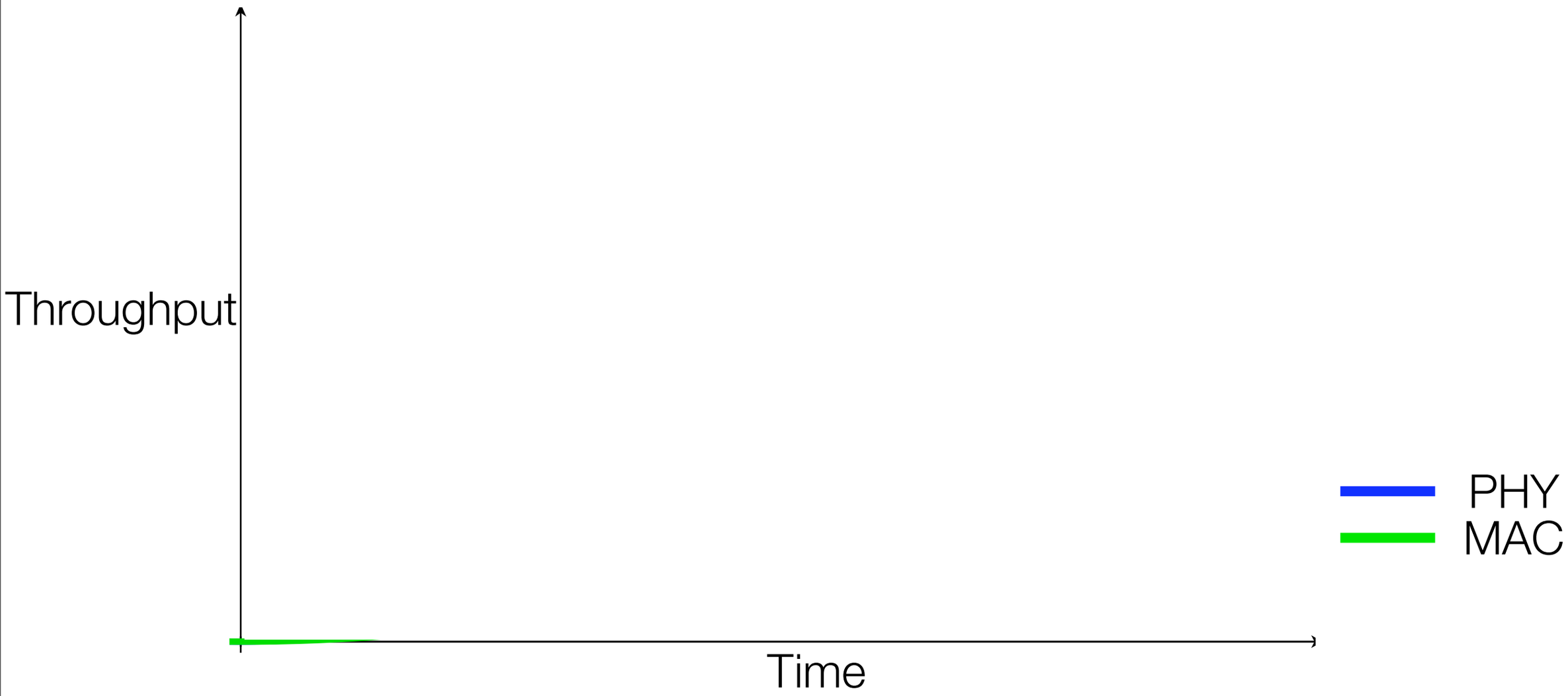
RICE

WARP

WIRELESS OPEN-ACCESS
RESEARCH PLATFORM

XILINX®

Advancements in 802.11



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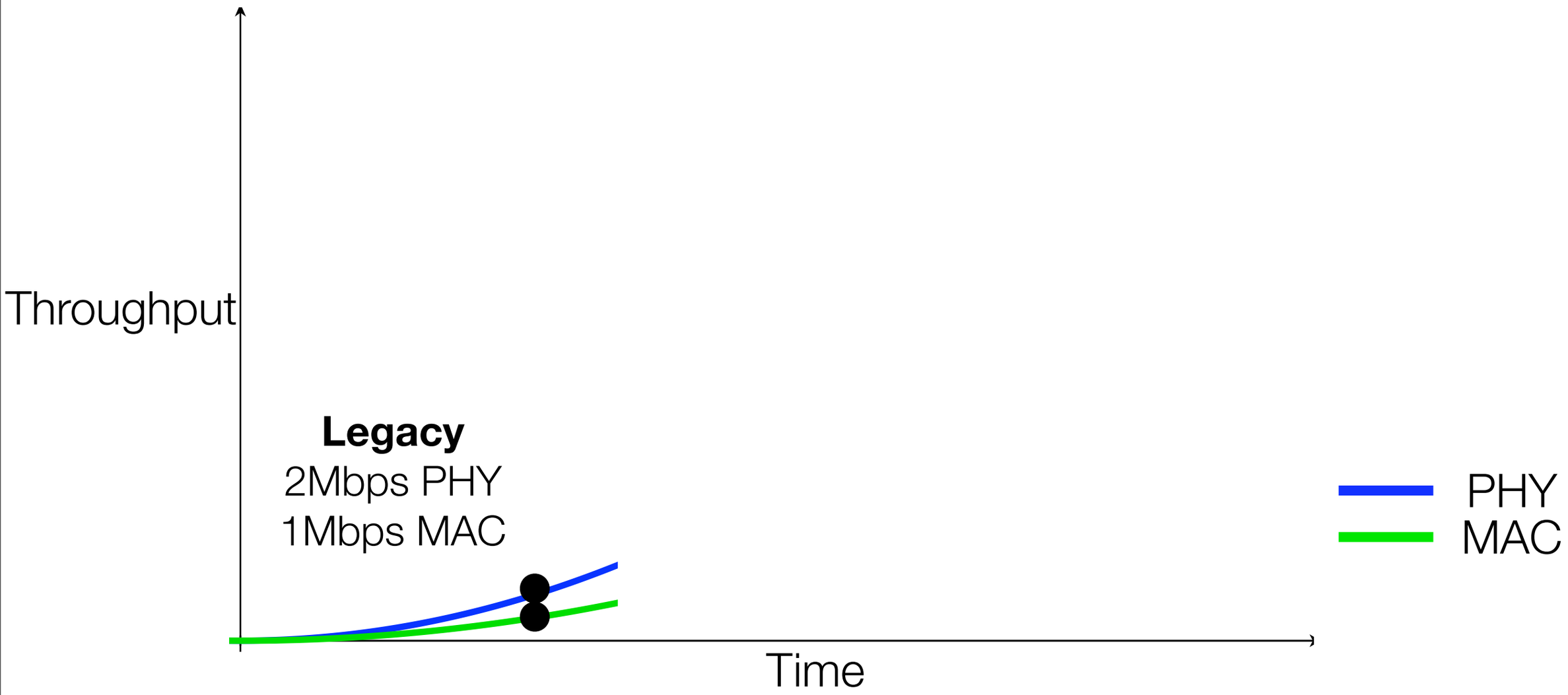

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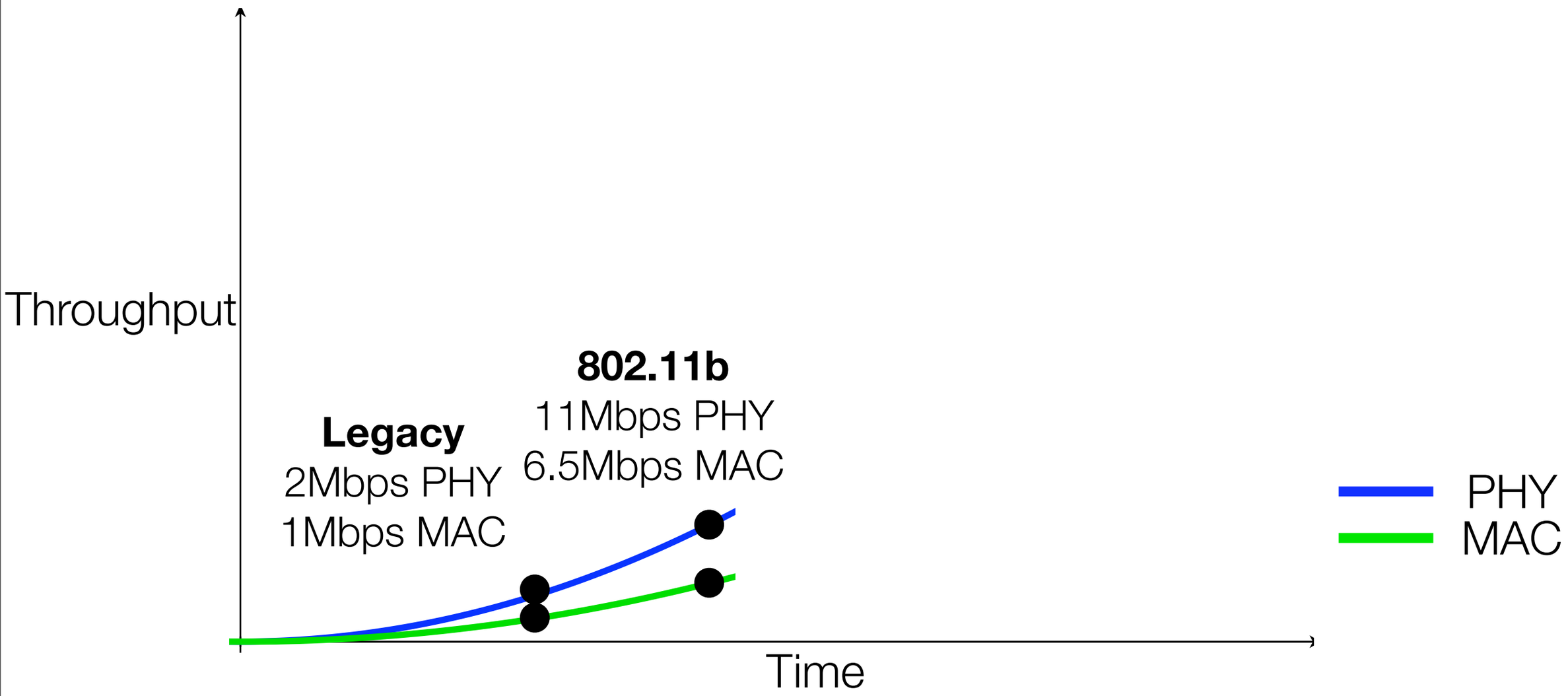

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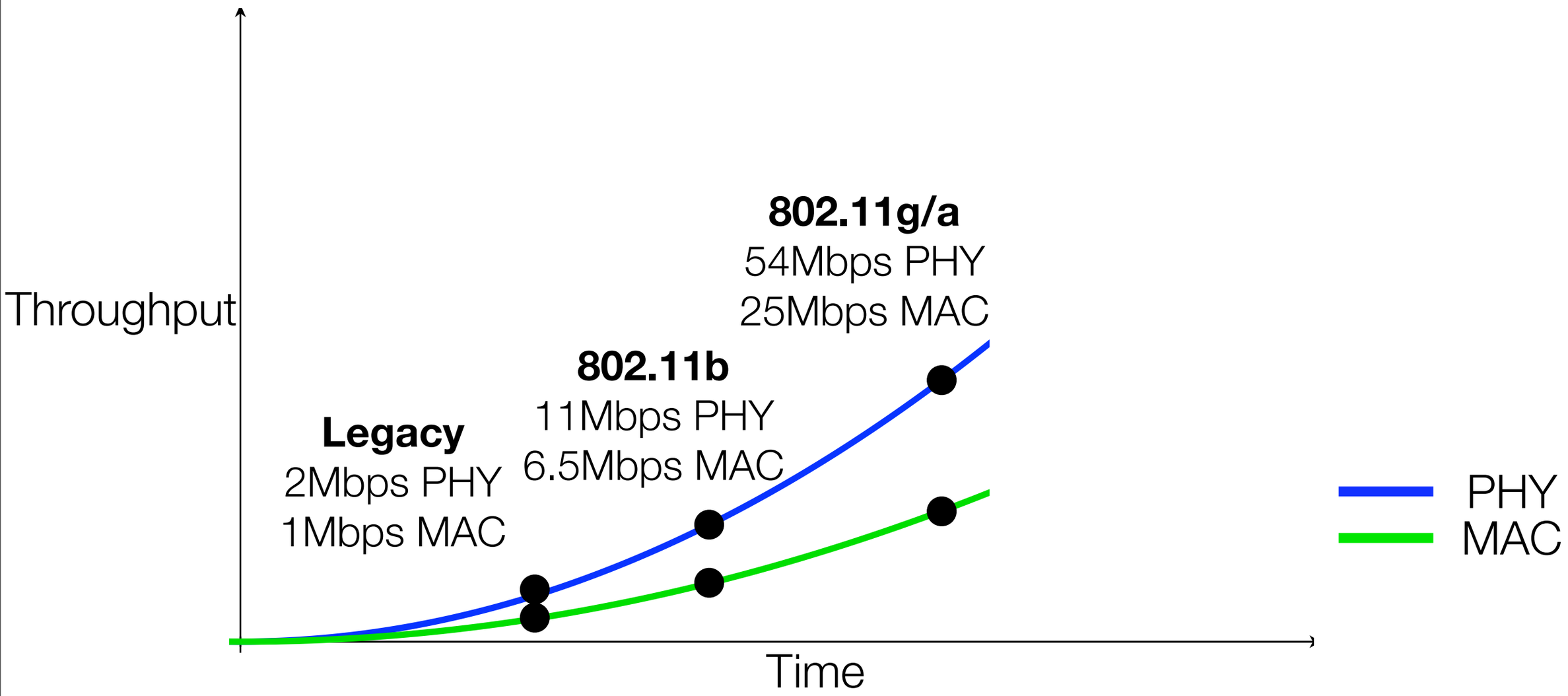

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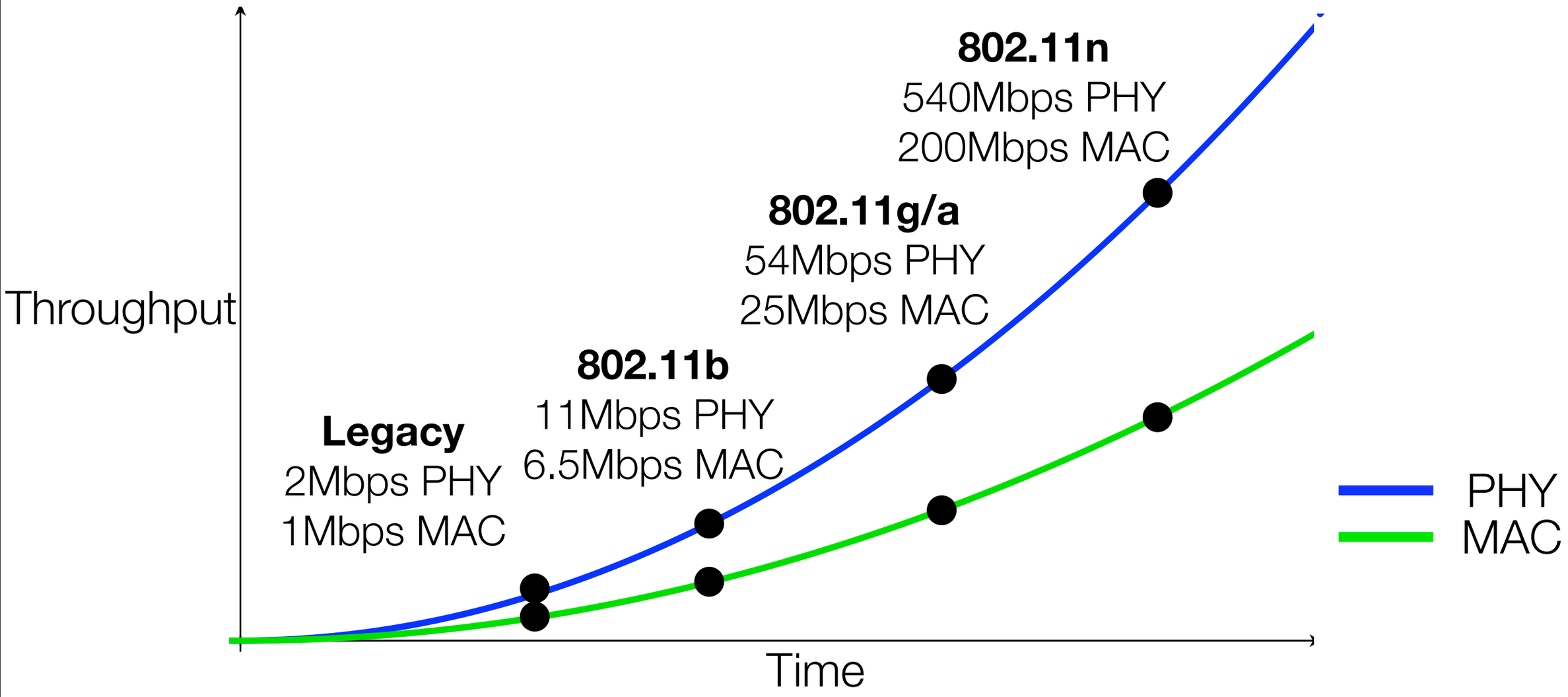

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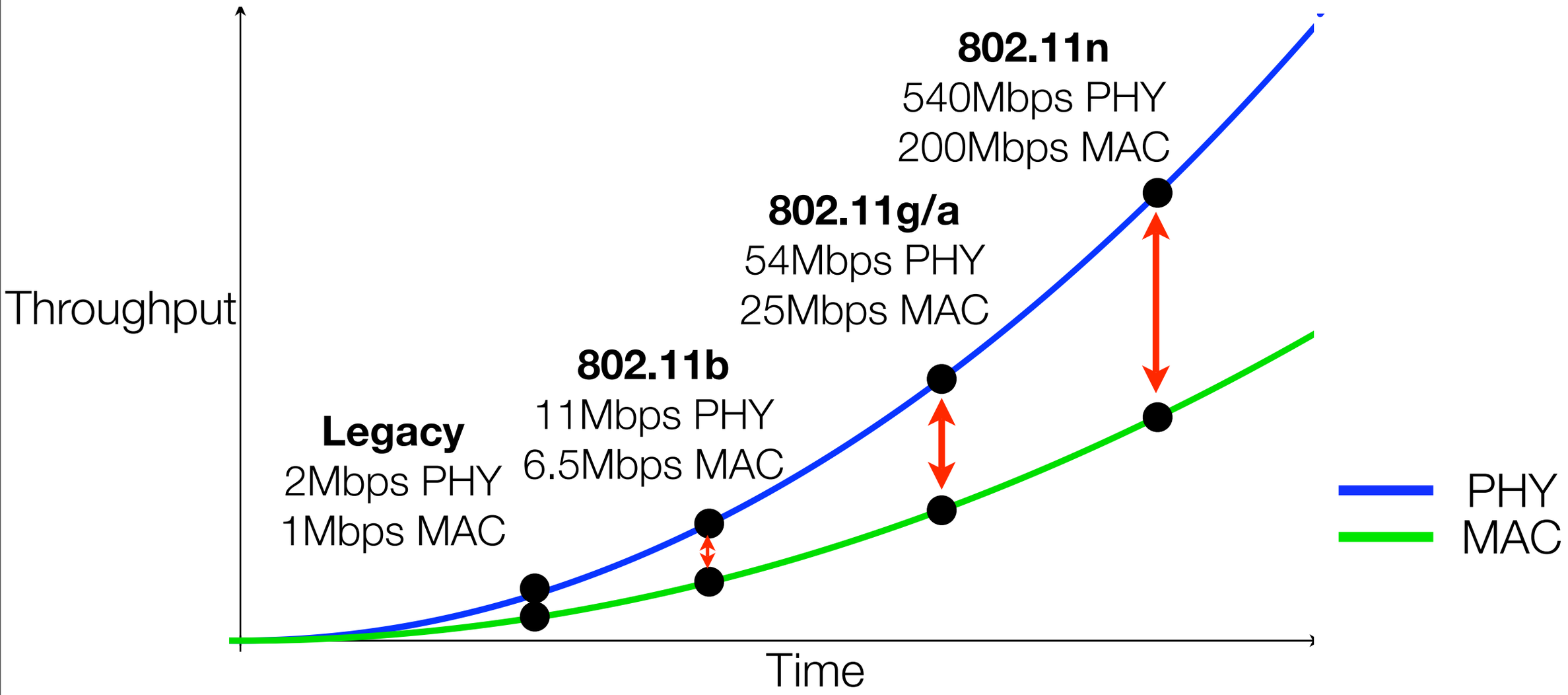

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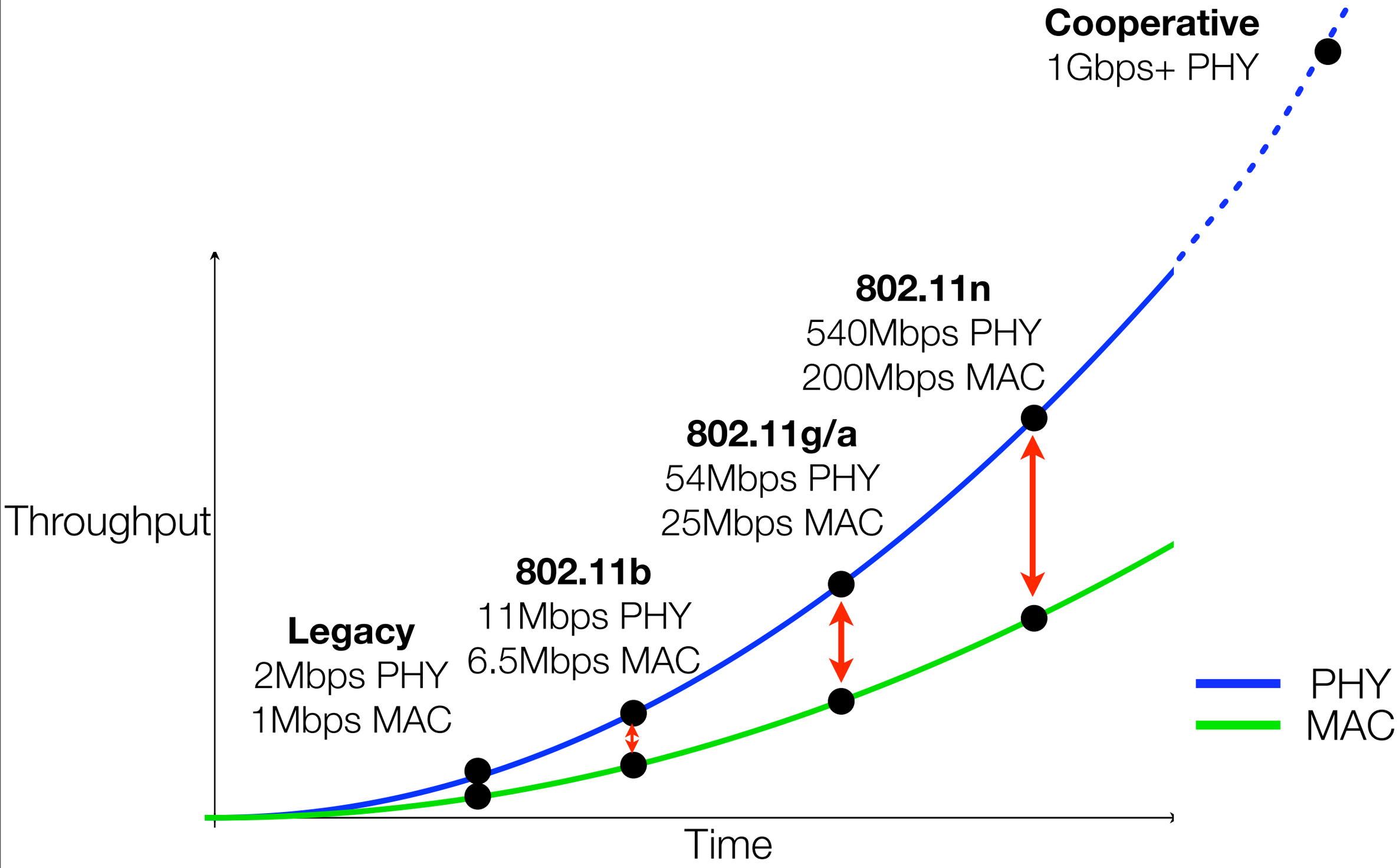


State of the Art

Many novel MACs proposed in literature with simulation results from NS-2

- NS-2 is a critical first-pass test
- Conversion from algorithm to C-code is tractable

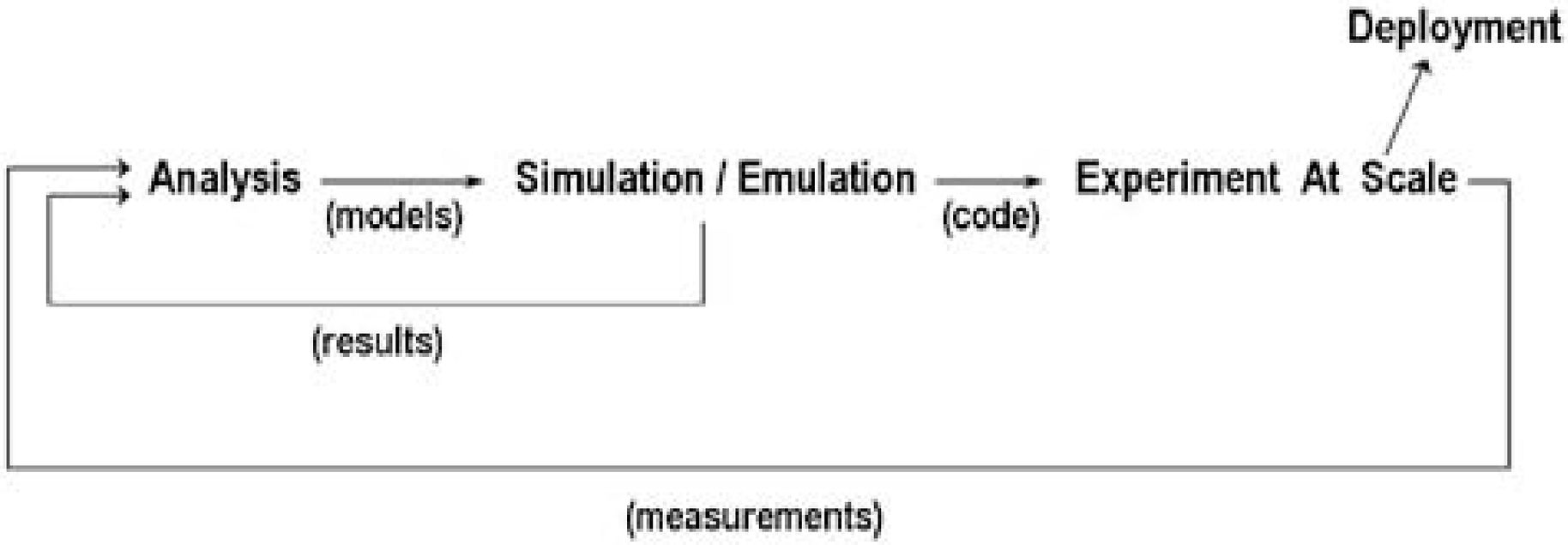
Limitations:

- Weak physical-layer models hurt robustness claims
- Better, sample-level, PHY model too slow for network time scales

State of the Art

Networking research community pushing for at-scale experiments

- GENI Project (http://www.geni.net/)



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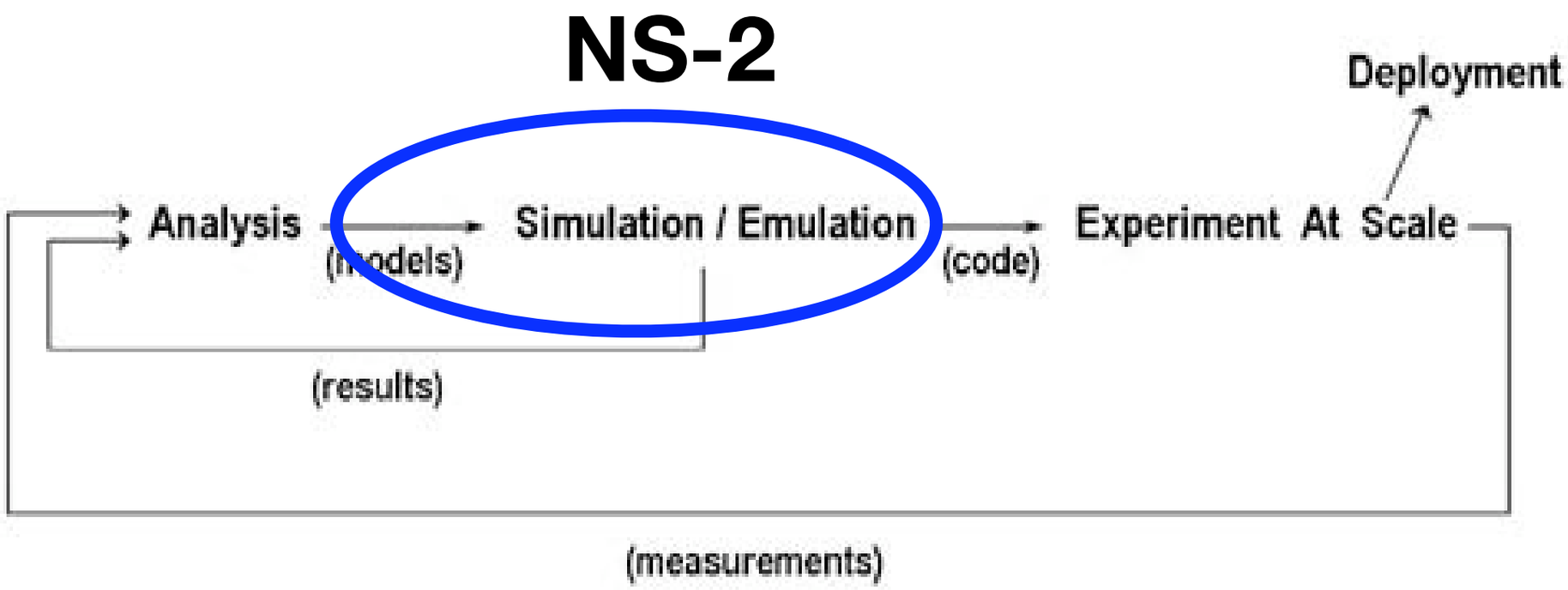

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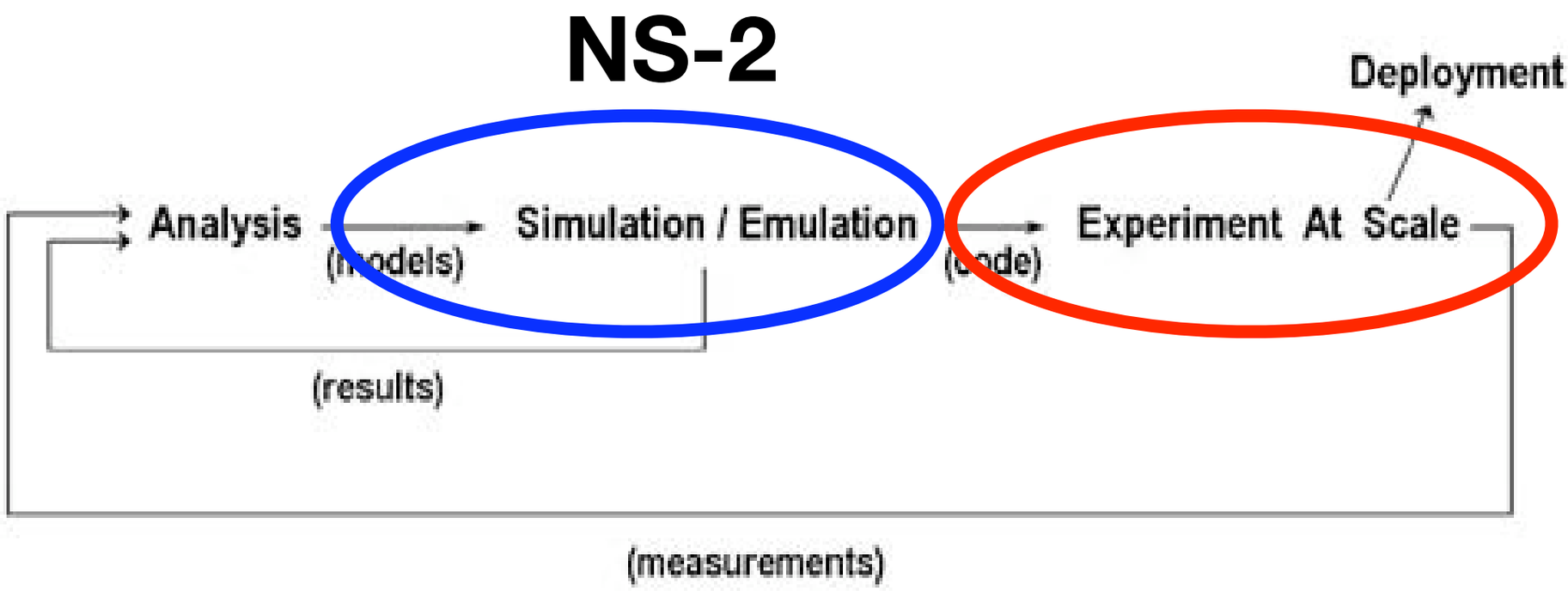


Need to put “paper” MACs on hardware

Implementing Novel MACs

Existing Approach: Overwrite existing MAC behavior in 802.11 devices

- SoftMAC Project - https://systems.cs.colorado.edu/projects/softmac
- Madwifi - http://madwifi.org/

Functionality

- Control packet contents and timing

Limitations

- No control over PHY
- Not sustainable.... at the mercy of chipset manufacturers

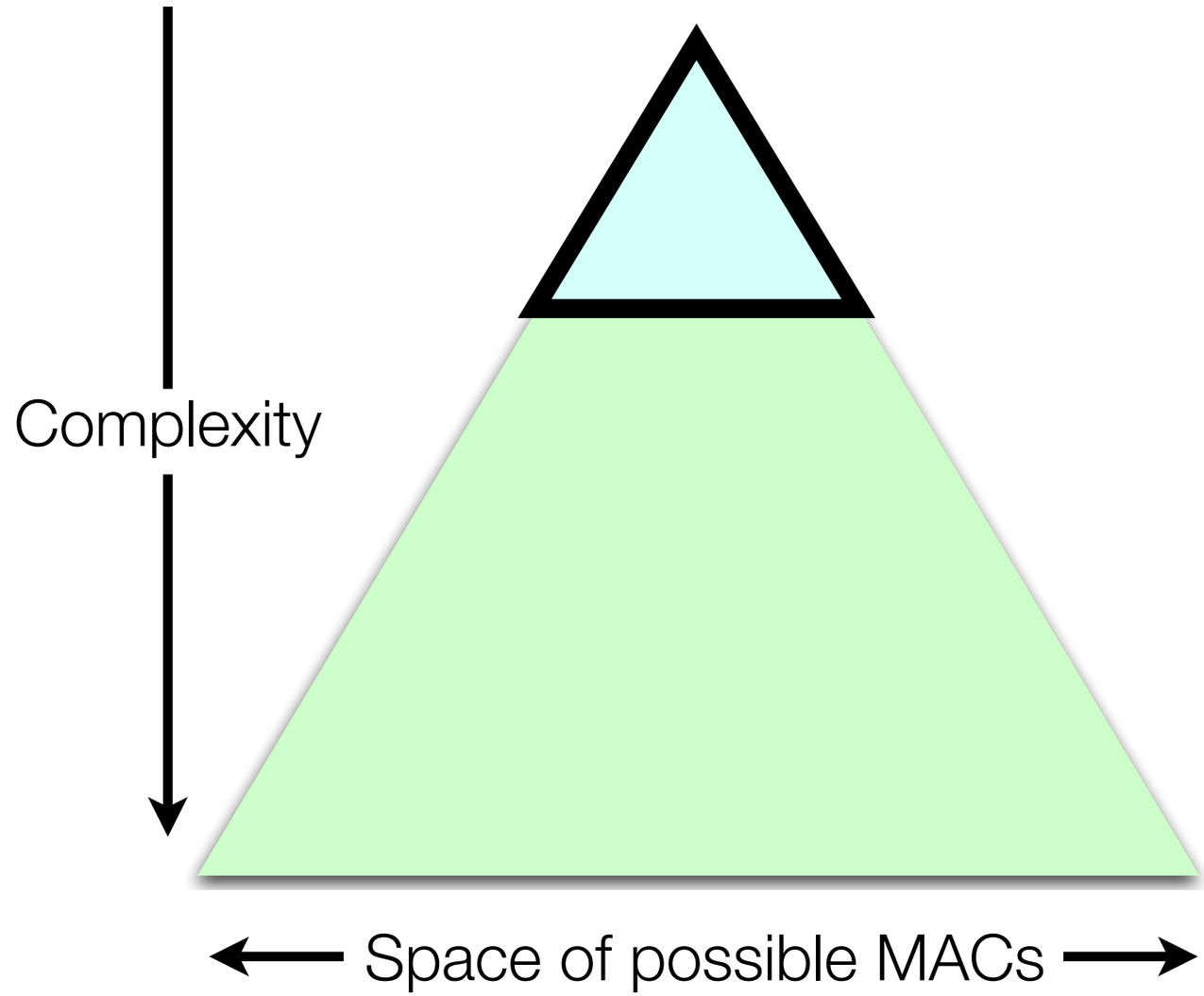
Rice's Approach

First Tier

- High-level, low breadth capabilities for derivatives of standard random-access protocols

- Opportunistic Auto Rate (OAR)
  (Sadeghi, Kanodia, Sabharwal, Knightly 2002)

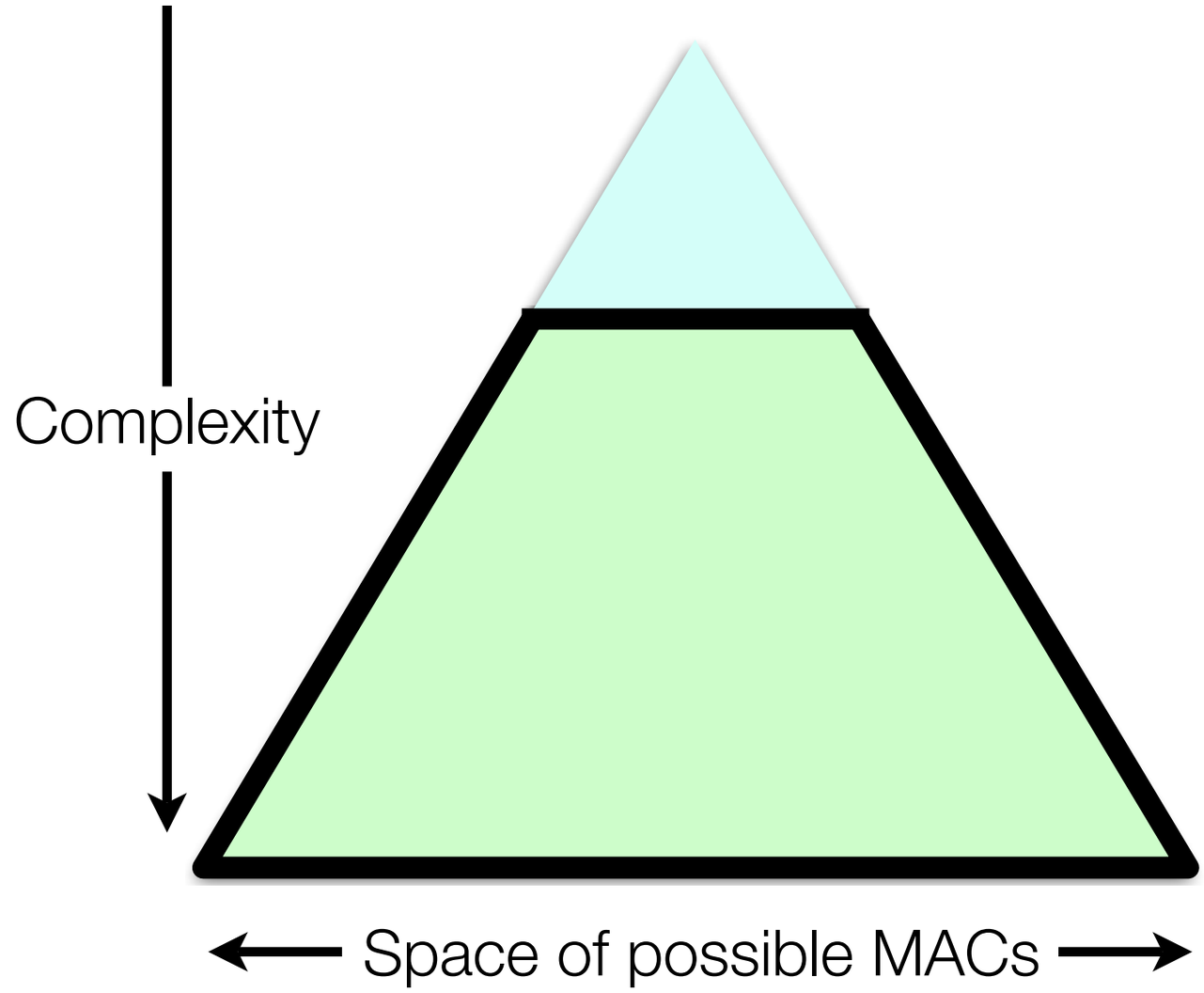
- Multichannel Opportunistic Auto Rate (MOAR)
  (Kanodia, Sabharwal, Knightly 2004)



Rice's Approach

Second Tier

- Low-level, high breadth capabilities for clean-slate MAC-PHY systems
  - scheduled access like WiMax
  - cooperative relays
  - future MACs for future PHYs



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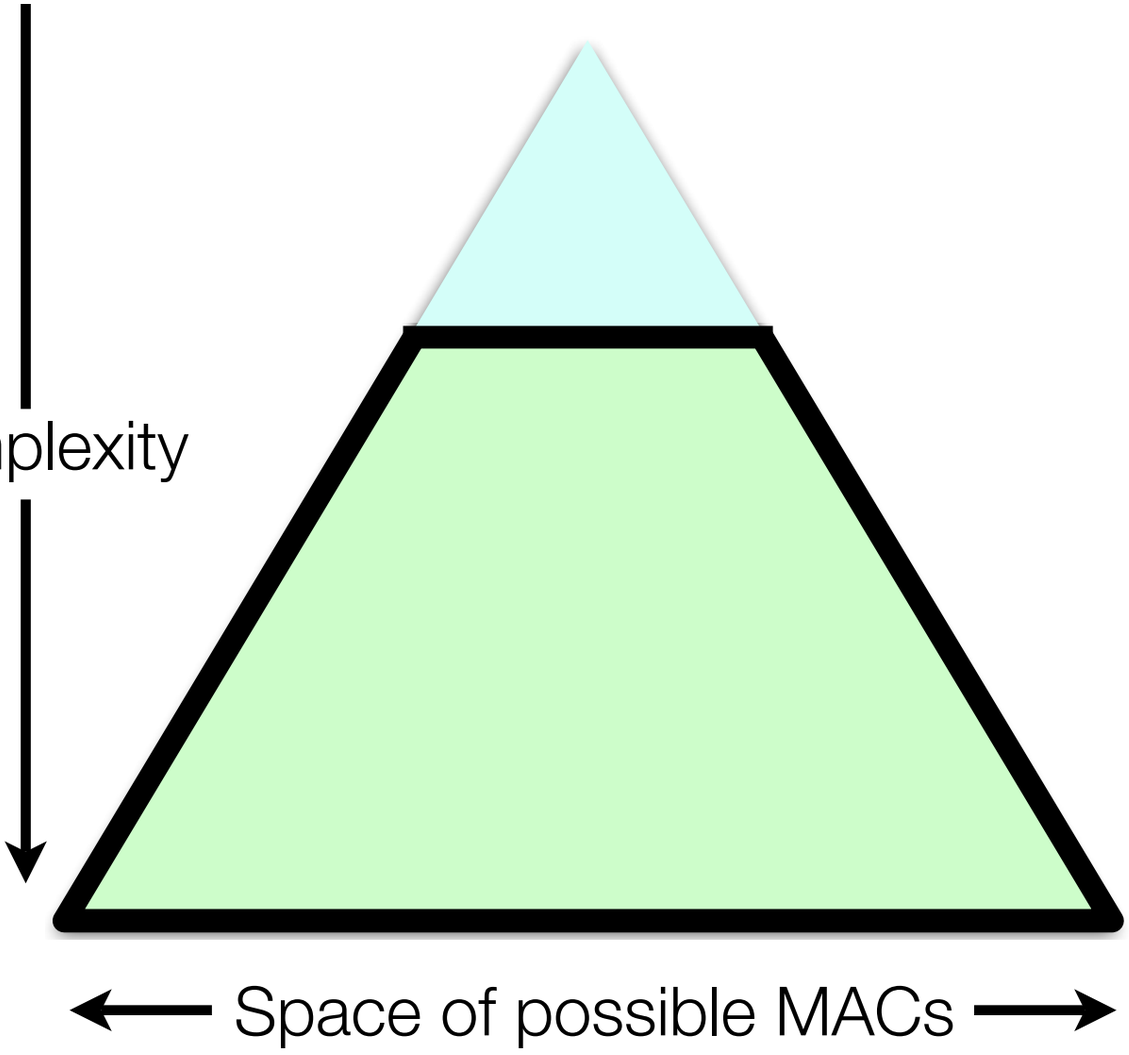

This organization leads naturally to WARPMAC

Overview of WARPMAC

- WARP Hardware - What's "under the hood"?
- Design Realization - What are the hardware requirements of a basic MAC?
- WARPMAC - What tools do we provide for MAC development?
- Examples - Current MACs at Rice

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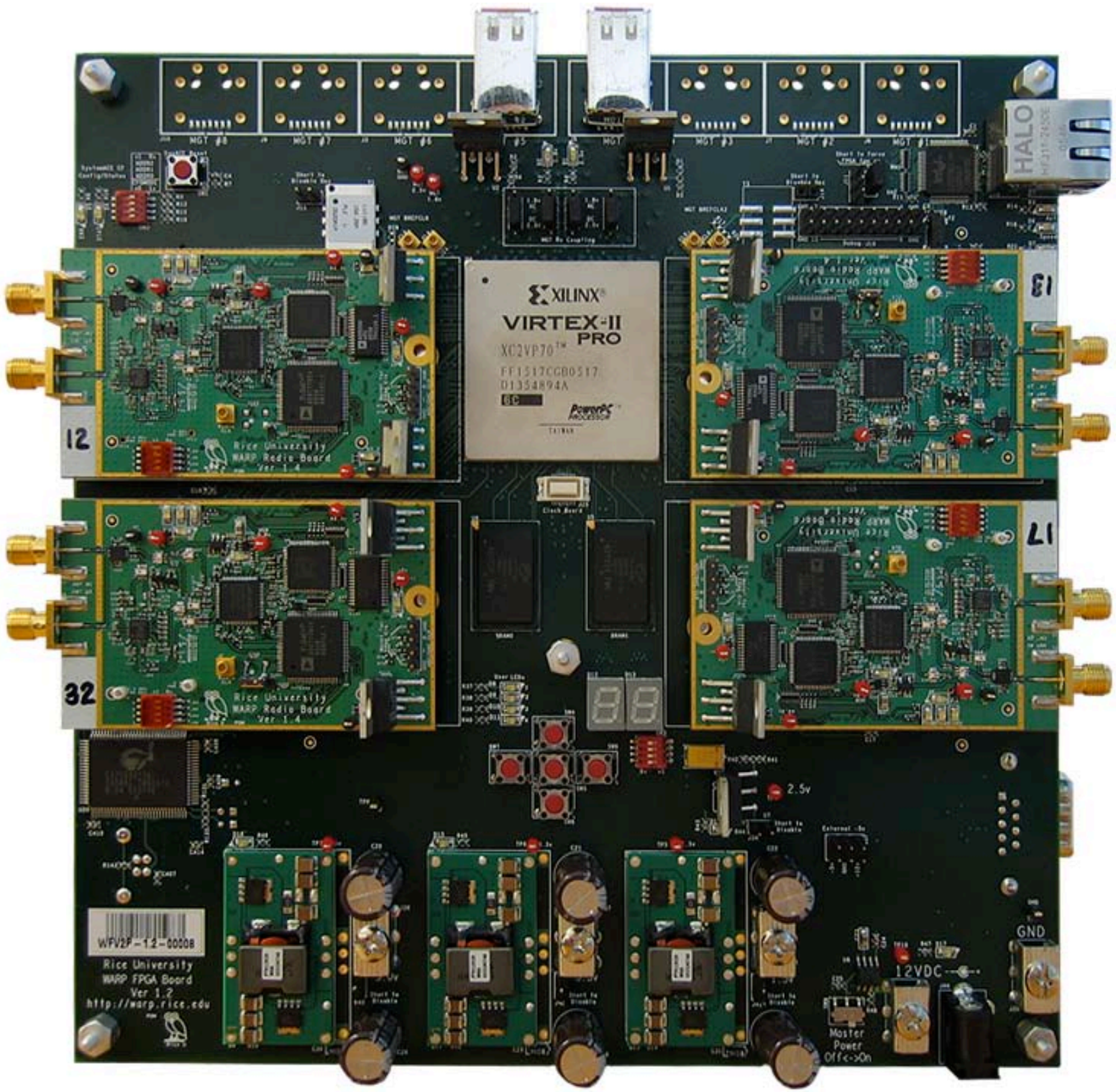
WARP - The Base Hardware



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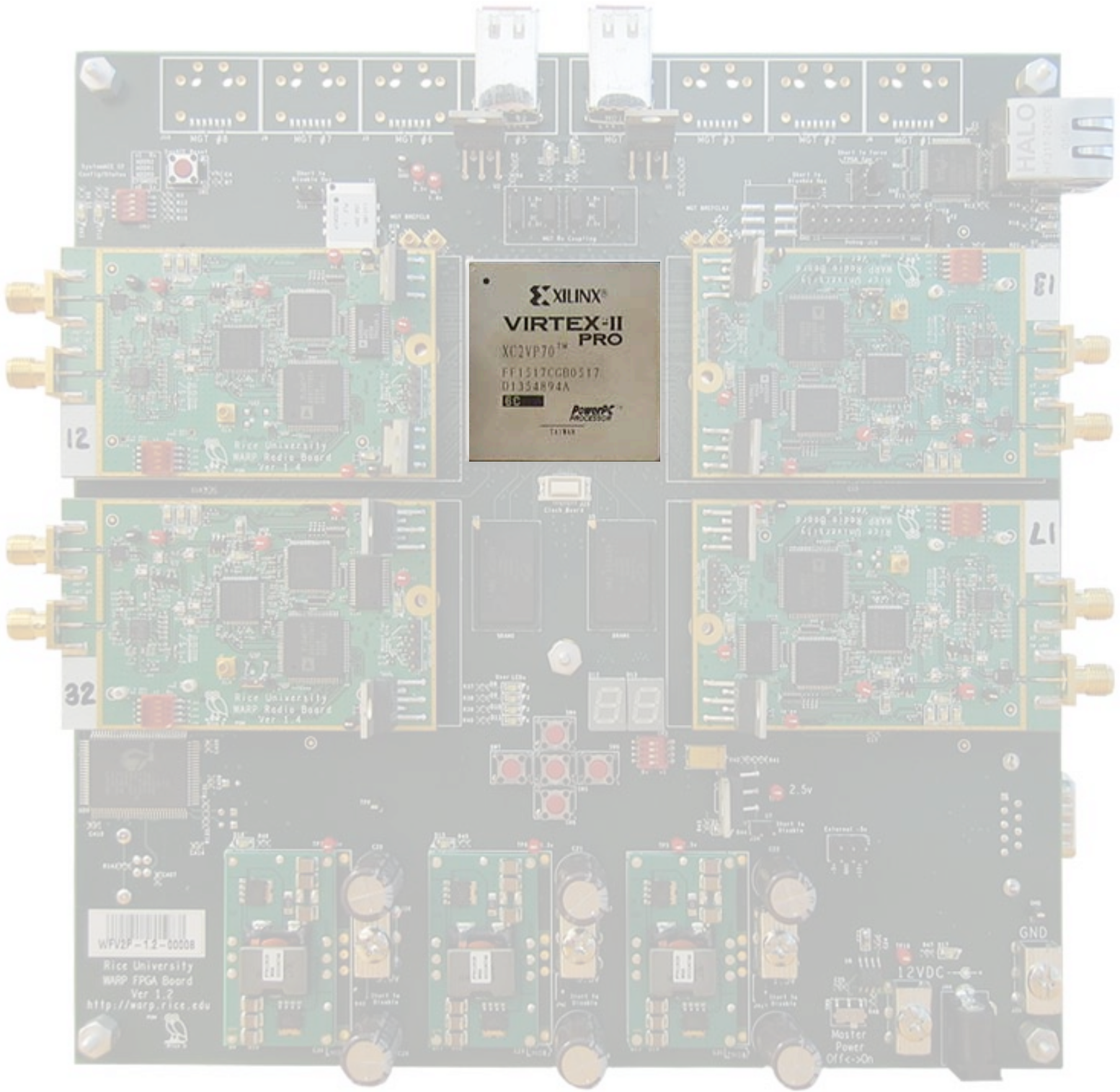
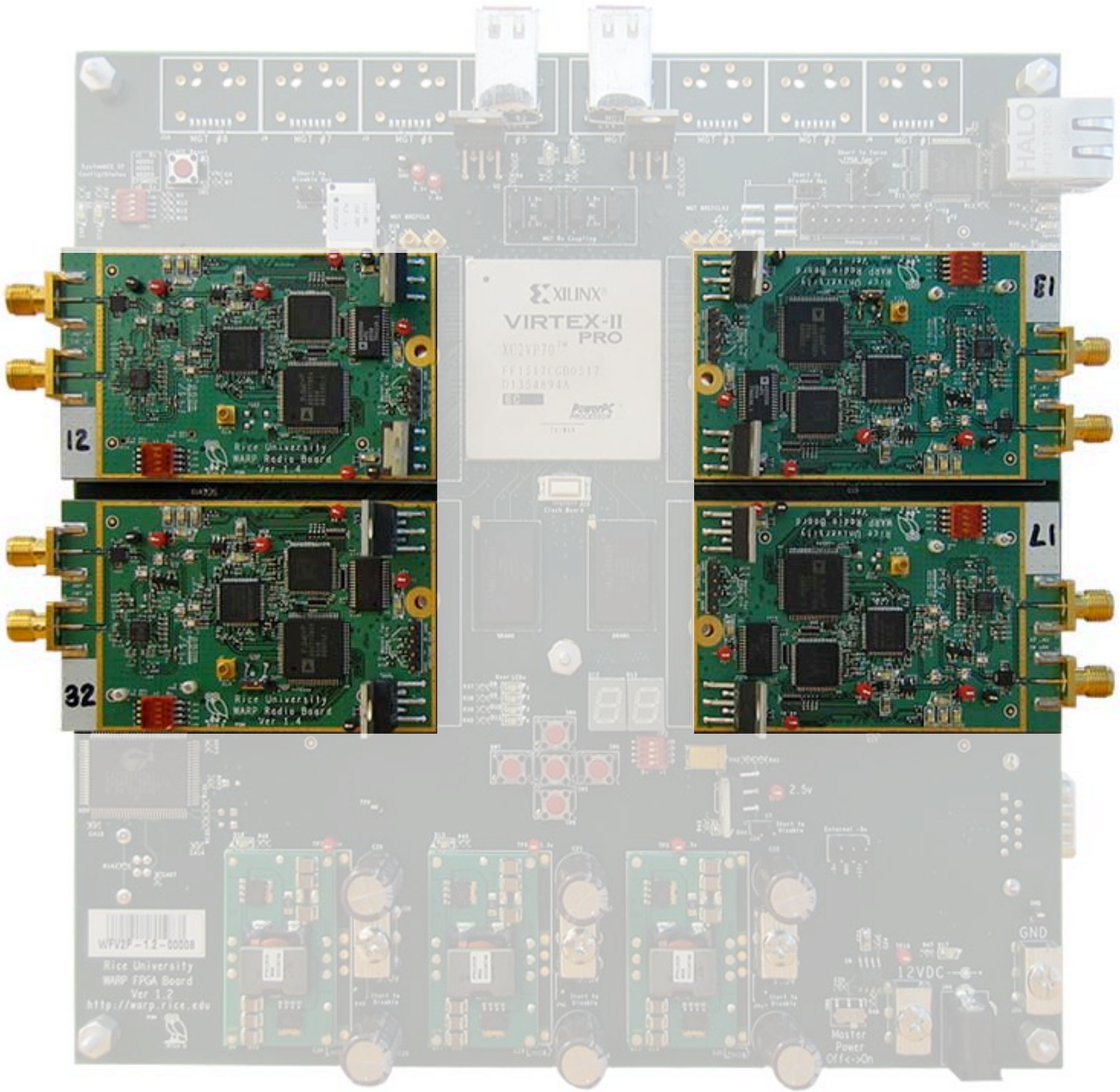


Xilinx Virtex-II Pro (XC2VP70)

- 2 PowerPC Processors
- 328 multipliers for DSP
- 66,000+ 4-input LUTs
- 66,000+ flip-flops

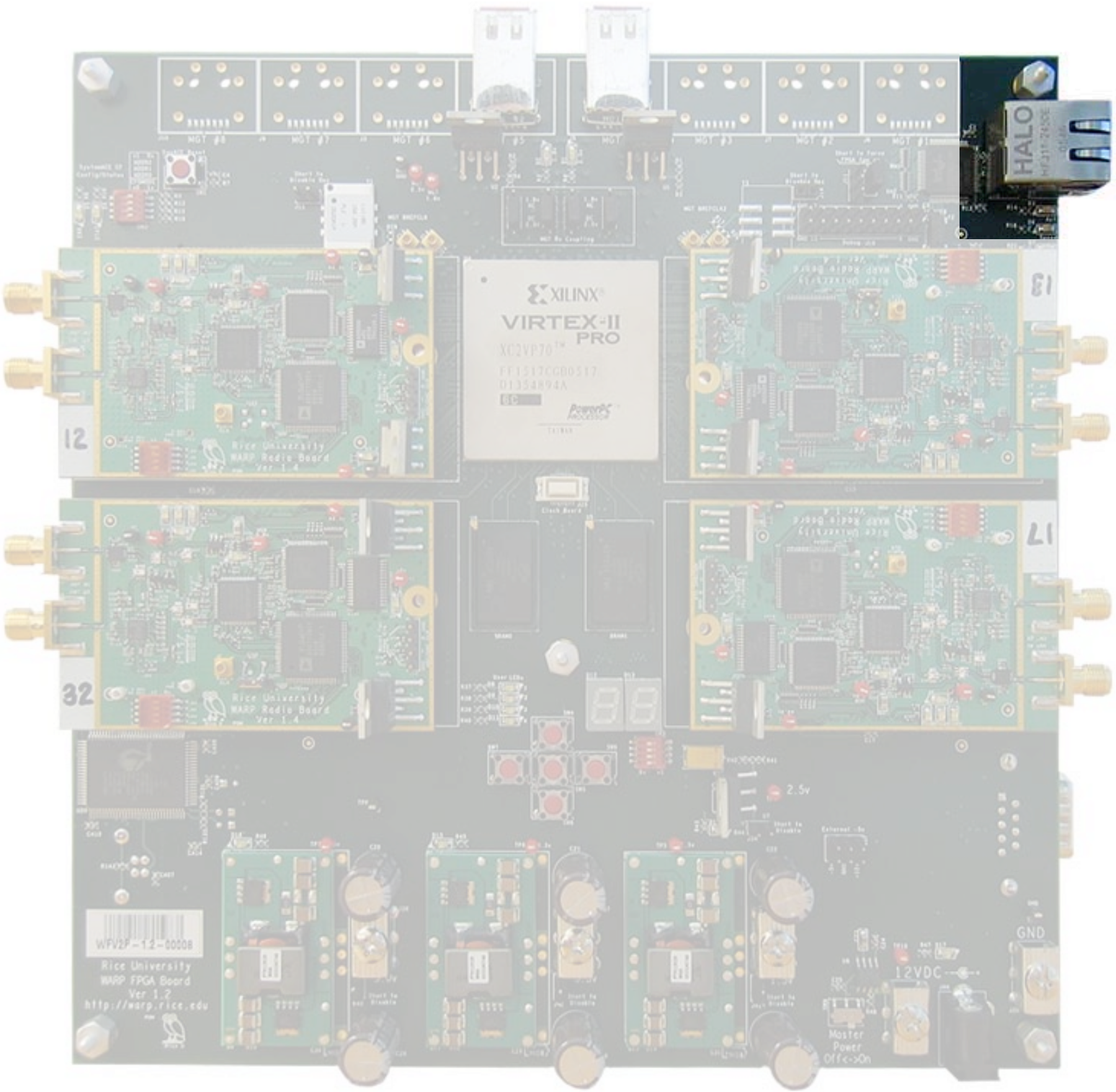
WARP - The Base Hardware



MIMO-capable radios

- 2.4 and 5GHz ISM Bands
- Wide-band operation (40MHz) for OFDM applications
- Direct baseband-RF upconversion and downconversion

WARP - The Base Hardware



Ethernet

- 10/100 Ethernet PHY
- Ethernet MAC core available from Xilinx

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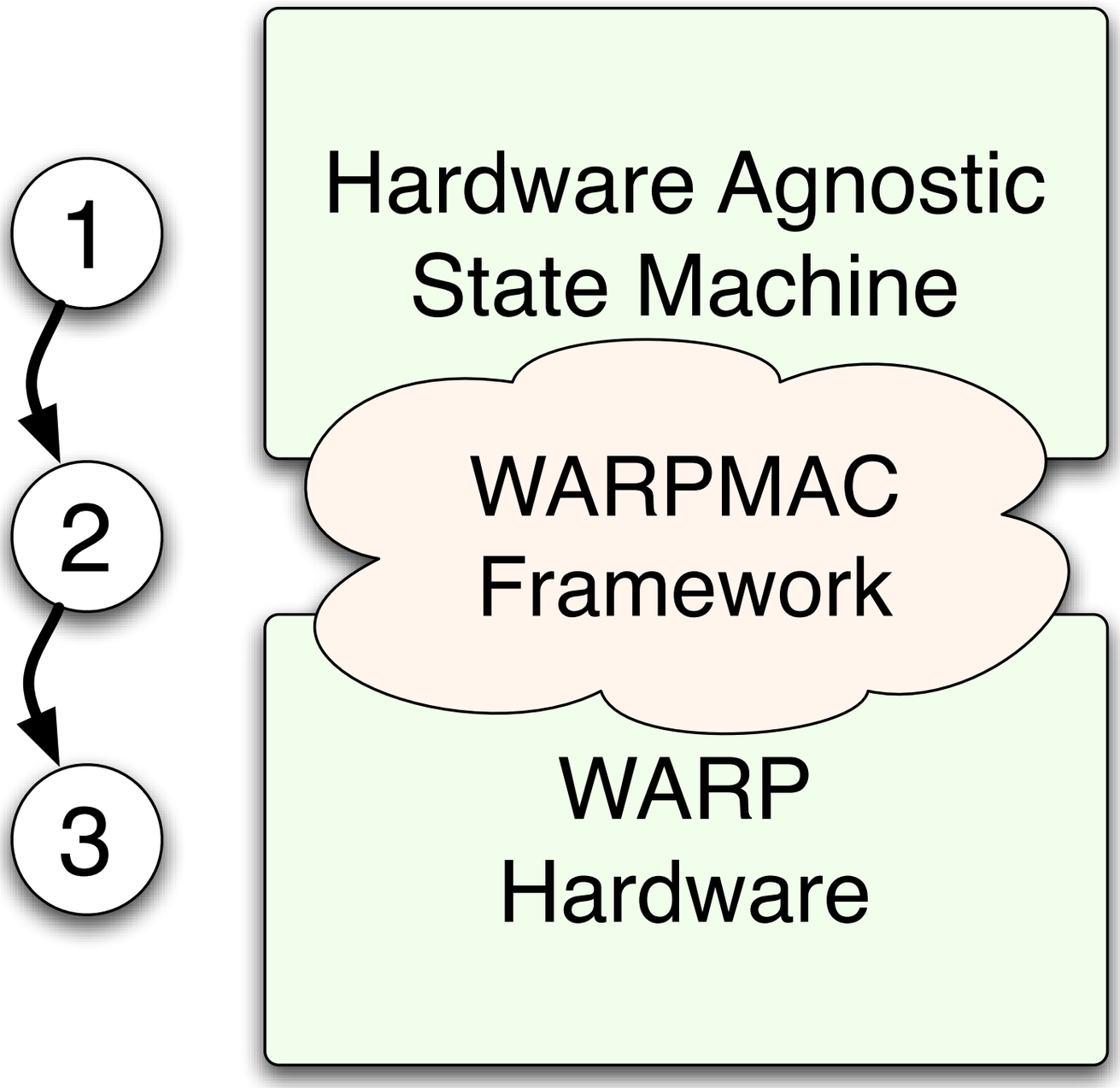
Design Realization



- Program high-level MAC behavior independent of hardware
- Use the WARPMAC framework to stitch the MAC to hardware

An example: ALOHA

- Simplest MAC
- Serves as a foundation to a large class of other random access protocols
- The algorithm is simple:

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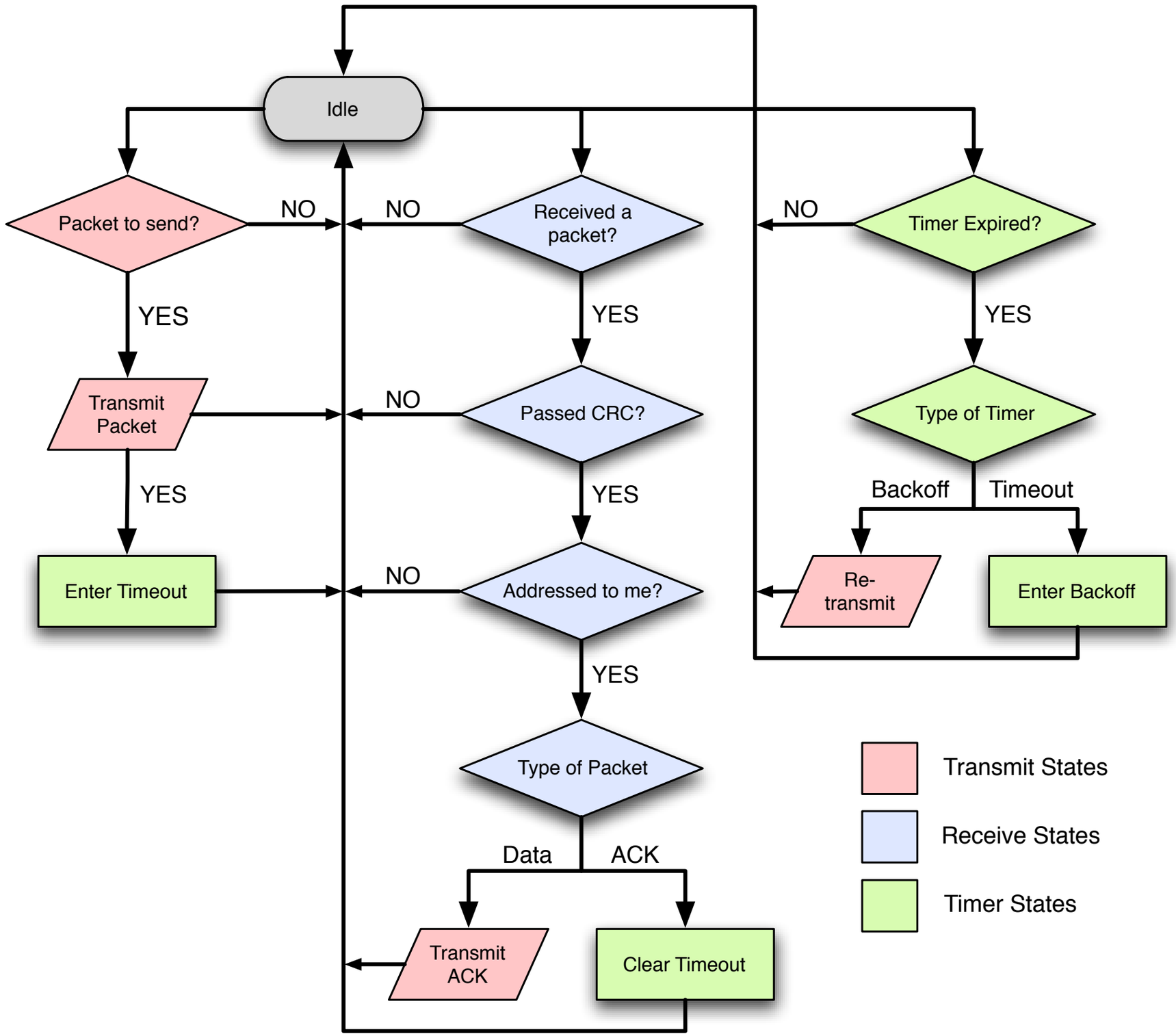
Packet to send? Just send it

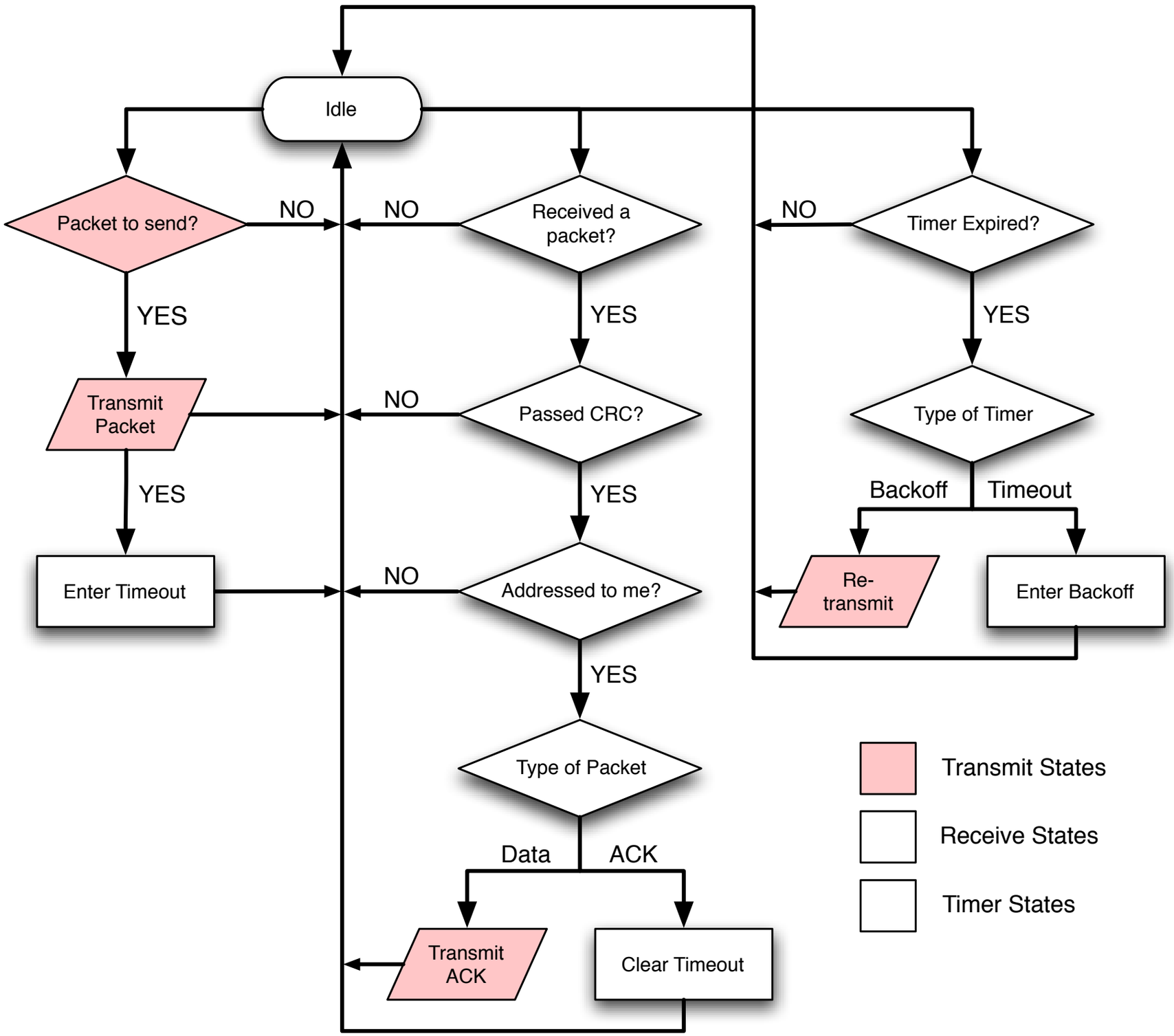
Received a packet? Send an ACK

Received no ACK? Backoff and resend

An example: ALOHA
PHY Agnostic State Machine



An example: ALOHA
Implicit Hardware Requirements



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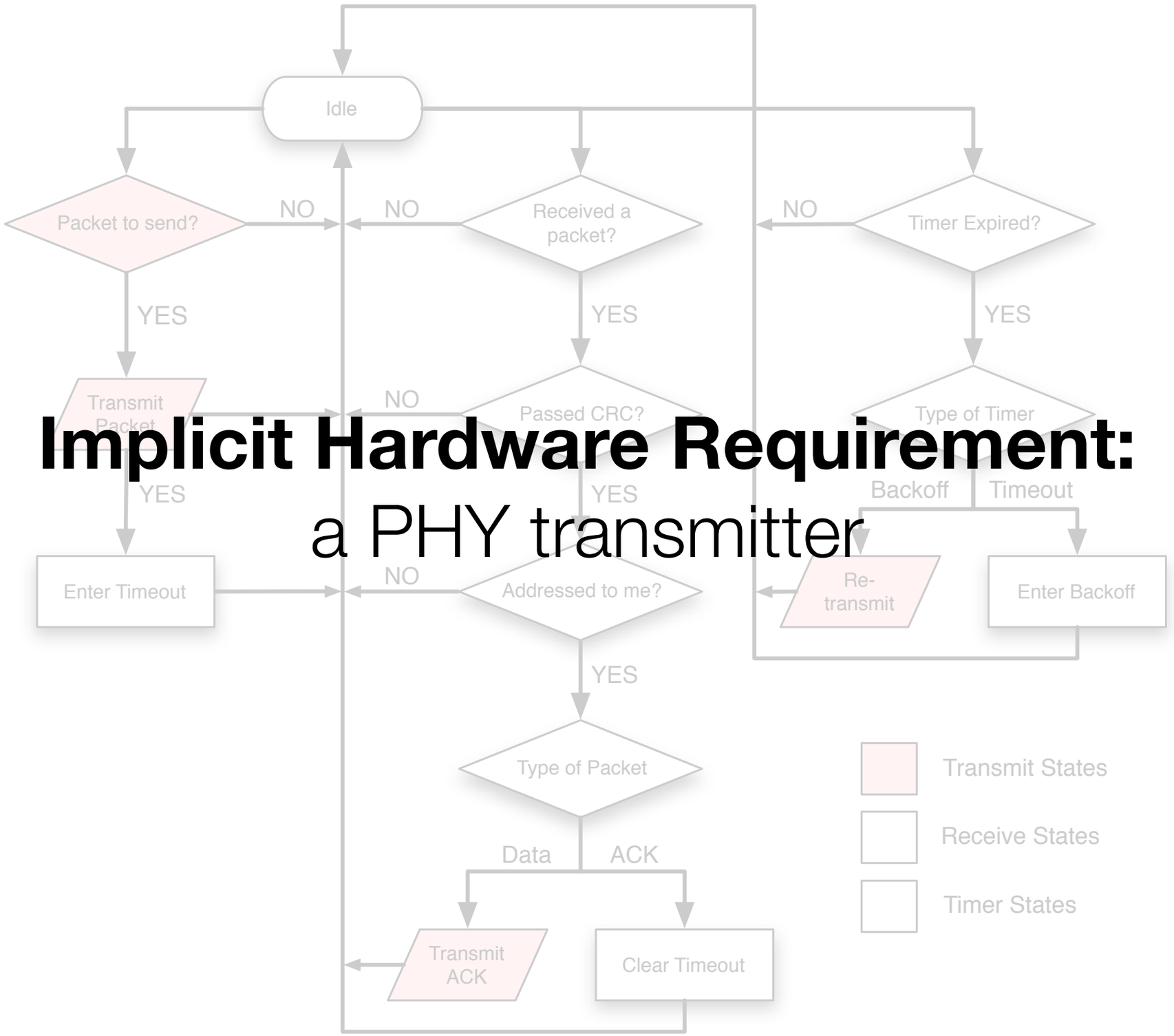

Implicit Hardware Requirement:
a PHY transmitter

An example: ALOHA
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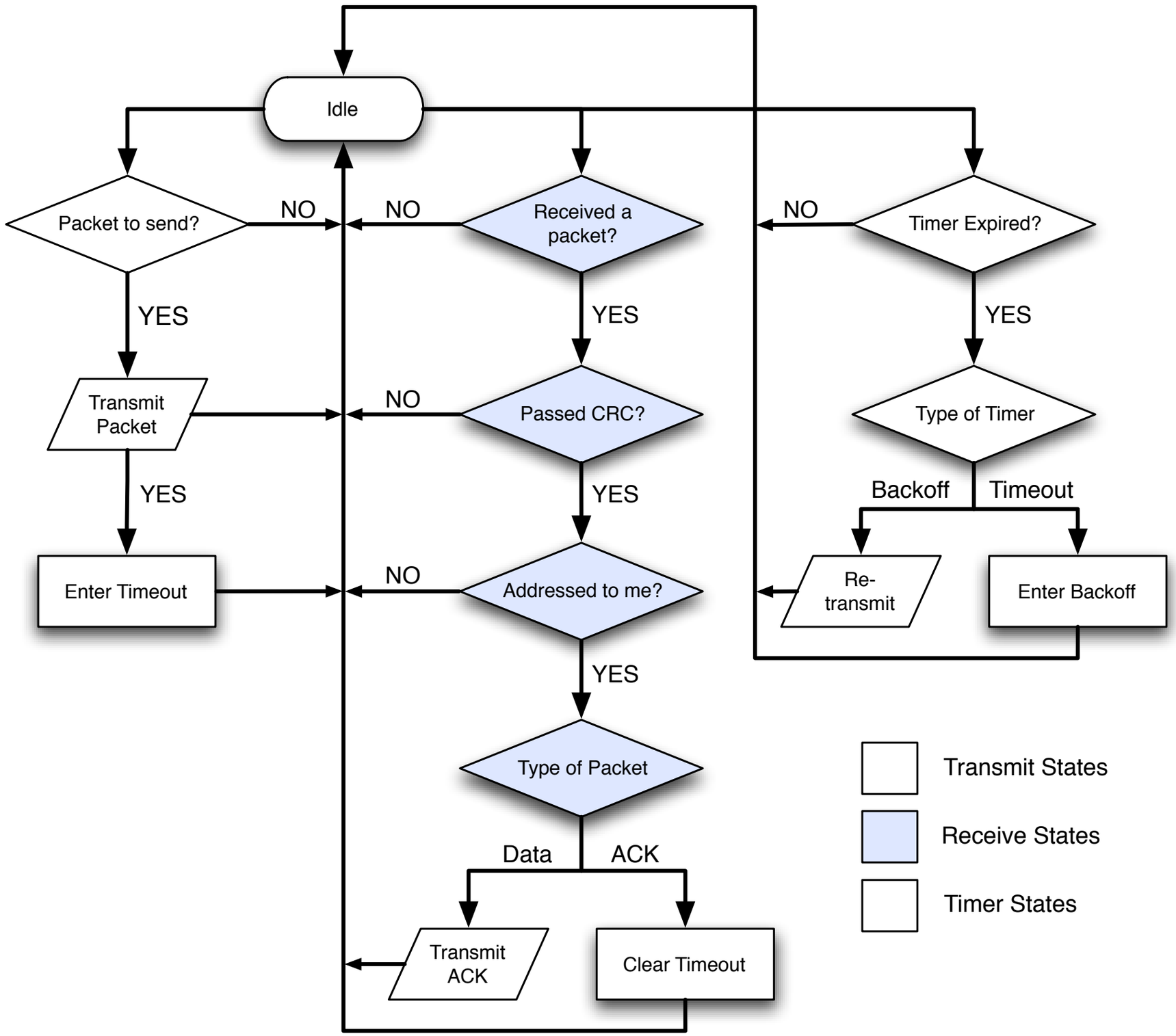

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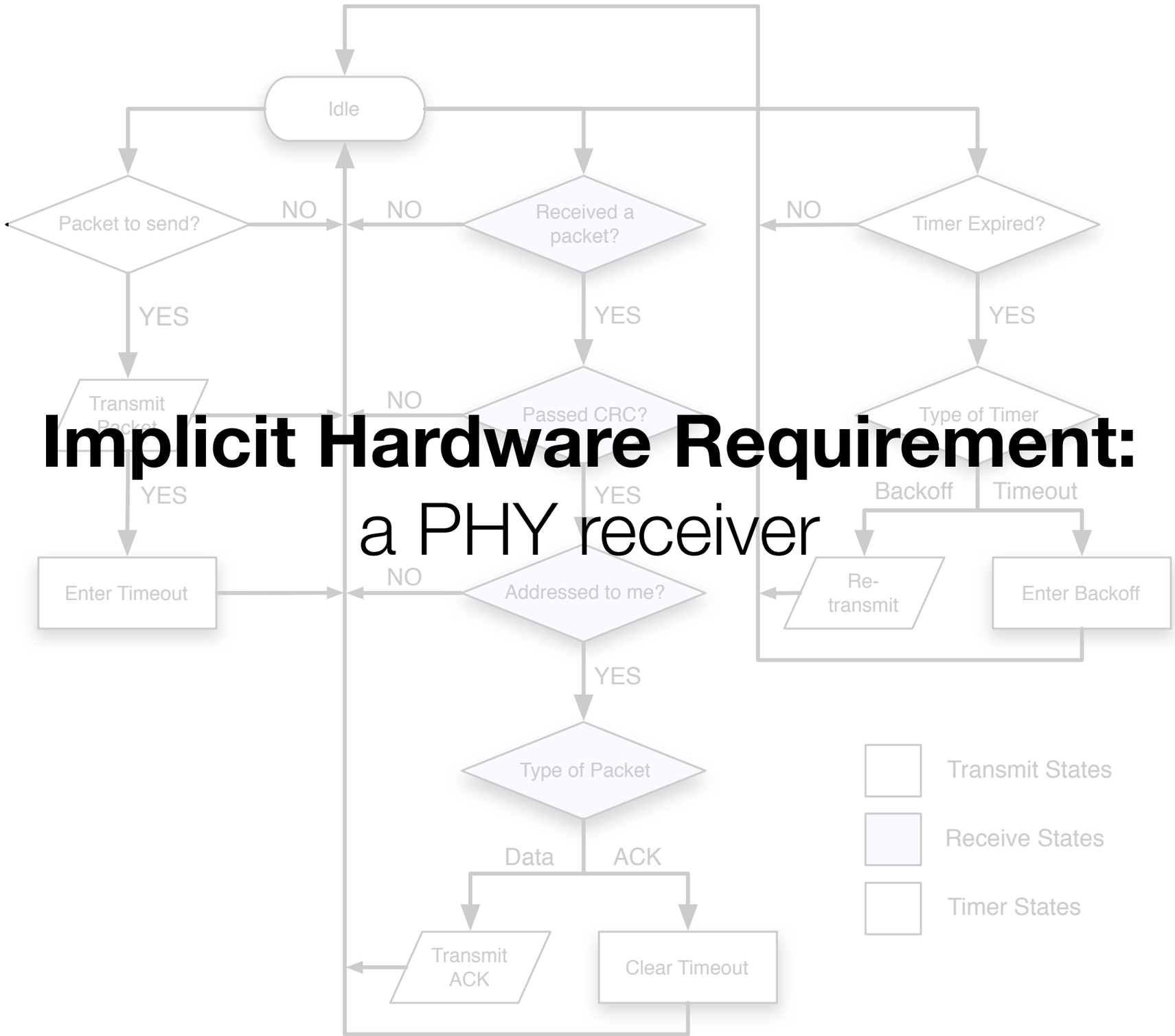
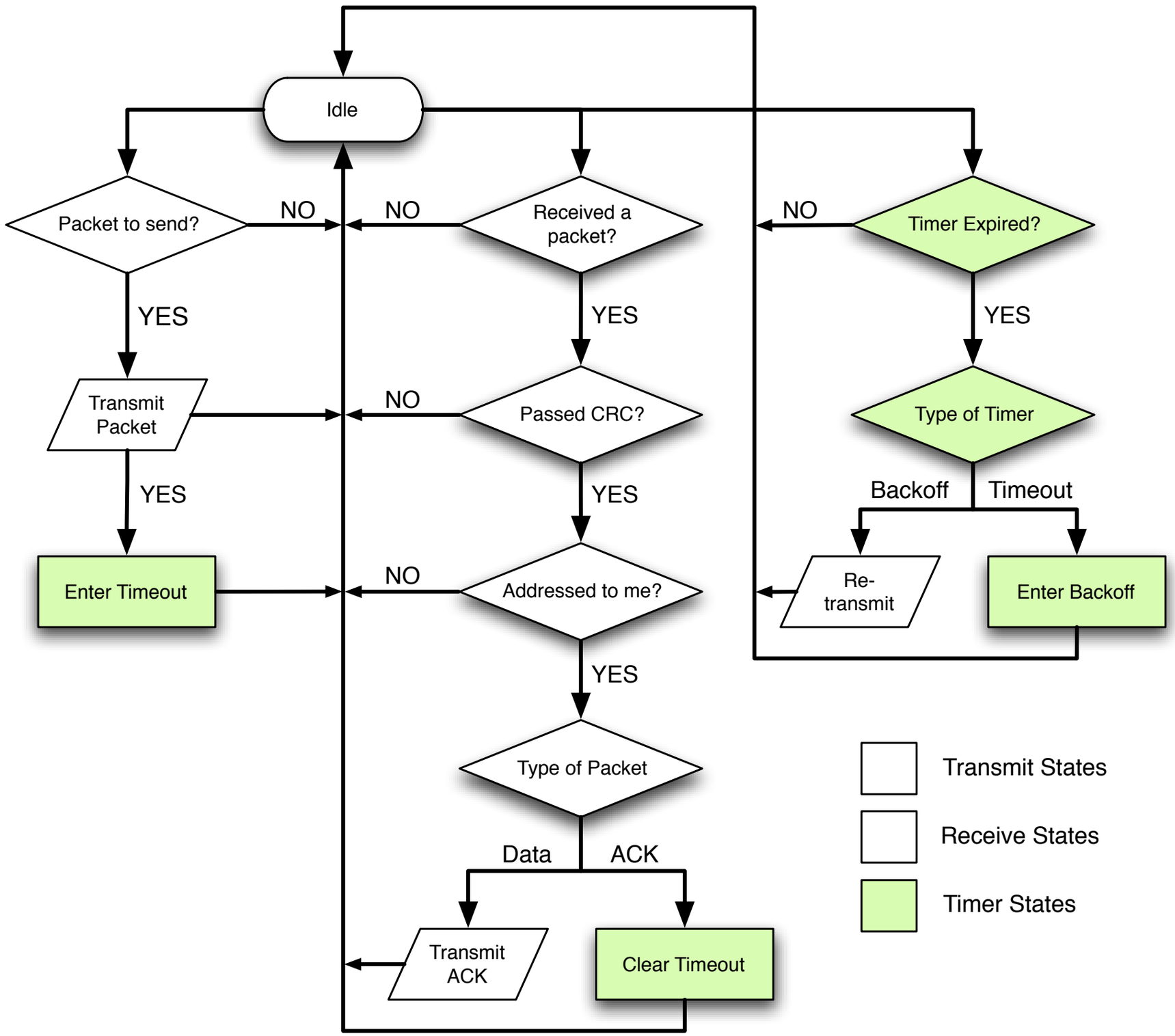


Implicit Hardware Requirement:
a PHY receiver

An example: ALOHA
Implicit Hardware Requirements



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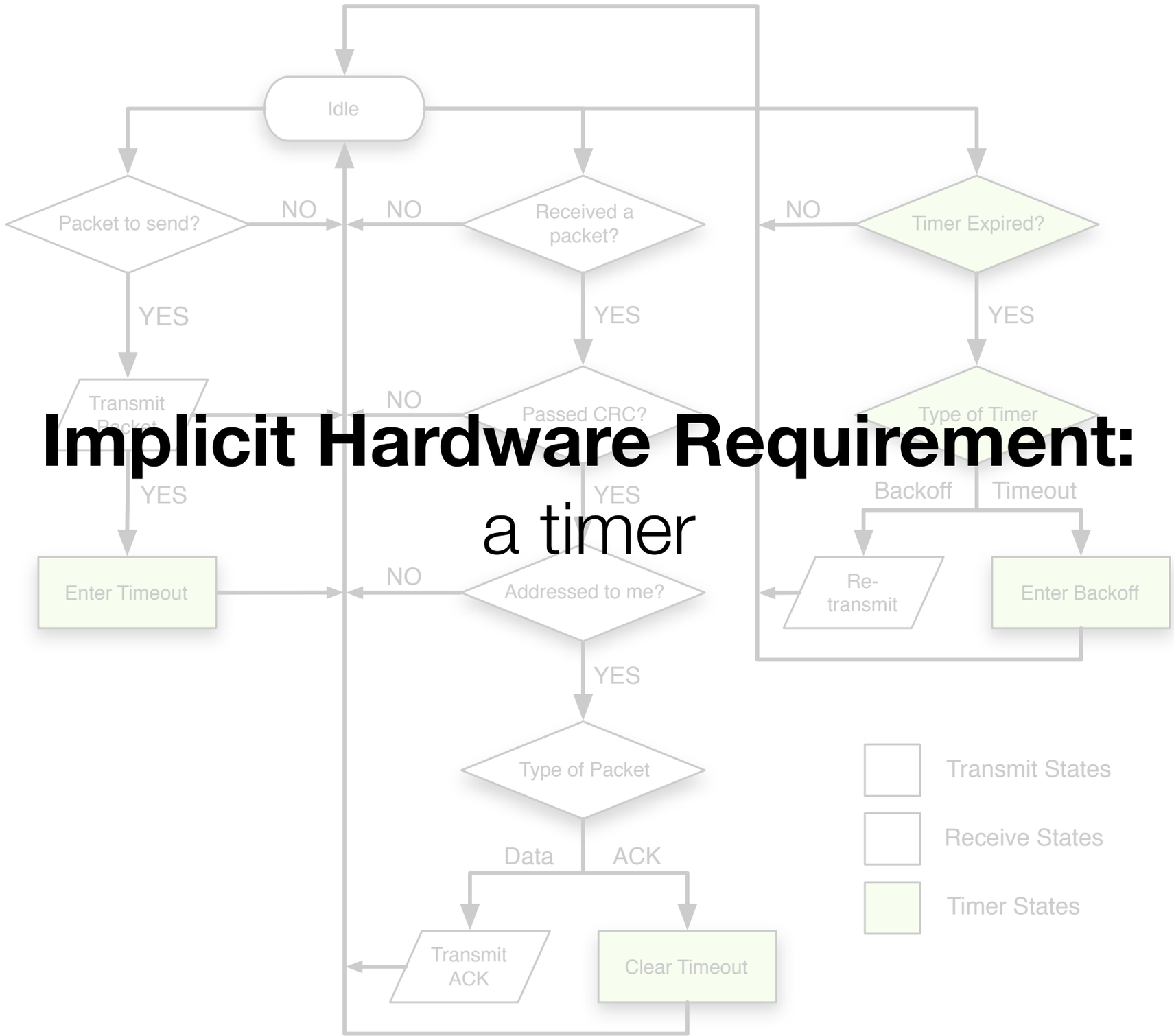
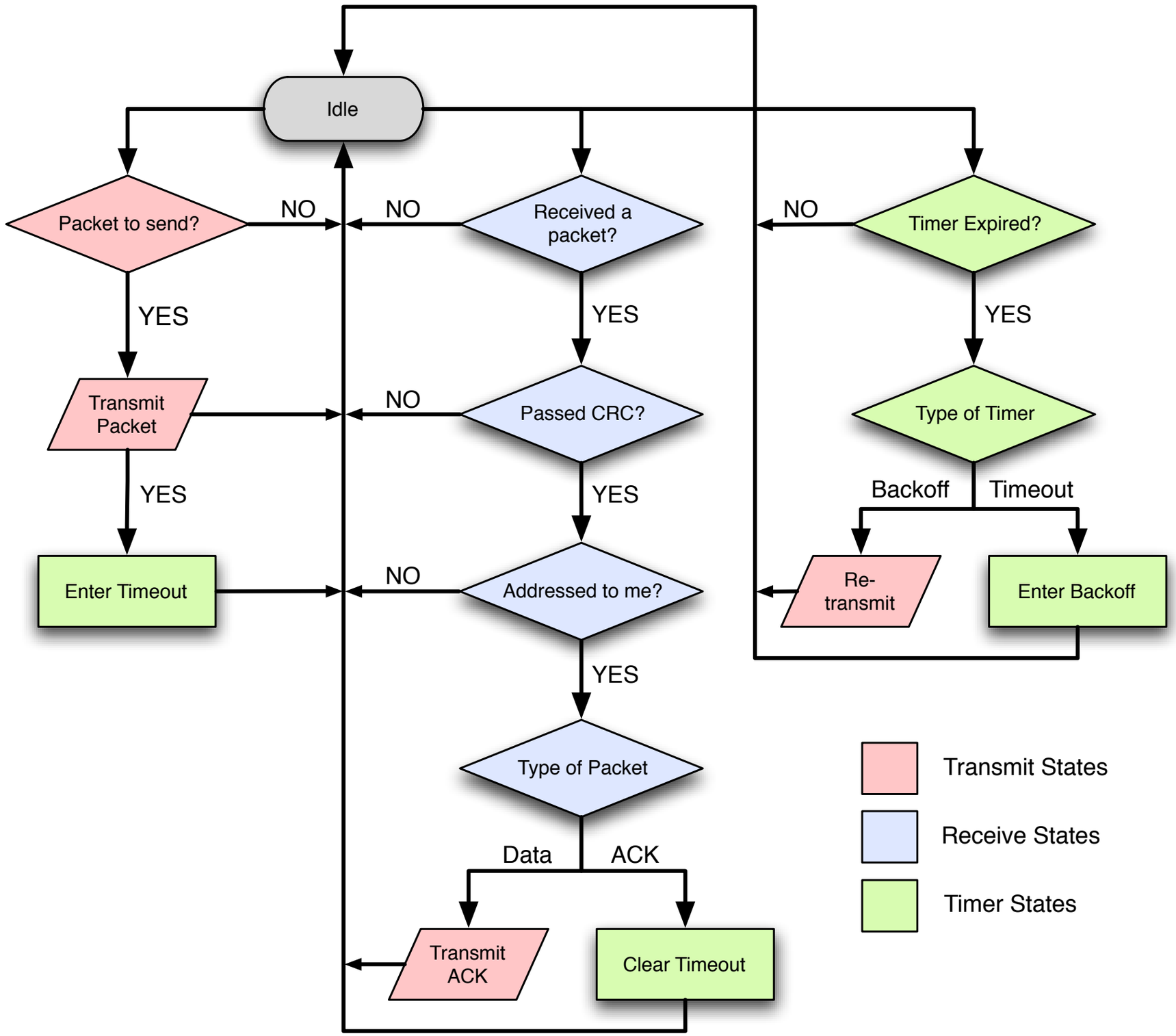


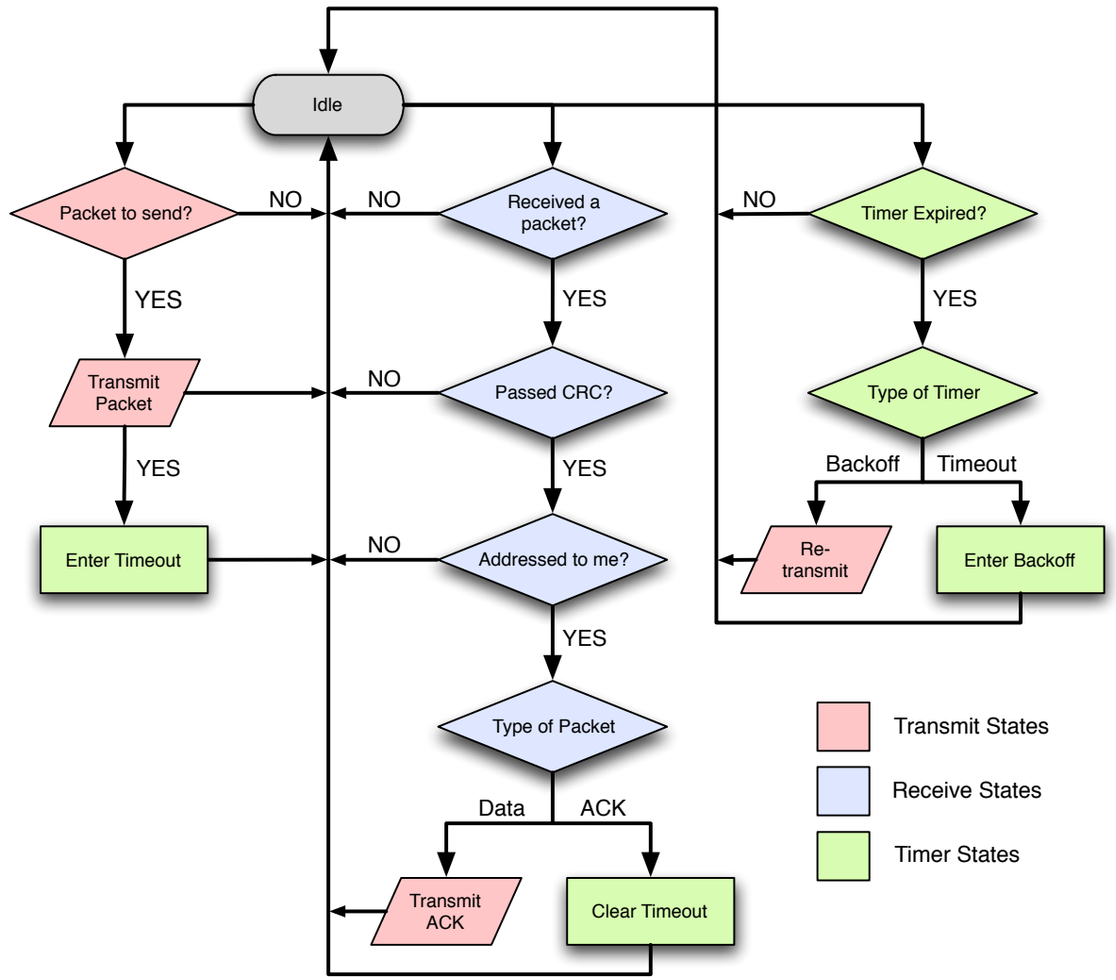
Implicit Hardware Requirement:

a timer

An example: ALOHA
PHY Agnostic State Machine



Hardware Requirements



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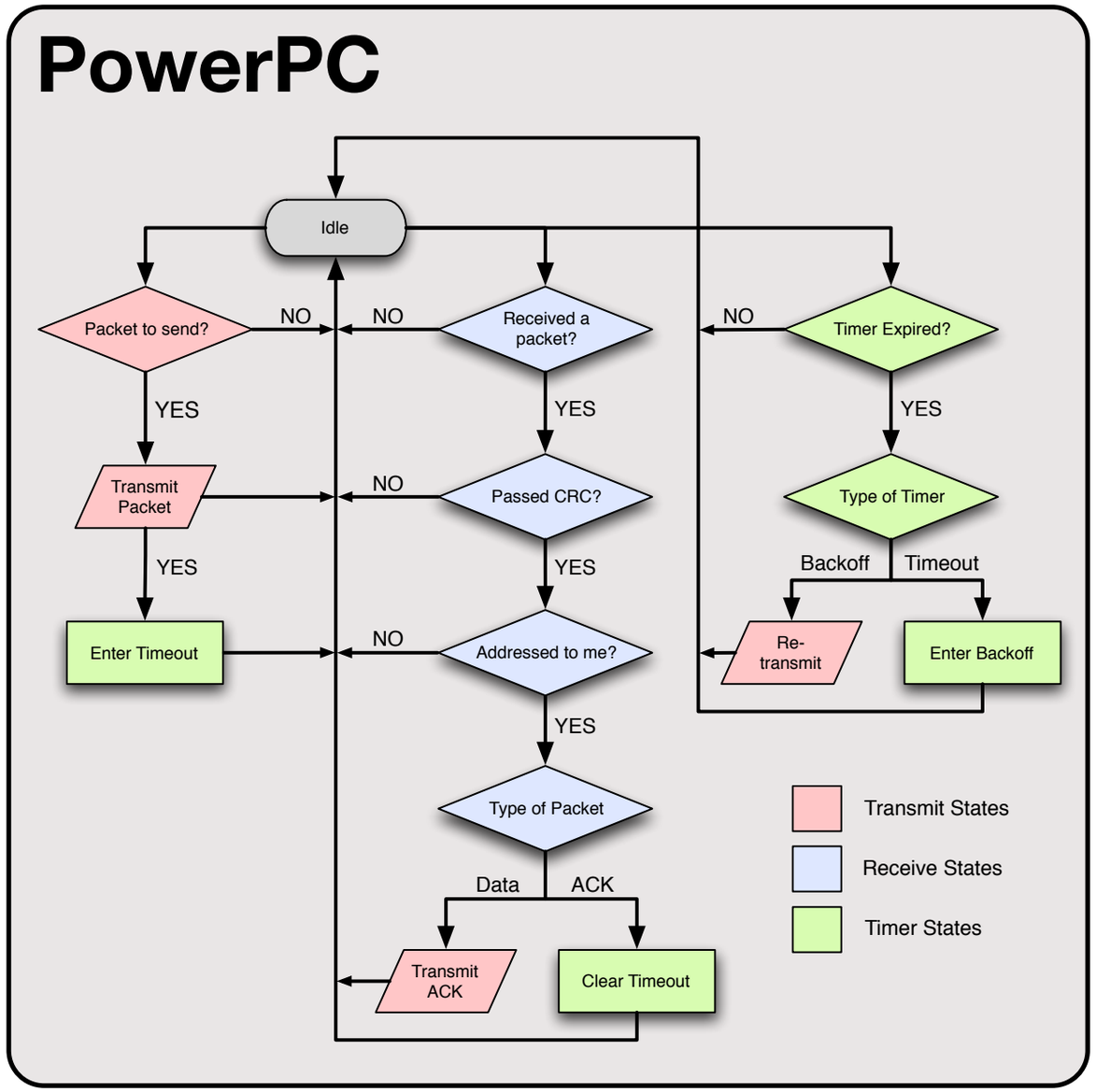
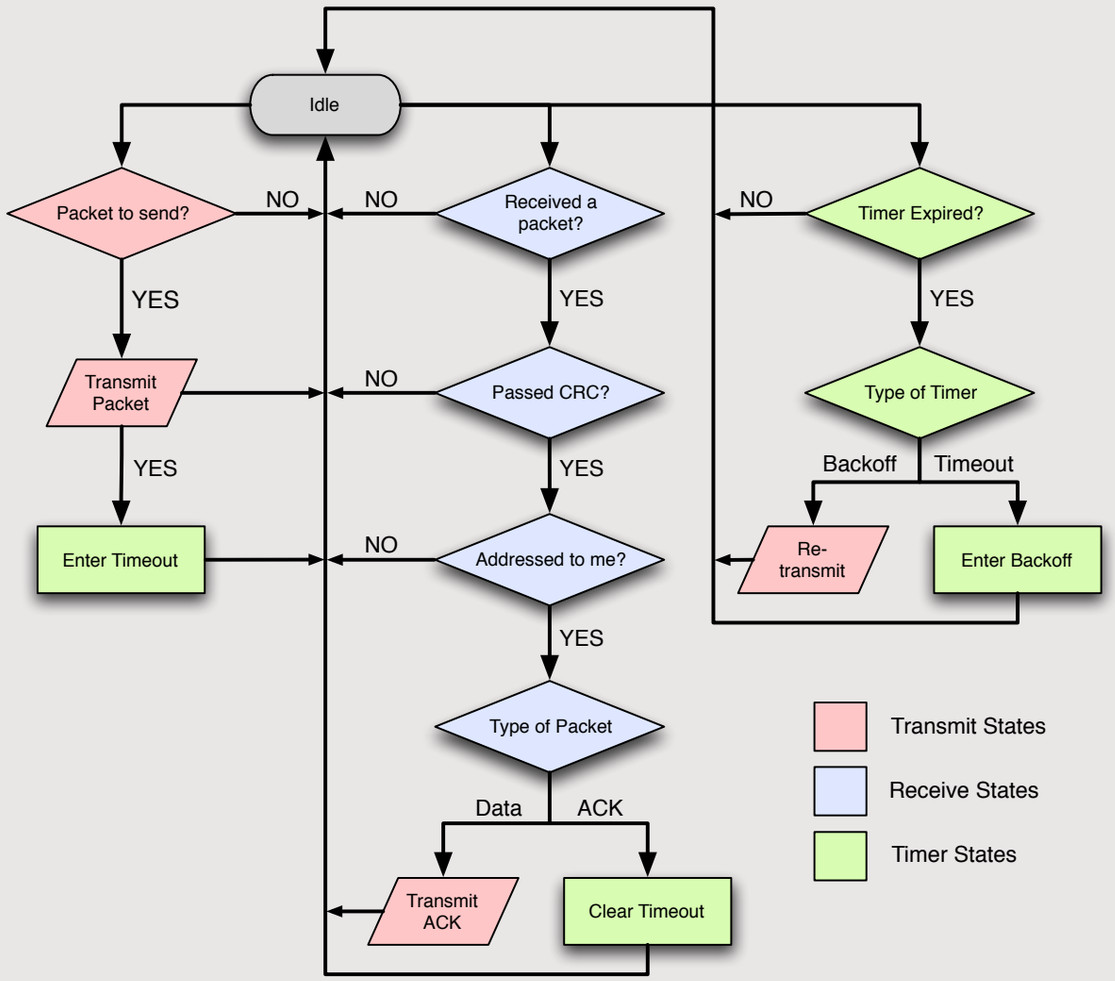


Hardware Requirements

PHY Transmitter

PHY Receiver

PowerPC



Hardware Timer

Ethernet

Hardware Requirements

PHY Transmitter

PHY Receiver

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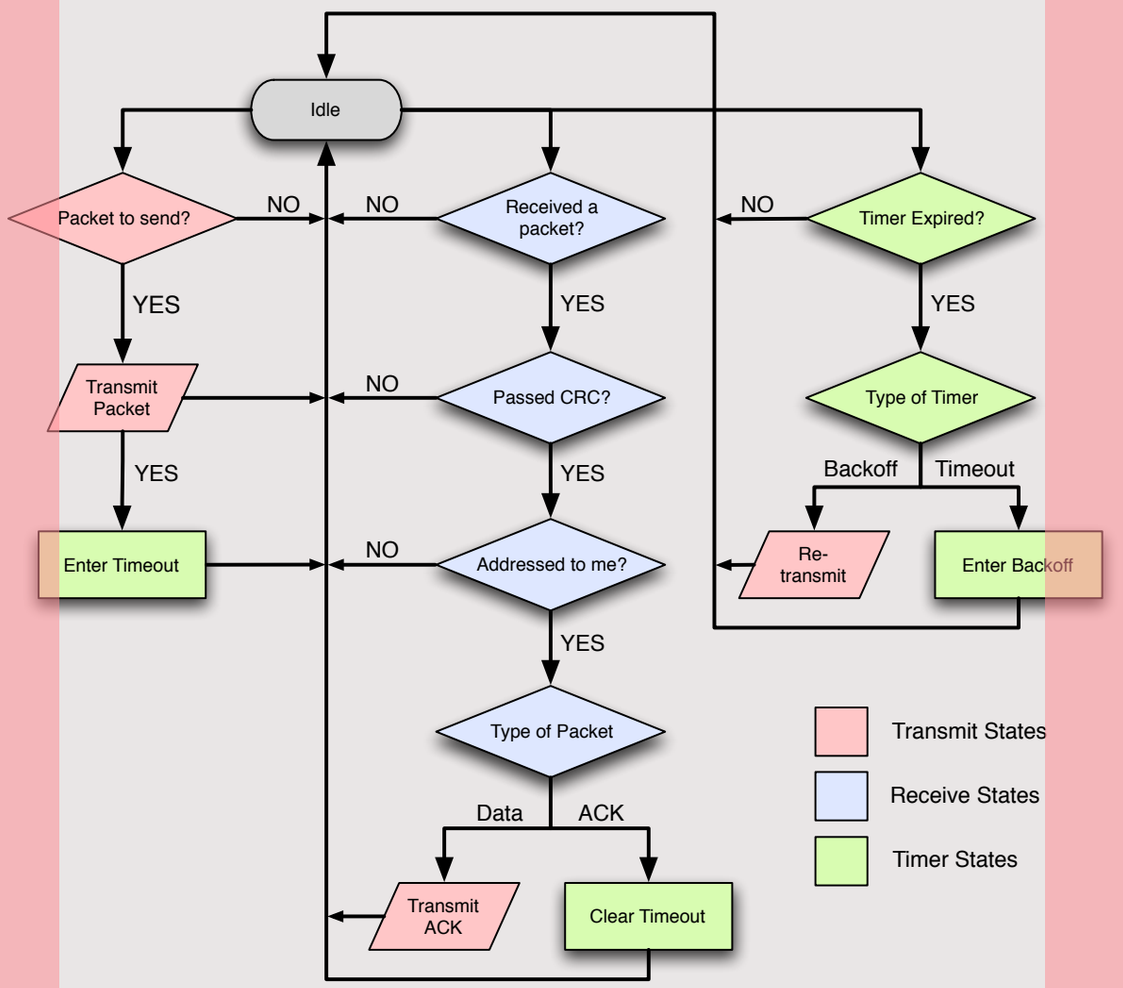


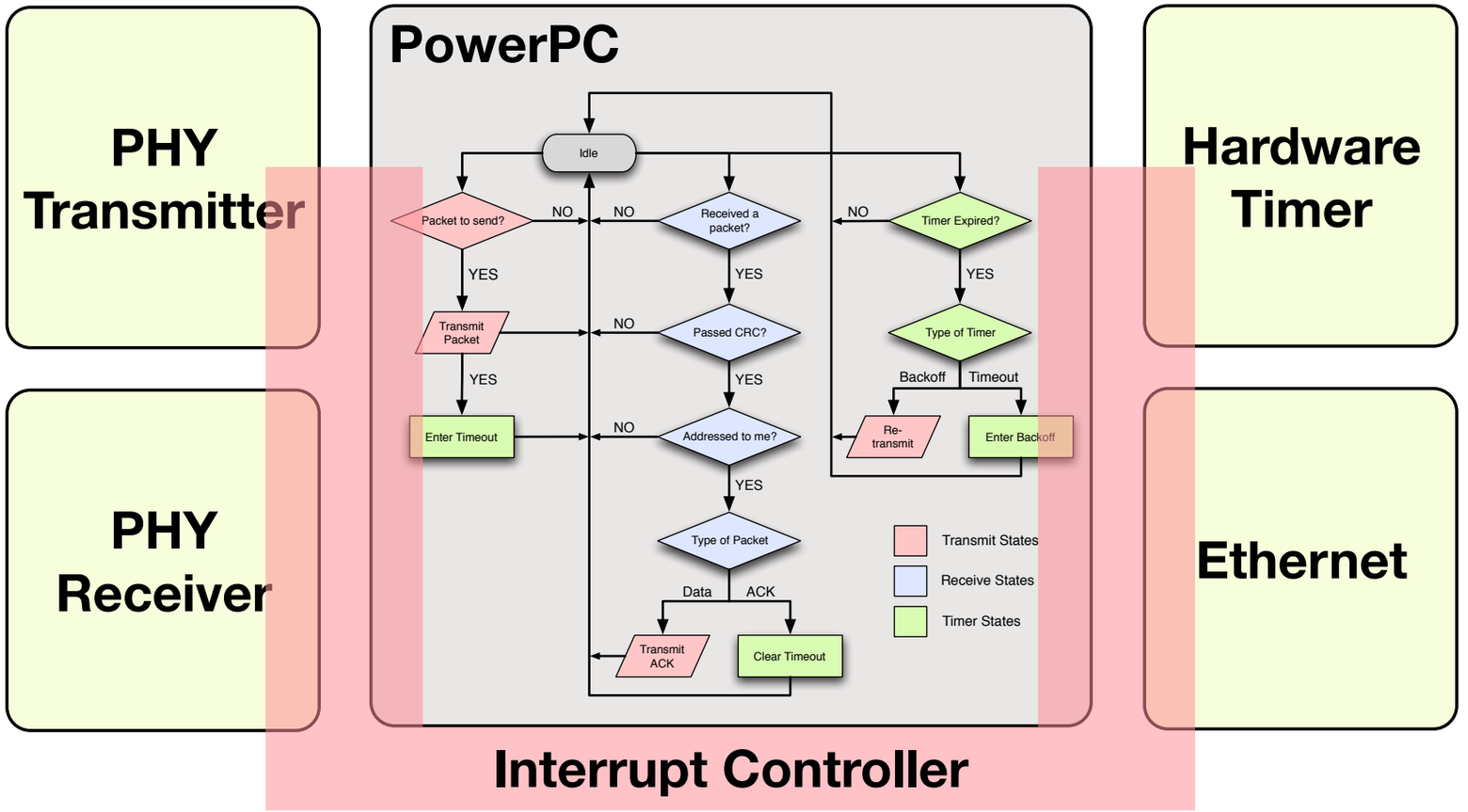
Hardware Timer

Ethernet

Interrupt Controller

Hardware Platform

Hardware Platform



Hardware Platform

Radio Controller

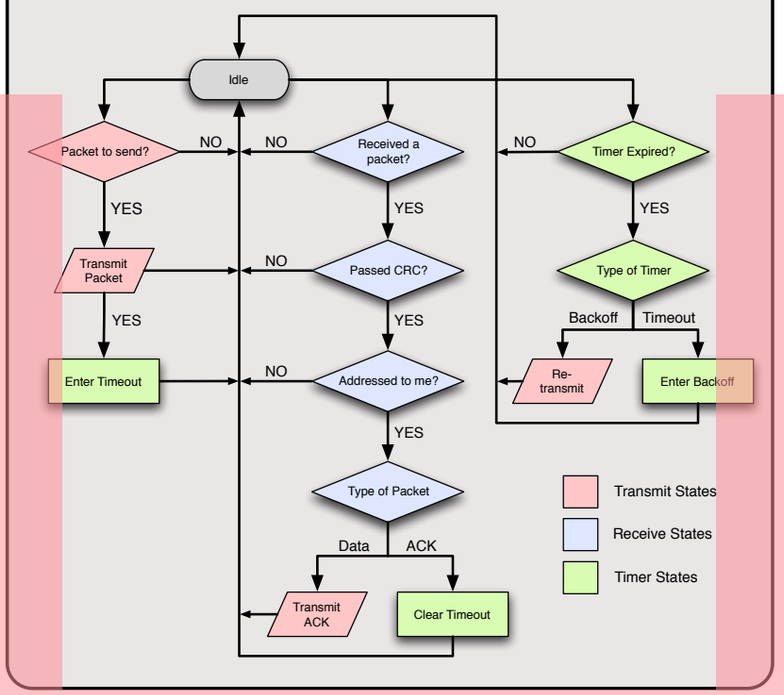
Packet Detection

Automatic Gain Control

PHY Transmitter

PHY Receiver

PowerPC



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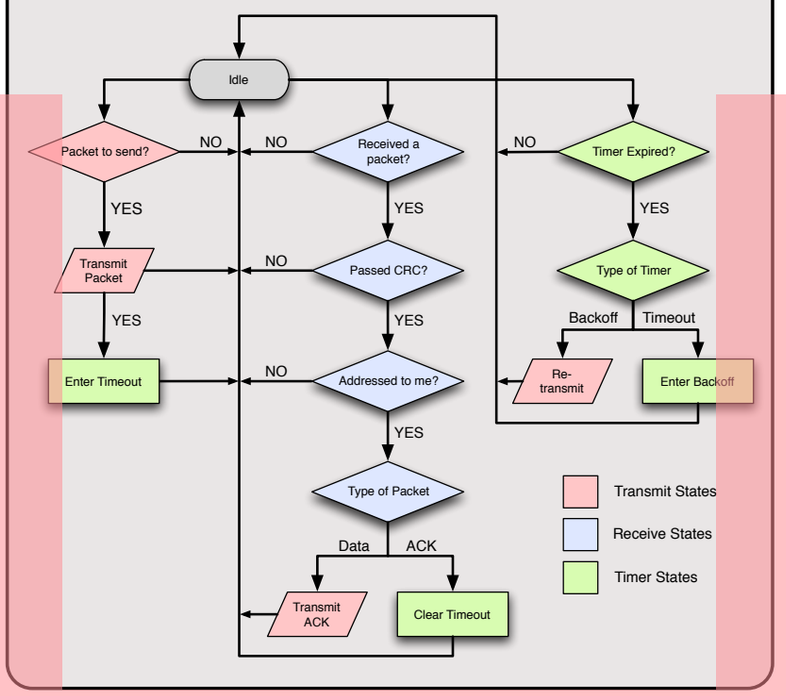


Interrupt Controller

Hardware Timer

Ethernet

Push-buttons

LEDs

RS232 Serial

Hardware Platform

Radio Controller

Packet Detection

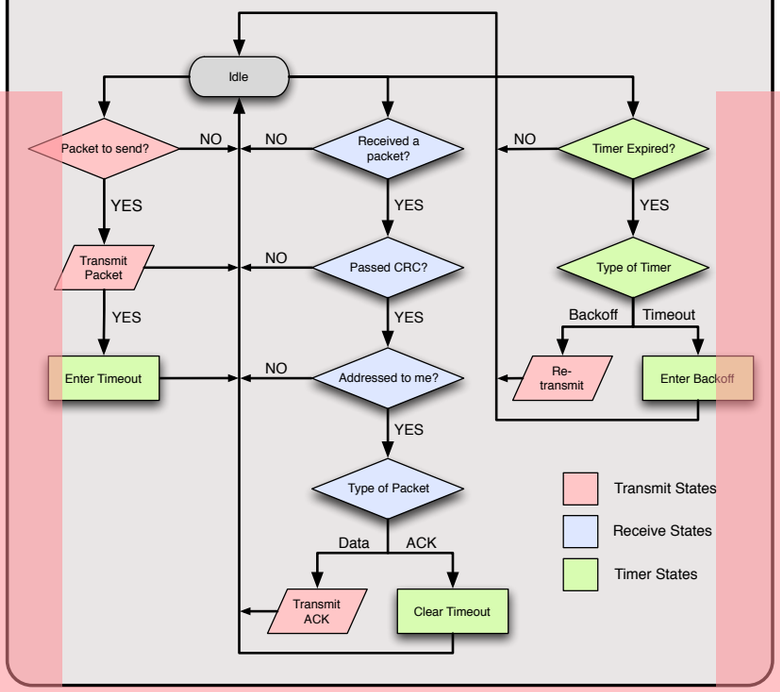
Automatic Gain Control

PowerPC

Control Code

PHY Transmitter

PHY Receiver



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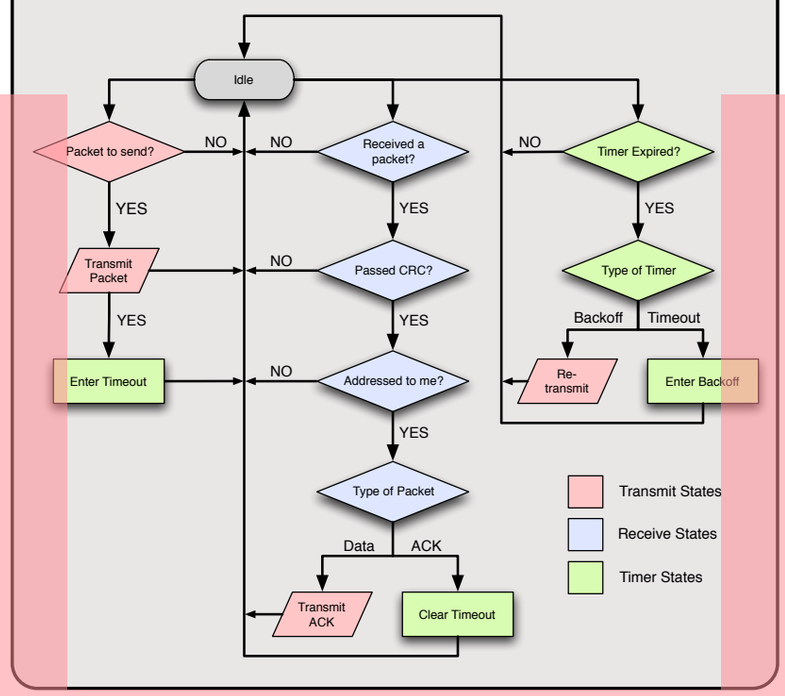

Interrupt Controller

Hardware Timer

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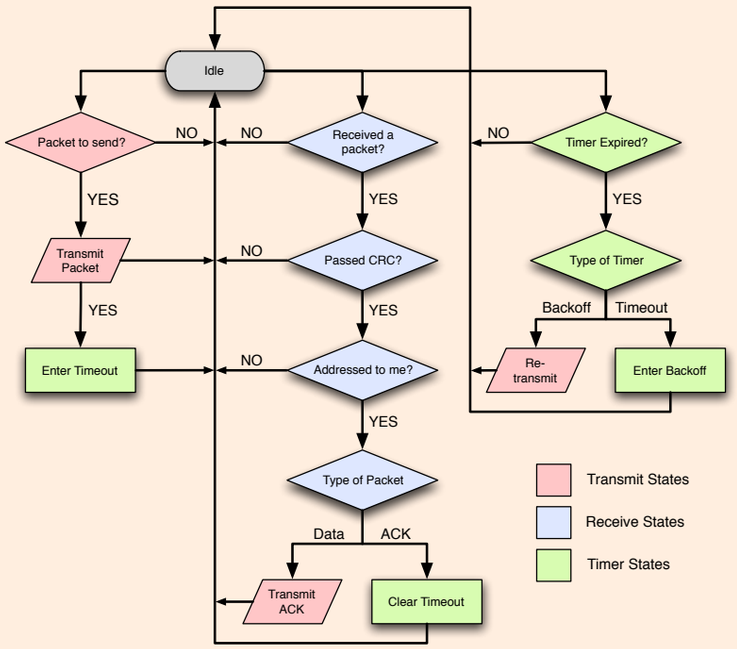
RS232 Serial

Processor Busses (OPB/PLB)

One extreme: Abstract away everything

WARPMAC



Ease of use at the cost of flexibility

Somewhere in between

WARPMAC

PowerPC

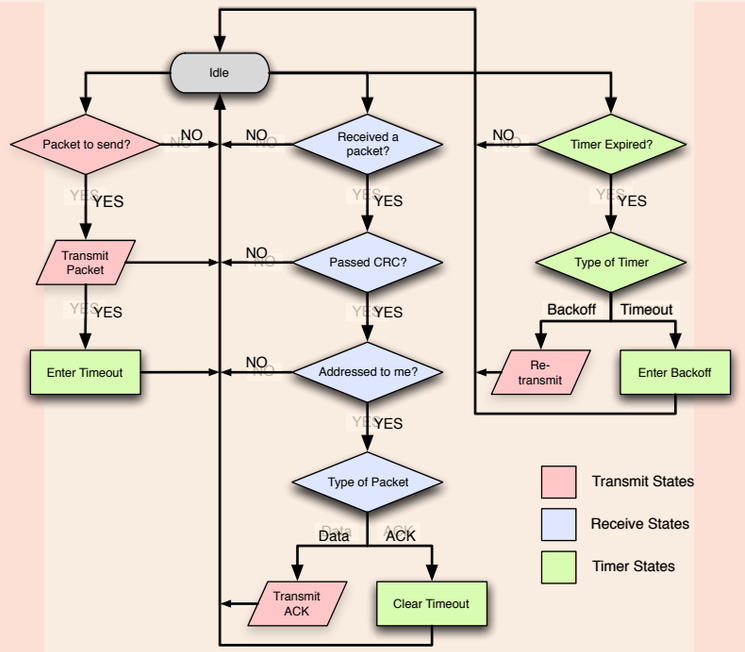
Control Code

Radio Controller

PHY Transmitter

Hardware Timer

Push-buttons



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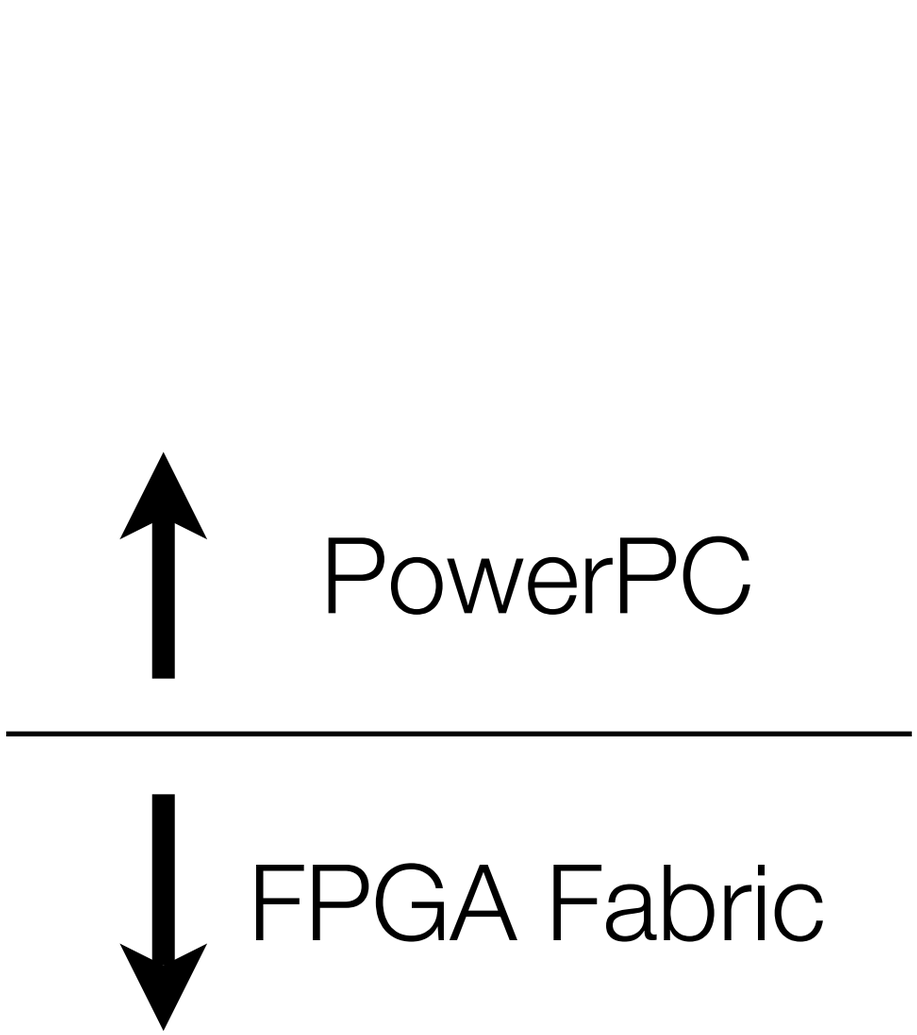
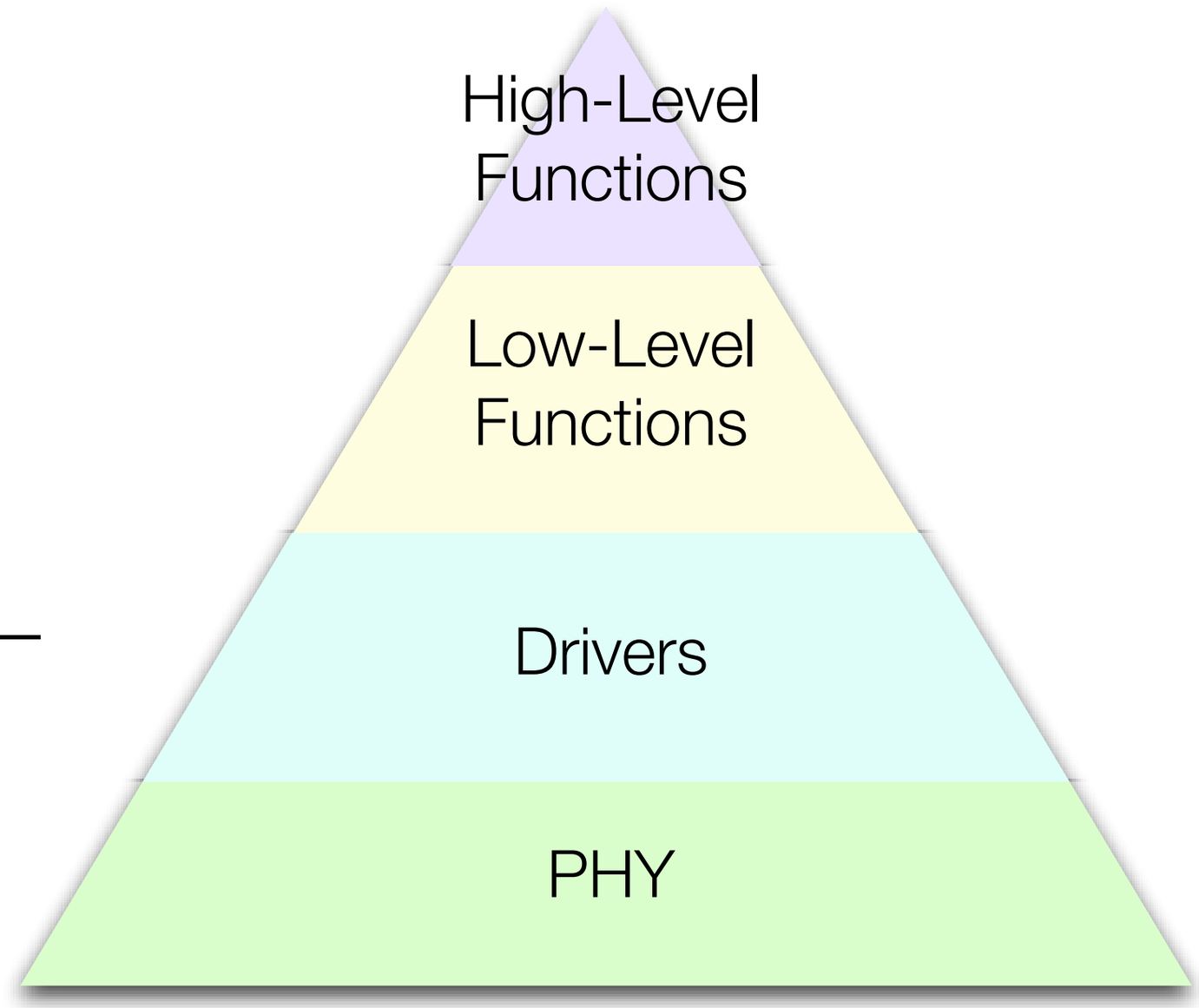
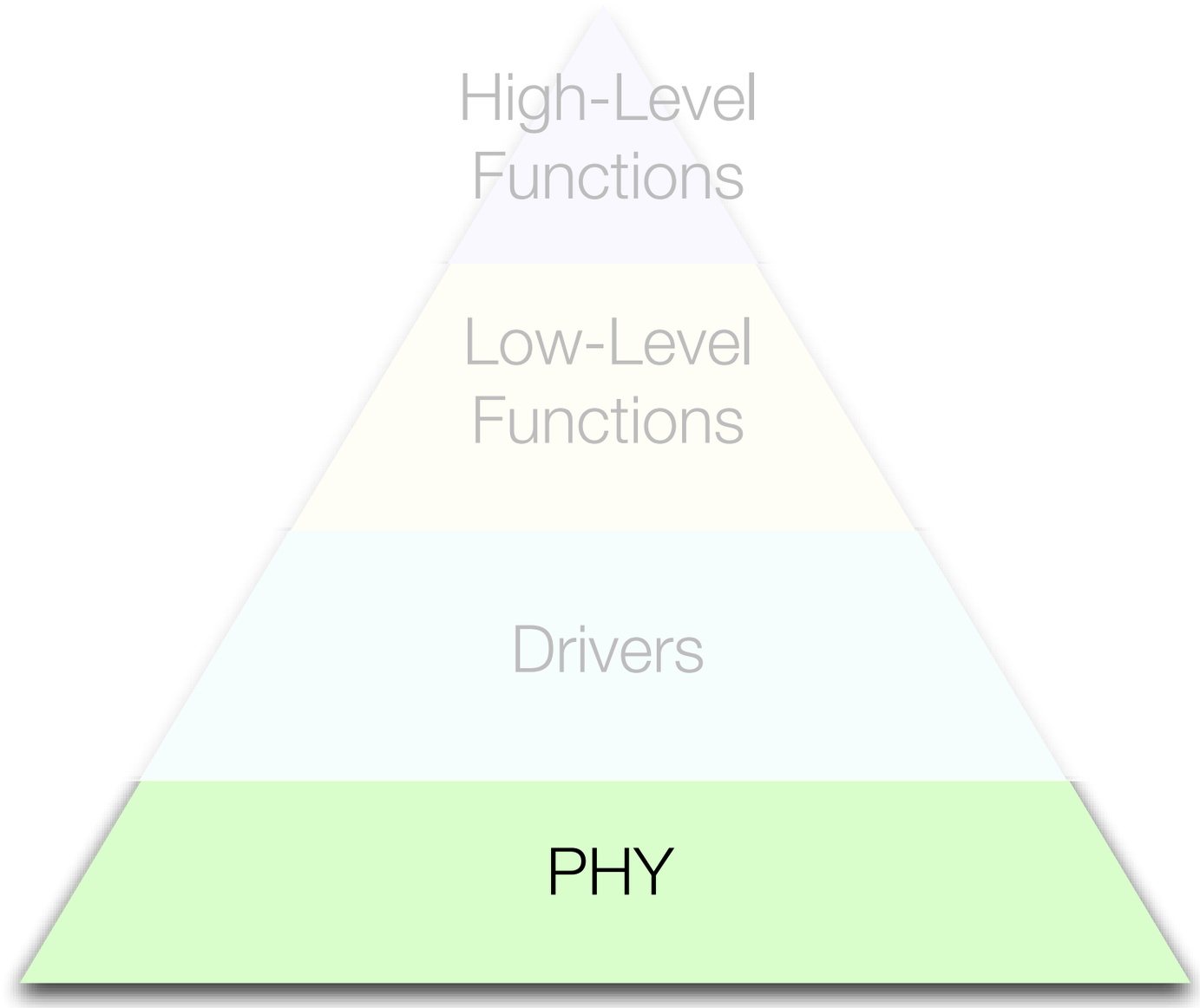

PowerPC
FPGA Fabric


High-Level Functions
Low-Level Functions
Drivers
PHY

WARPMAC

Current Offering:

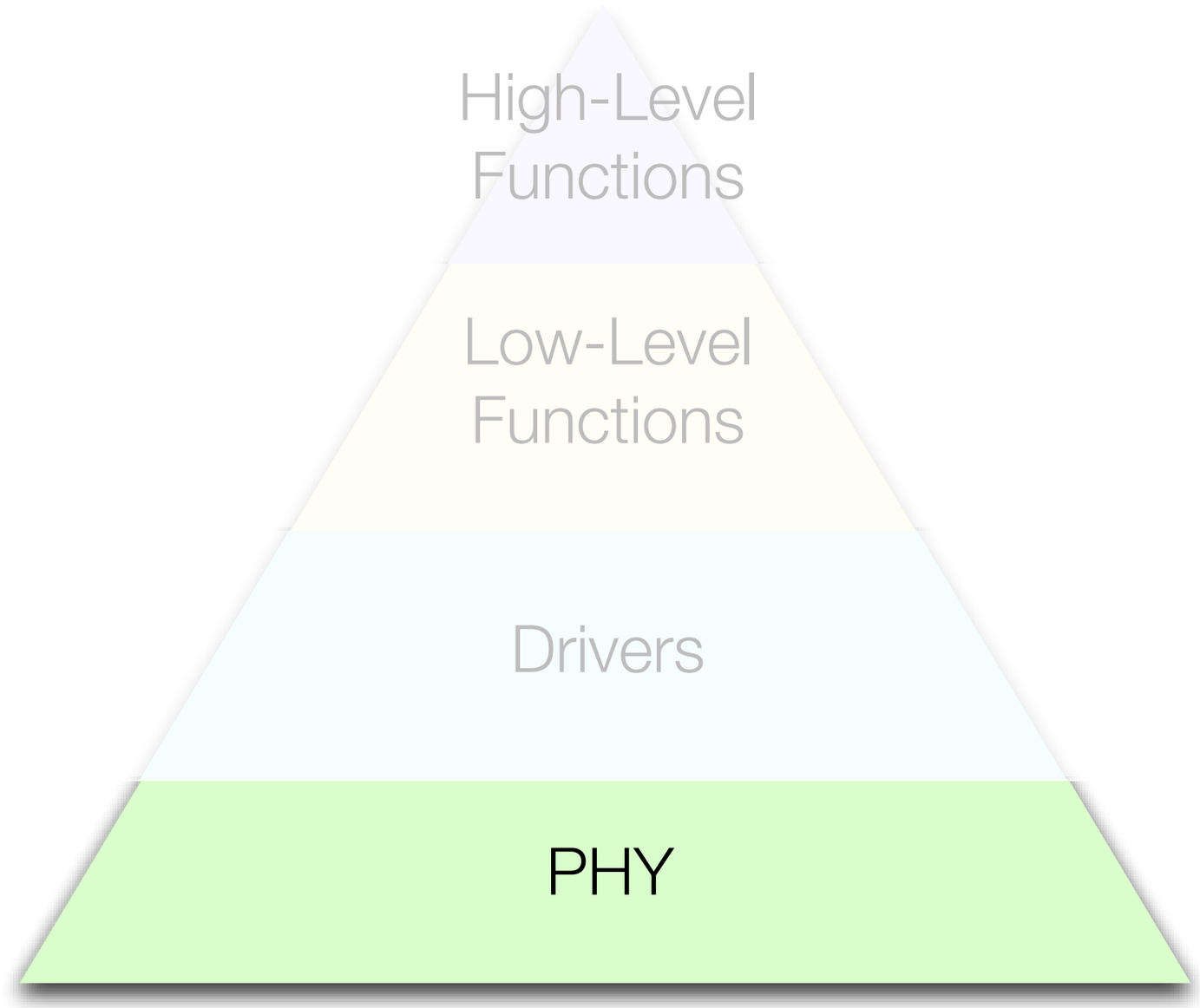
- Custom OFDM Baseband Processor
  - Flexible data rate starting at 12Mbps
  - Hardware CRC
  - Hardware CSMA



WARPMAC

In General:

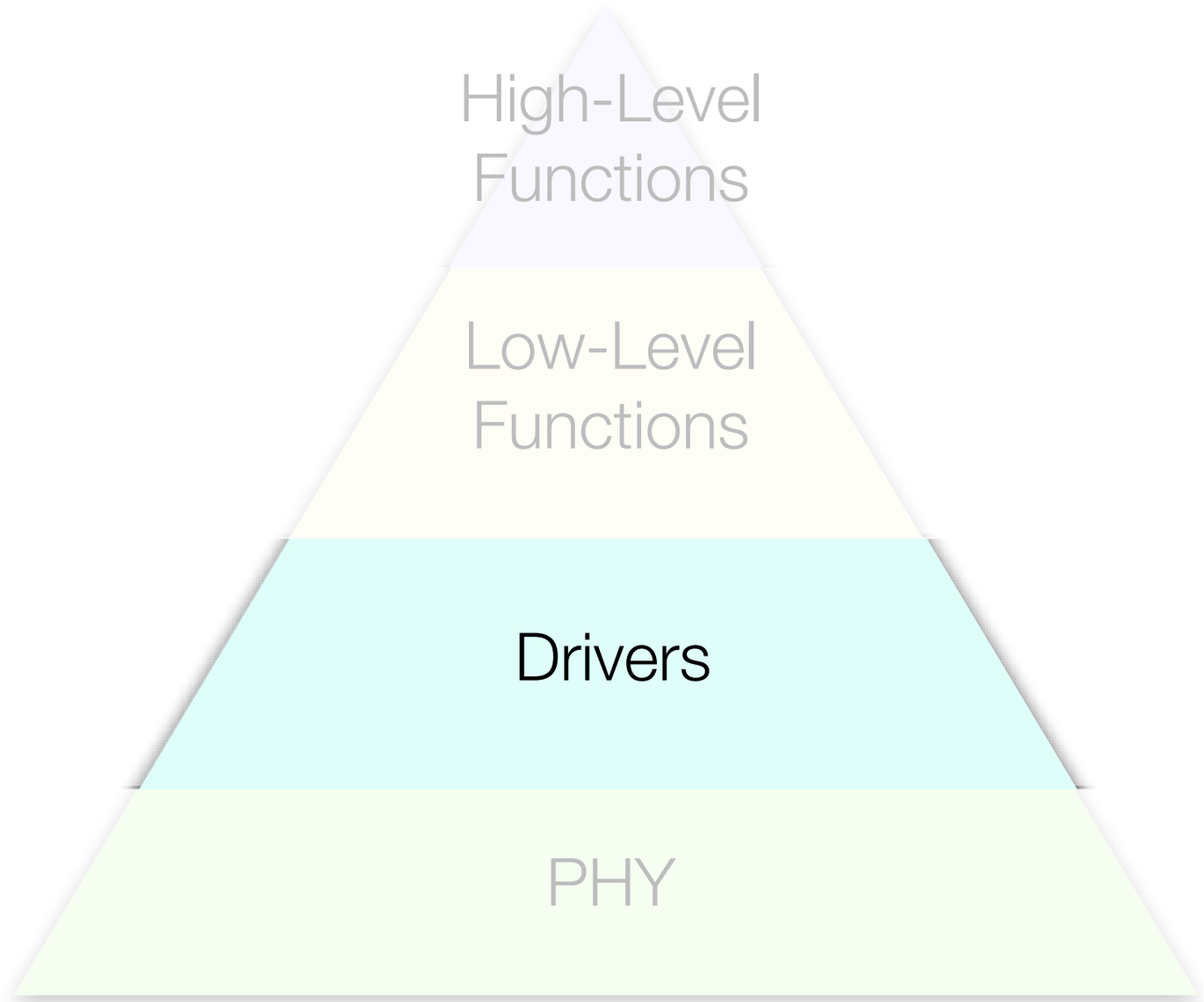
- SISO/MIMO, wide/narrow band are all possible



WARPMAC

PHY Driver:

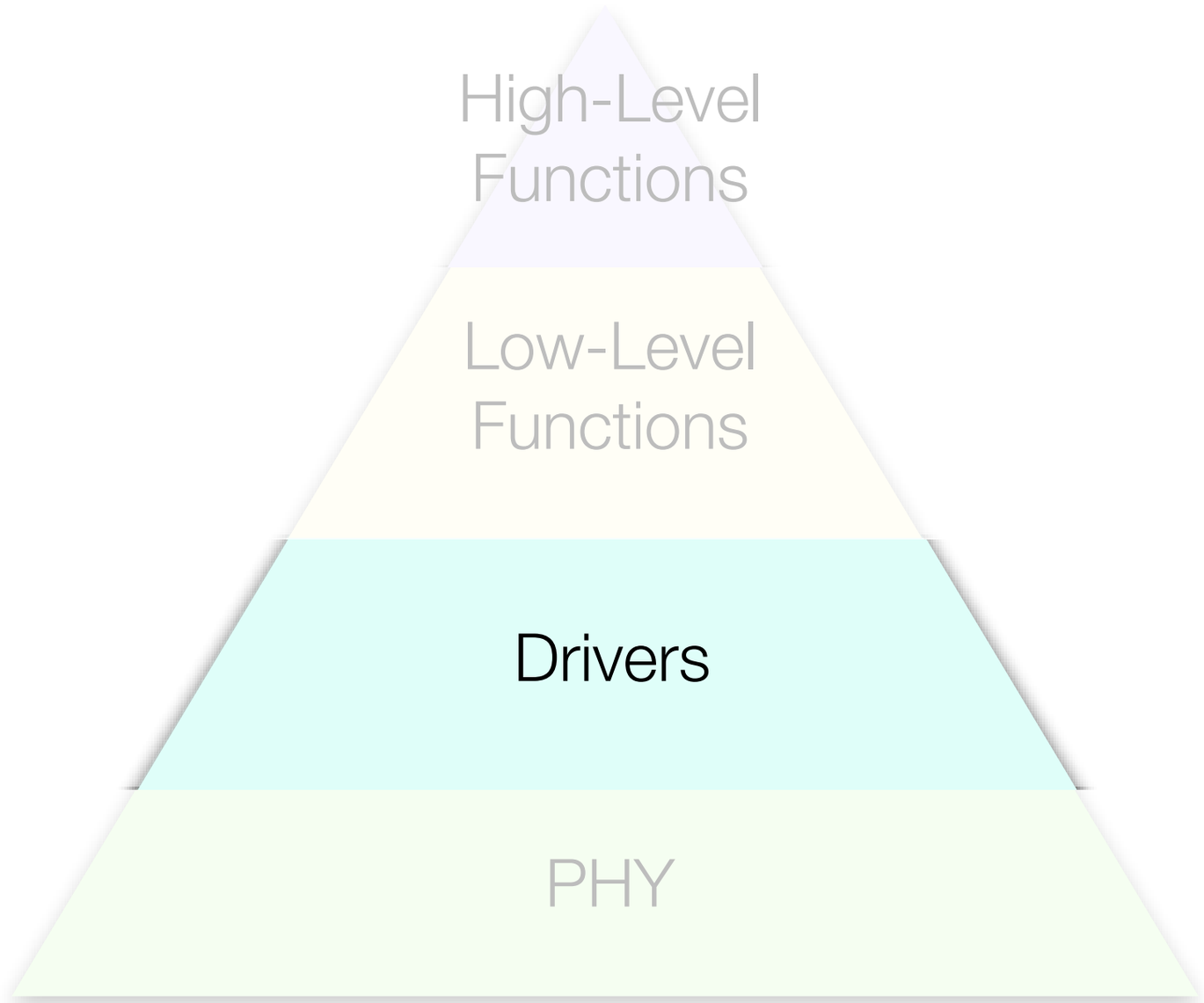
- Configure constellation size
- Thesholds in packet detection, automatic gain control, cross-correlation in receiver
- “Start” and “Stop” the PHY



WARPMAC

Radio Driver:

- Set center frequency
- Switch from Rx to Tx mode and vice versa



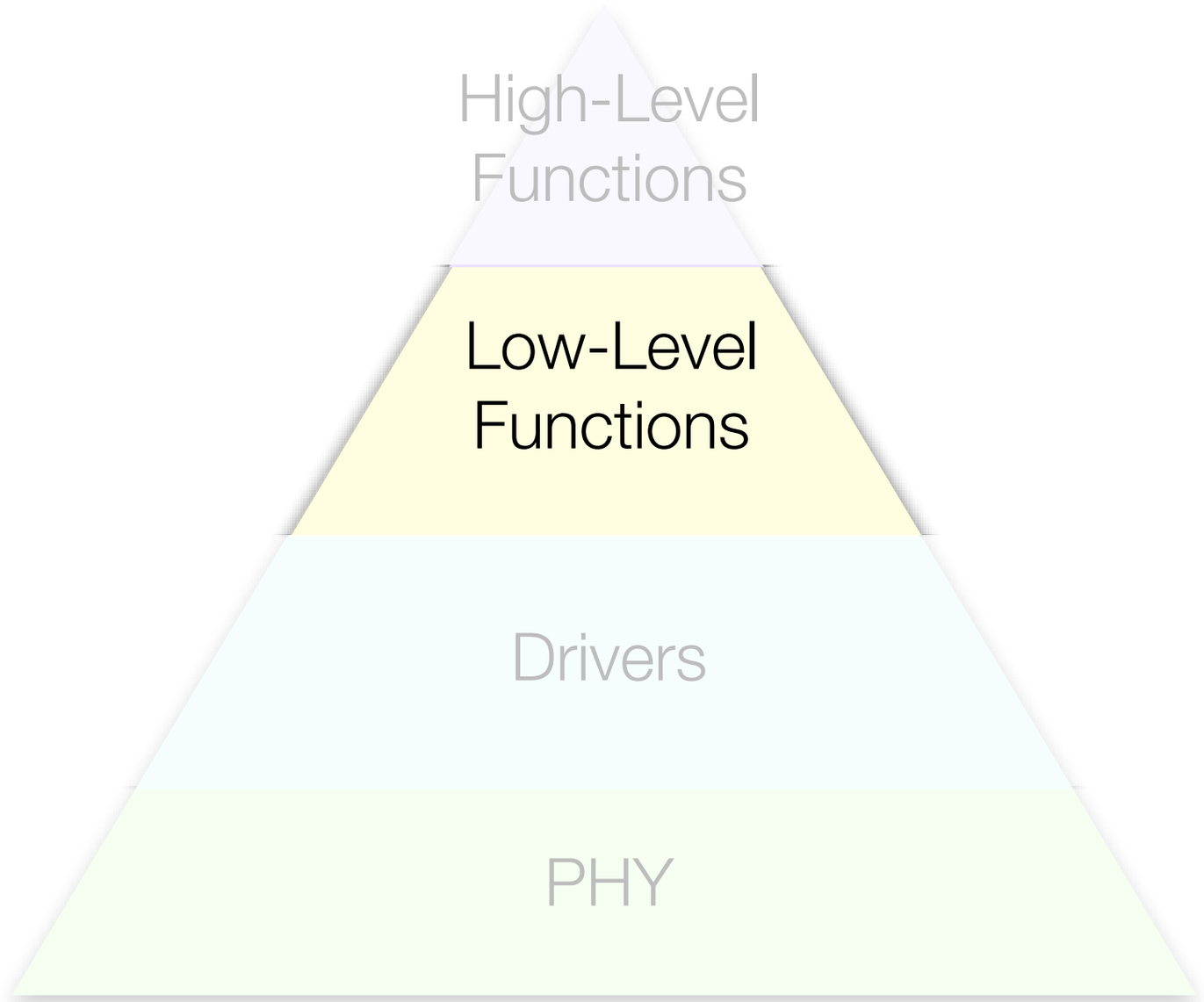
WARPMAC

- Wraps driver calls for another layer of abstraction

- For example:

warpmac_sendOfdm(myPacket)

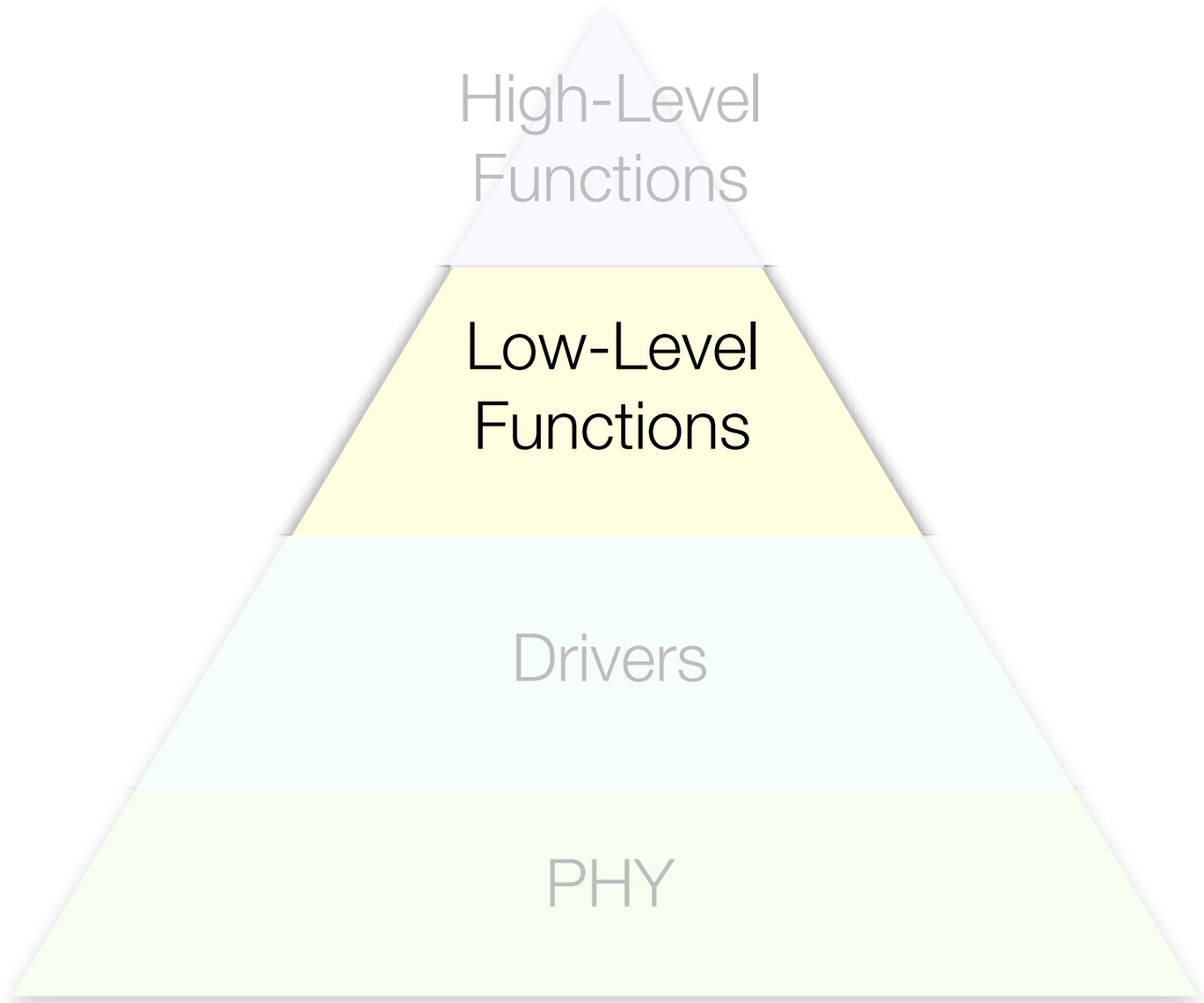
puts radio into transmit mode, loads payload into PHY, begins transmit



WARPMAC

Interrupt Handling:

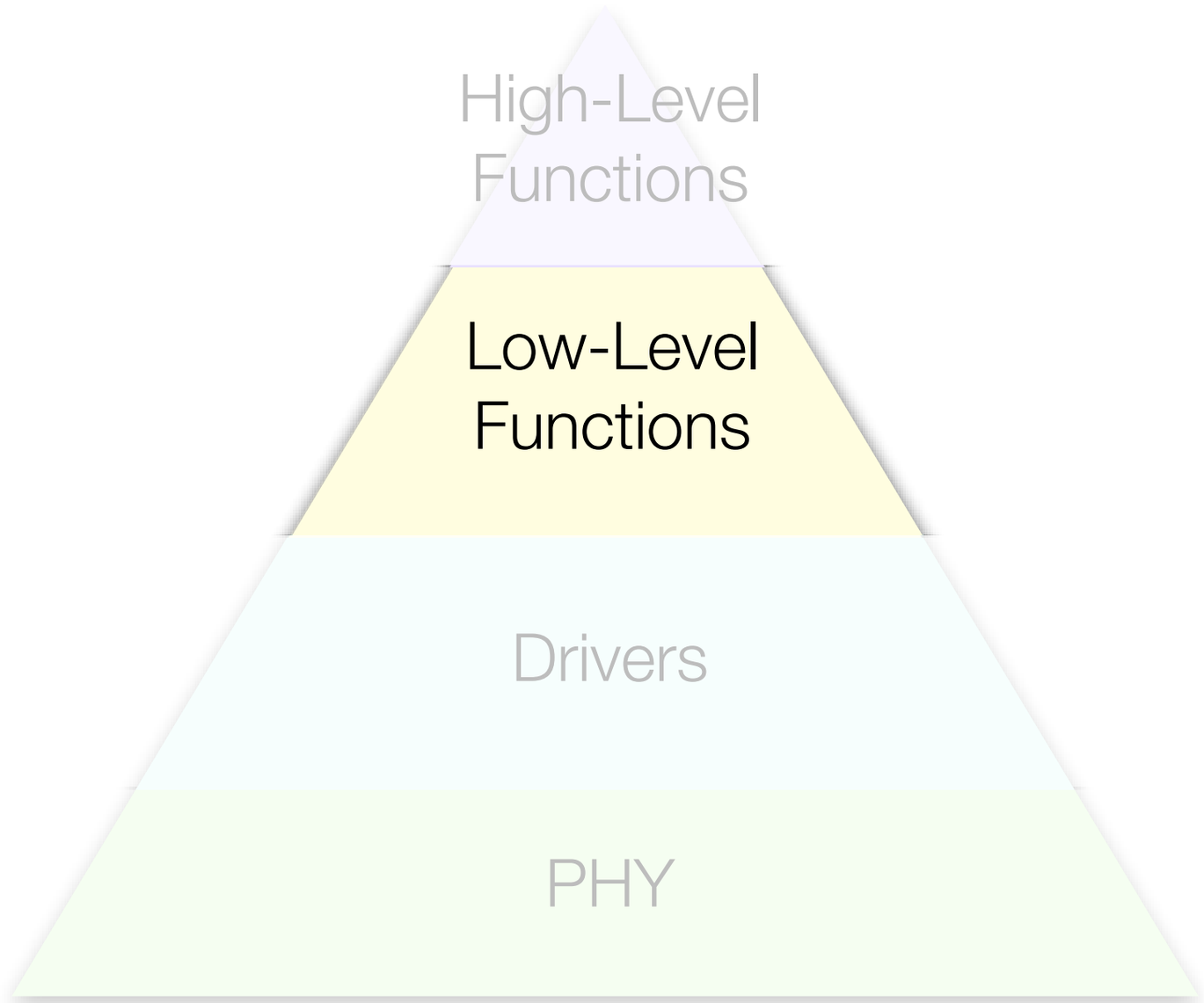
- Register functions to be called upon:
  - Reception of “Good” Packets
  - Reception of “Bad Packets”
  - Expiration of a timer



WARPMAC

Timer Control

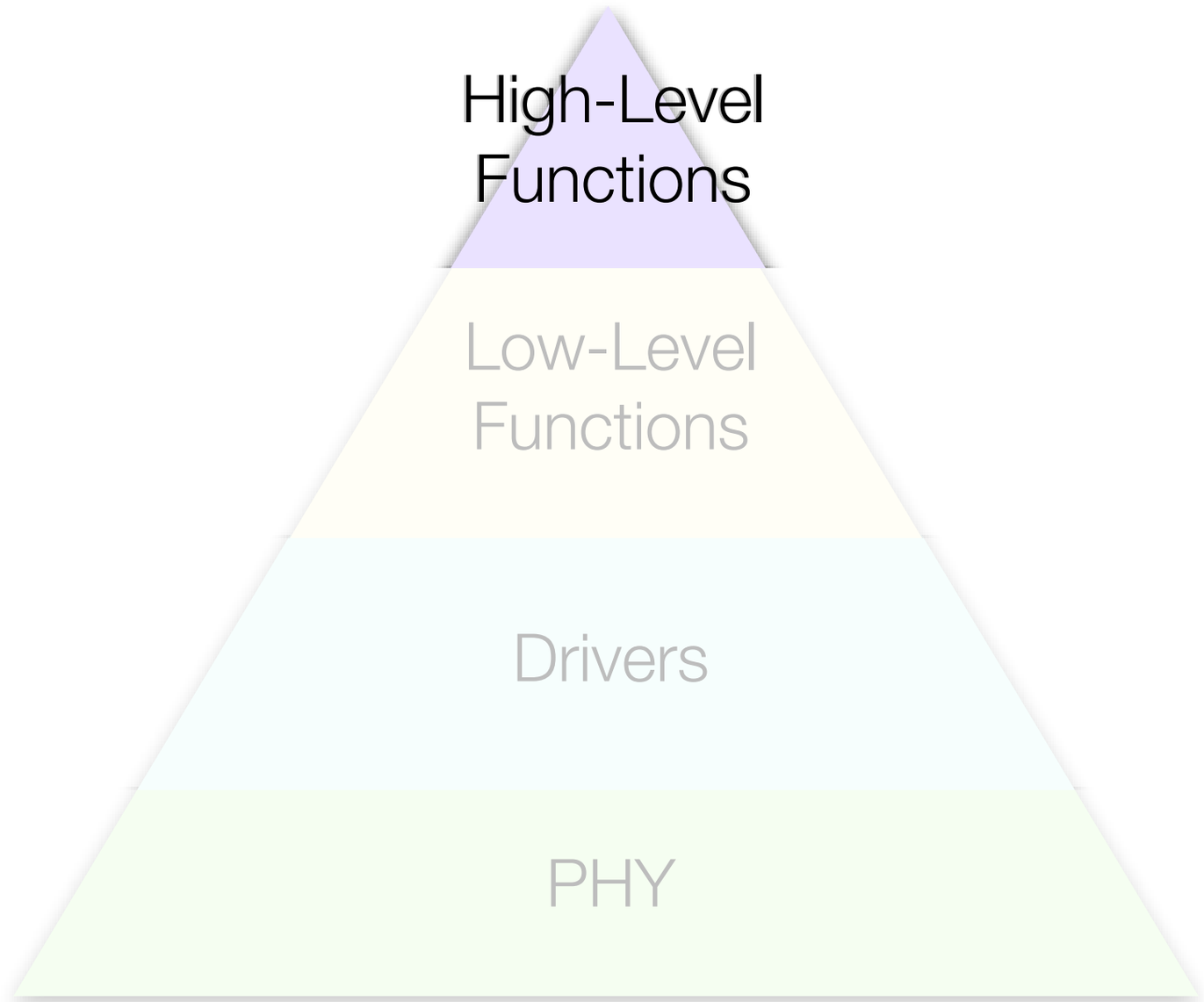
- Start a count down for a certain number a clock cycles
- User-registered handler will be called upon expiration



WARPMAC

- All the functions necessary to implement the ALOHA protocol

- For example, timer control function now abstracted to implement binary exponential backoff



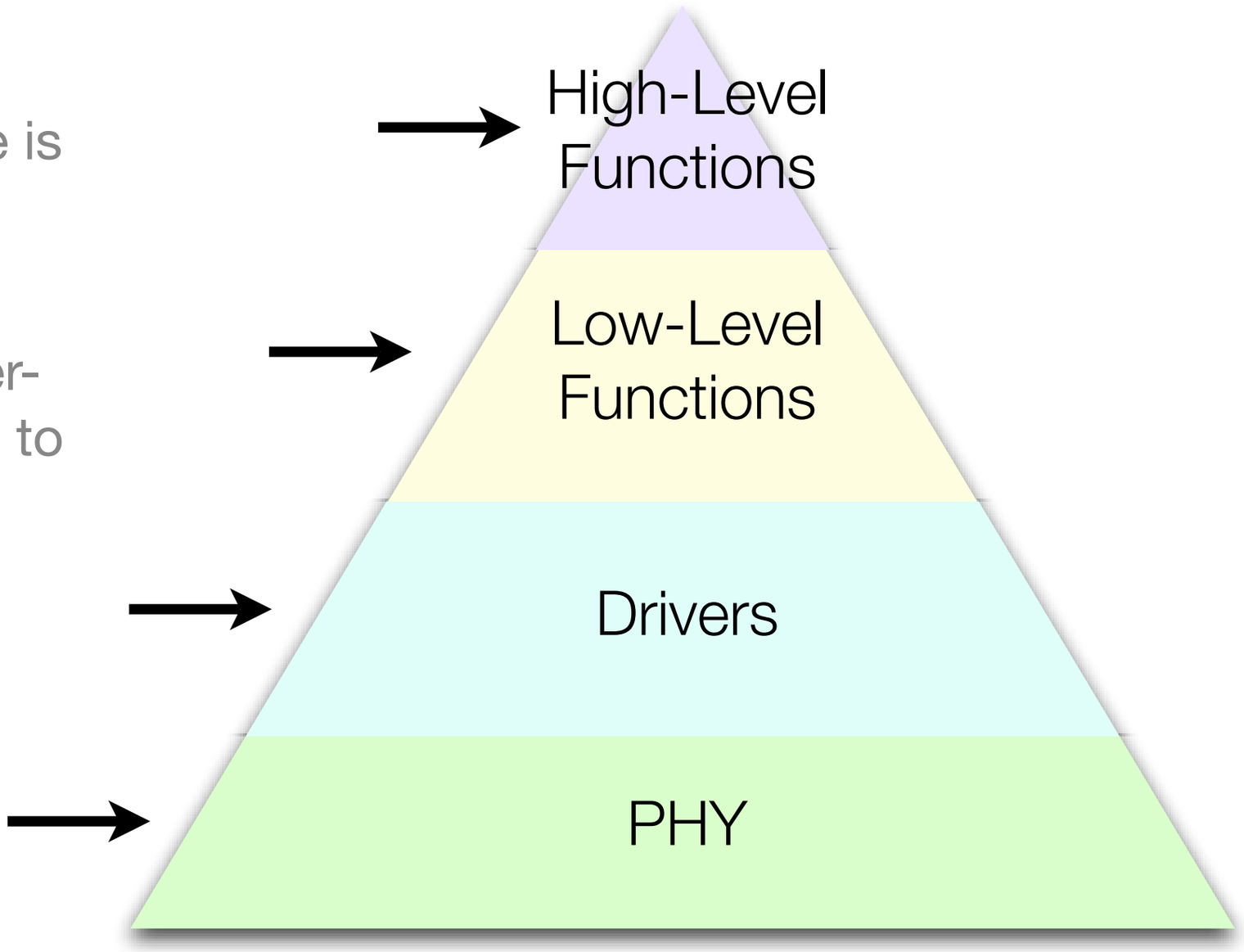
WARPMAC

Implementing Novel MACs:

- "Level" of WARPMAC to use is MAC dependent

- New PHYs, MACs, and lower-level functions will be added to the WARP repository:

  http://warp.rice.edu/trac

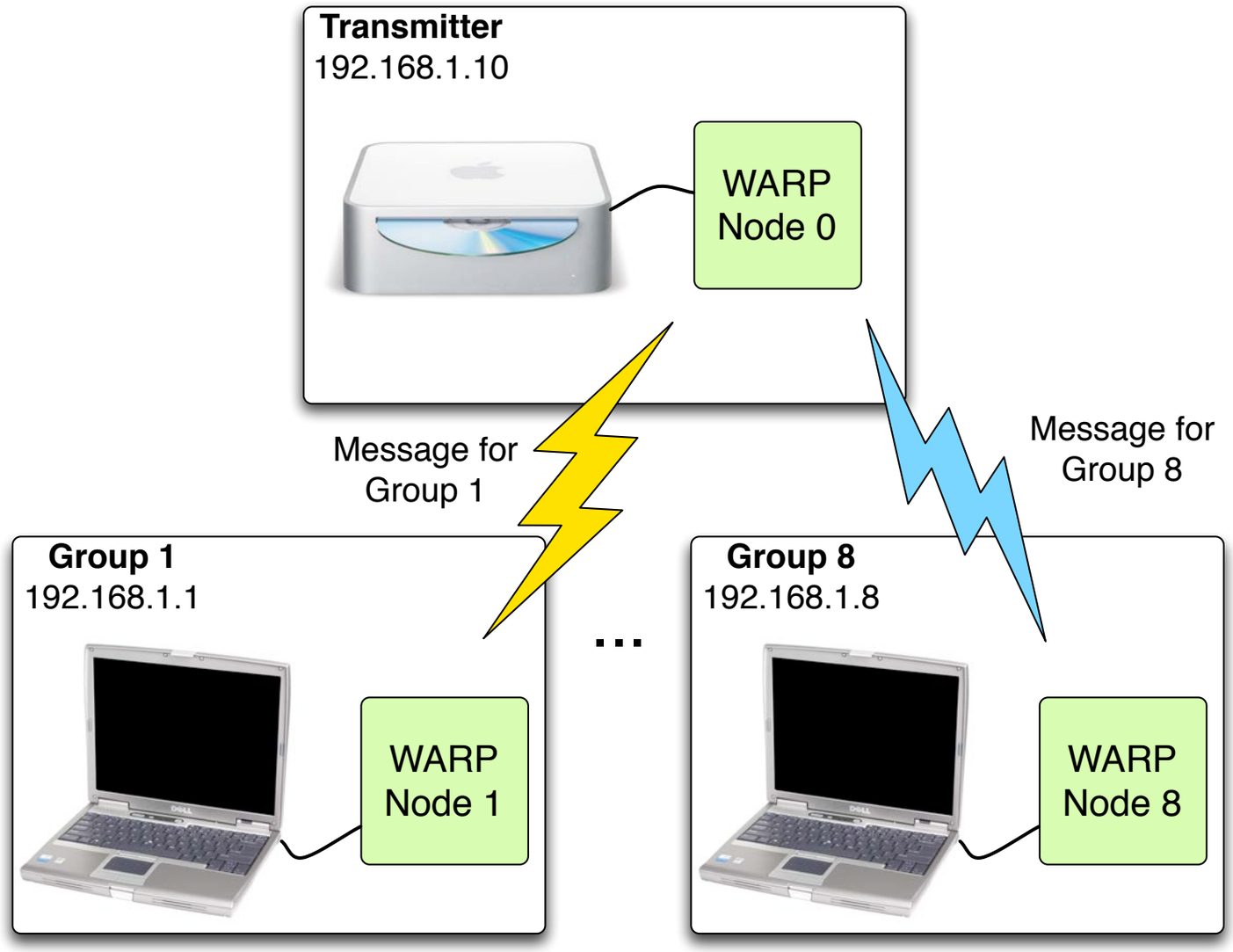


Overview of WARPMAC

- WARP Hardware - What's "under the hood"?
- Design Realization - What are the hardware requirements of a basic MAC?
- WARPMAC - What tools do we provide for MAC development?
- Examples - Current MACs at Rice

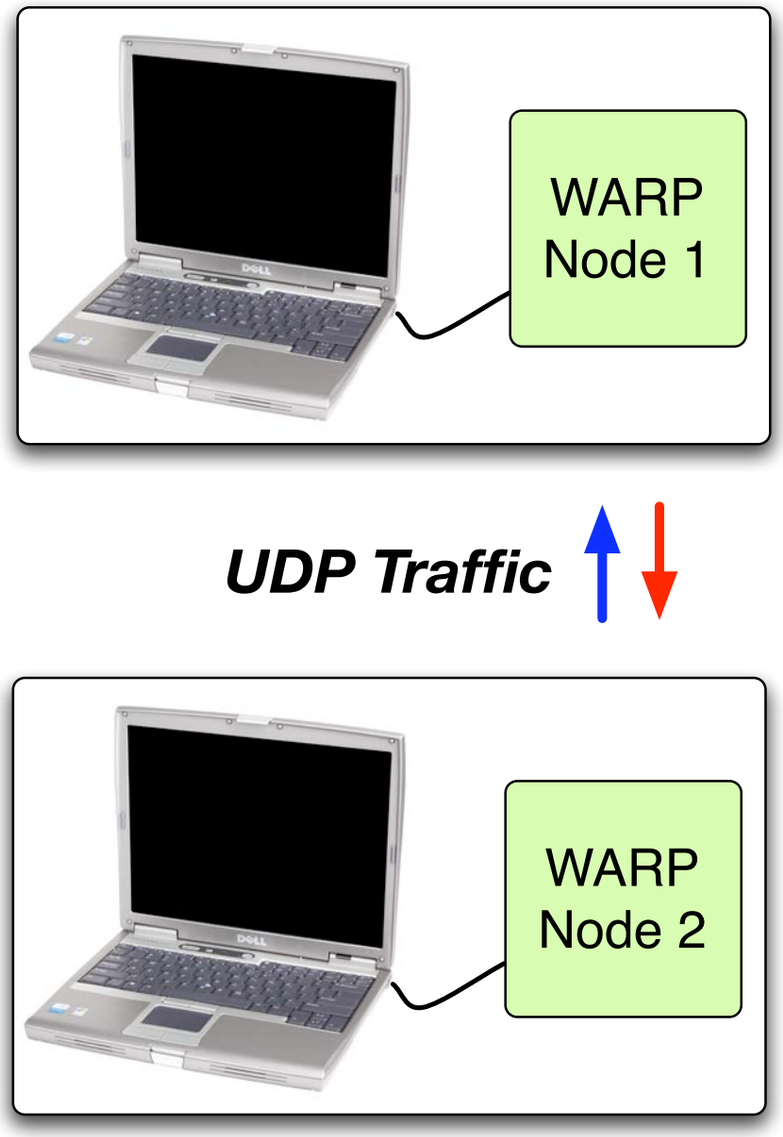
Current MACs at Rice:

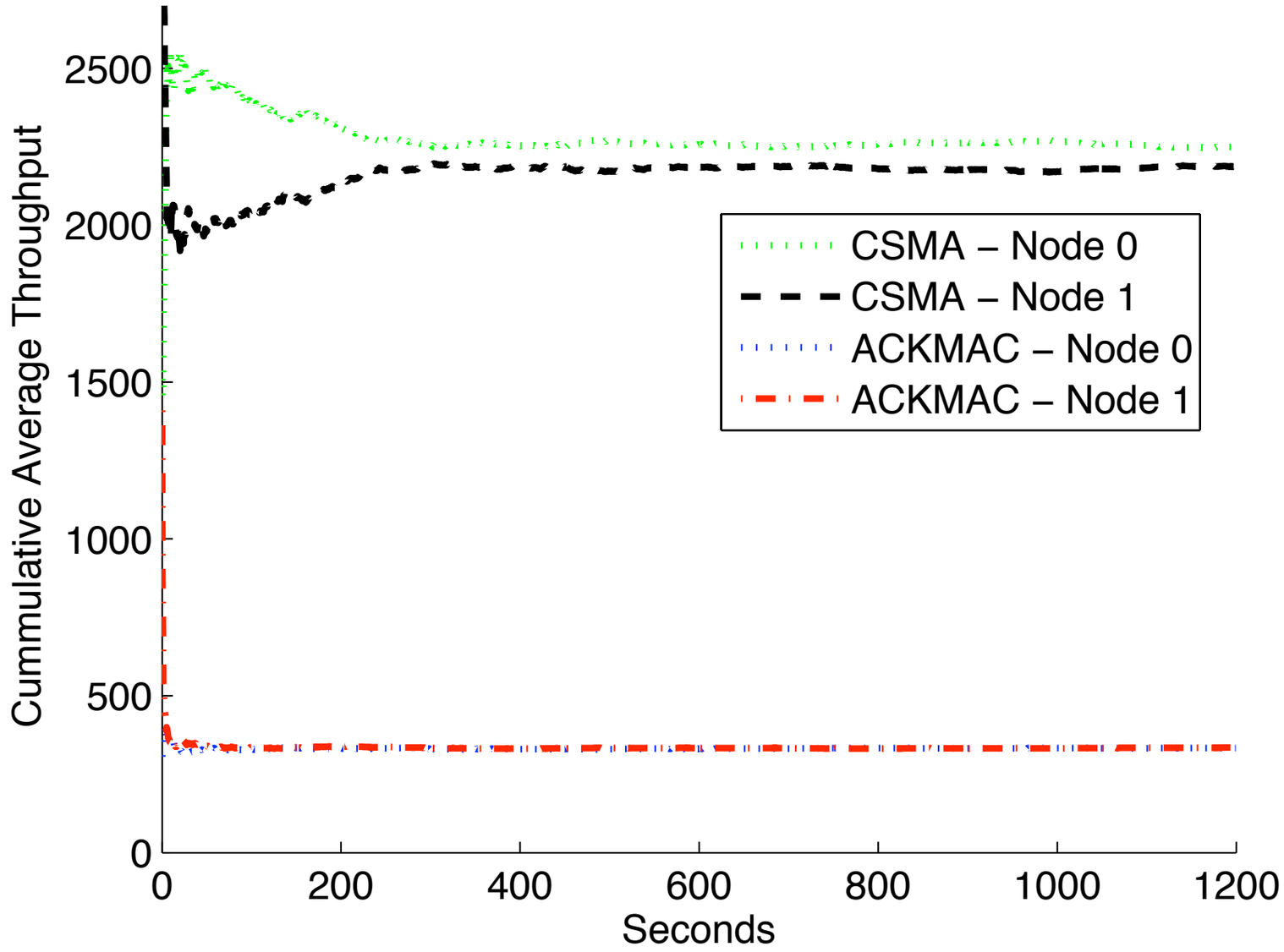
- ALOHA
  - Application-layer throughput measured at 6Mbps for a 12Mbps PHY
  - 1ms RTT, 60usec TAT
  - Tested in 9-node topology at WARP workshop (Rice 10/19/2006)



Current MACs at Rice:

- CSMA-enabled MAC

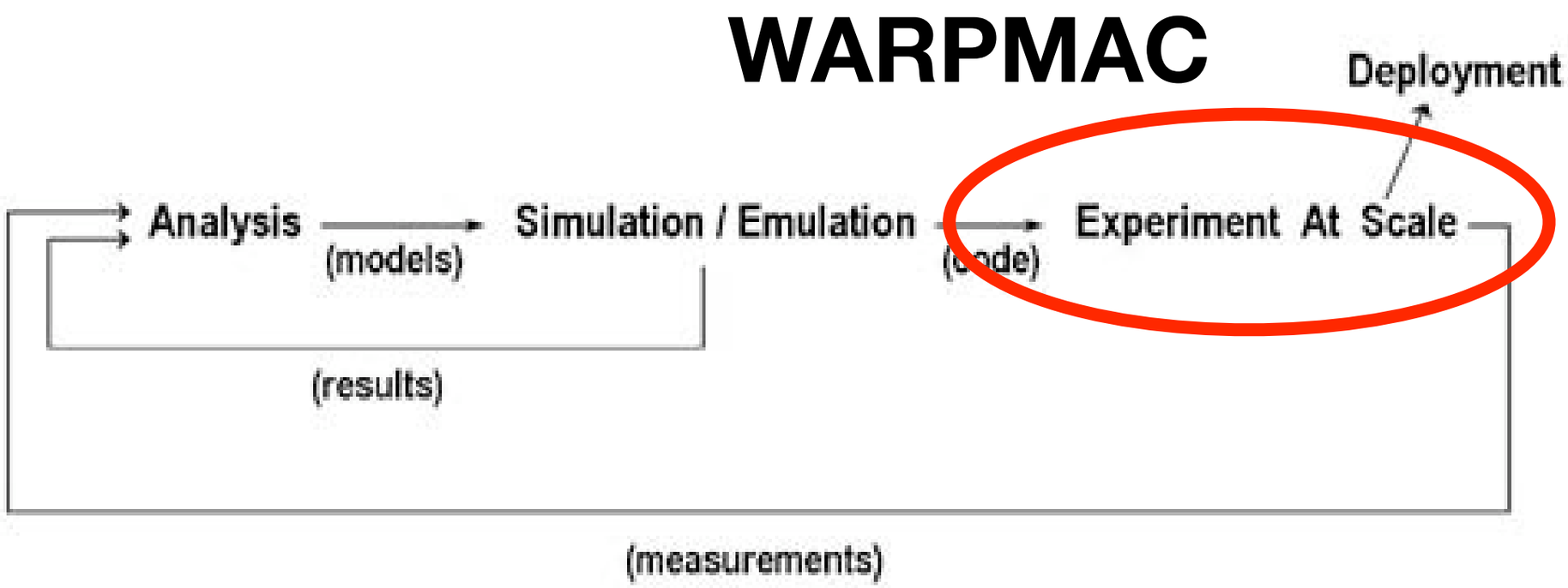




Summary

WARPMAC - Two-tiered MAC development framework for WARP

- High-level access for “current generation” random-access protocols
- Low-level access for the future



Questions?

http://warp.rice.edu

- wiki
- forums
- repository